A HIGH-SFDR DIRECT DIGITAL FREQUENCY SYNTHESIZER WITH EMBEDDED ERROR-COMPENSATION CMOS OTP ROM FOR WIRELESS RECEIVERS

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ABSTRACT: A direct digital frequency synthesizer (DDFS) using on-chip CMOS one-time programmable read-only memory (OTP ROM) is presented. A straight-line approximation algorithm for sinusoid with compensation is adopted such that the accuracy could be maintained and the cost is reduced. Most important of all, a CMOS OTP ROM is used as a look-up ROM table, which is implemented by a typical logic CMOS process. Therefore, the proposed DDFS can be integrated in any CMOS-based front-end circuit for wireless communication systems. The proposed DDFS design is fully implemented using a typical 1P6M 0.18 μm CMOS process. It has a 12-bit amplitude resolution with 86.89 dB spurious free dynamic range using a small ROM size of 256 bits. © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1695–1699, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24422

Key words: frequency synthesizer; DDFS; one-time programmable; OTP; wireless communication; straight-line approximation

1. INTRODUCTION

The frequency synthesizer is an important part of a communication system, particularly in the receiver front-end, where sinusoidal signals are required to down-convert a high-frequency-modulated input signal to an intermediate frequency (IF) band, which will then be demodulated into a baseband signal [1]. Phase-locked loops (PLL) were widely used for frequency synthesis traditionally. As the frequency is getting higher, the power consumption becomes a serious problem in a portable communication device. When compared with PLL, DDFS has faster frequency switching, higher resolution, better spectral purity, lower phase noise, and continuous-phase frequency switching. Moreover, DDFS allows direct phase and frequency modulation in the digital domain [2].

In prior DDFS researches, ROM-based (or namely table look-up) methods have been widely studied, for example, [3–5]. The conventional nonvolatile ROM such as EPROM, EEPROM, and flash EEPROM, are manufactured with a special process. As the SOC evolving lately, the programmable non-volatile memory manufactured with typical logic CMOS process is strongly needed to physically integrate the DDFS and ROM into a single chip.

Many researches for OTP ROMs have been proposed. Most of them used either fusing or antifusing technology [6], for example, polyfusing, oxide-nitride-oxide (ONO) [7], and metal-oxide-metal (MOM) [8, 9]. Polyfusing is not adaptable because of process changing, while the ONO and MOM require additional process steps. Therefore, none of them is suitable for CMOS-based SOC fabricated by a typical logic process. With the development of deep-submicron technologies, the gate oxide of transistors becomes very thin which makes break down thereof very much easy. The transistor can be punched-through (antifused) without damaging other circuits in a neighborhood region. Then, OTP ROM realized by logic CMOS processes without any postprocess is feasible. This kind of OTP ROM can be used to increase the flexibility and calibratability of an ASIC or SOC after chip fabrication. In this article, we propose a DDFS using the straight-line approximation for quadrant sinusoid. Most important of all, the error compensation is carried out by a COMS OTP look-up ROM table to save the hardware cost and justify the SOC feasibility.

2. THE PROPOSED DDFS DESIGN

A perfect sinusoidal wave is cyclic and symmetrical. It could be reconstructed with a quadrant waveform. The straight line approximation is deemed as one of the easiest algorithms to realize with digital circuitry. The classic straight line approximation approximates the quadrant sinusoid with n segment straight lines by choosing the closest slope and intercept. However, it will increase the number of processing units to design a high accuracy DDFS in the classic way, if n becomes very large.

<table>
<thead>
<tr>
<th>i</th>
<th>m_i</th>
<th>b_i</th>
<th>x</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3</td>
<td>3</td>
<td>0–11</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>14</td>
<td>12–21</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>34</td>
<td>22–29</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>32</td>
<td>30–31</td>
</tr>
</tbody>
</table>
The proposed DDFS is divided into two parts, that is, coarse approximation block (CAB) and fine approximation block (FAB). The low accuracy approximate waveform will be calculated in CAB part using the straight line approximation. Then, the error compensation will be carried out by looking up an OTP ROM table on the same chip to derive the waveform with a high resolution in FAB. The sinusoidal wave can be expressed as follows.

\[
y(x) = \begin{cases} 
  (m_0x + b_0)2^k + er_0(x), & x_0 \leq x < x_1 \\
  (m_1x + b_1)2^k + er_1(x), & x_1 \leq x < x_2 \\
  (m_{n-1}x + b_{n-1})2^k + er_{n-1}(x), & x_{n-1} \leq x < x_n 
\end{cases}
\]

where \(x\) is the output of the phase accumulator, whereas the \(m_i, b_i\) are the slope and intercept of each segment, respectively, \(er_i(x)\) is the error value of \(x\) to compensate the coarse approximation, and \(k\) is the shift index for saving the number of multipliers.

2.1. DDFS Design

Figure 1 shows the block diagram of the proposed DDFS design. The phase accumulator (PA) translates the frequency control word (FCW) into control signals of the other function blocks, P[6:0].

Generally, the phase accumulator works like a counter, whose parameters are decided by FCW. Thus, the frequency of the output sinusoidal wave can be adjusted. The first two bits of PA output (i.e., P[6:5]) are used to reconstruct the complete digital sinusoidal waveform from the quadrant waveform in the quadrant state control (QSC) block. The other bits (P[4:0]) notify the CAB and FAB parts as the variable \(x\) to calculate the quadrant approximate waveform magnitude accordingly. The CAB calculates the straight line approximation of the target sinusoidal wave, whereas the FAB looks up the table stored in an OTP ROM to get the error compensation value, \(er_i(x)\). The quadrant waveform, \(y(x)\), will be calculated by adding the straight line approximation and error compensation value. The digital output, SINE, is the complete sinusoidal waveform approximation reconstructed by switching the states of the quadrant sinusoidal waveform in QSC.

The proposed DDFS has an amplitude resolution of 12 bits. To reduce the hardware cost of the CAB and the FAB, the amplitude...
resolution of CAB is six bits, such that \( k = 6 \) is chosen. Besides, the four segments of straight line can approximate the quadrant waveform almost as good as the five segments of straight line by thorough MATLAB simulations. The 4-segment approximation requires less amplitude resolution of CAB and certainly less hardware cost. Table 1 is a selected combination of coefficients in the CAB part after detailed simulations. By Table 1, the CAB part calculates the coarse approximation as shown in Figure 2. Then, we can derive each \( \varepsilon r(x) \) by comparing it with the perfect sinusoidal waveform to generate the entries in the look-up ROM table. The simulation result after error compensation is shown in Figure 3. Figure 4 shows the error value between the output waveform and the perfect waveform. Because the largest error value is about \( 0.000122 < 2^{-12} \), the amplitude resolution of the DDFS is ensured to be 12 bits.

2.2. CMOS OTP ROM

Generally, there is a huge equivalent resistance between gate and bulk of a MOSFET fabricated by a standard CMOS process. If a high voltage is applied on the gate of the MOSFET, breakdown occurs to reduce the equivalent resistance sharply. This characteristic makes the standard CMOS process possible to realize OTP ROM. As long as we can control the programming time and voltage, we can write the data in the OTP ROM by “antifusing” the gate oxide correctly without damaging nearby circuitry.

Referring to Figure 5, the CMOS-based ROM cell is composed of three components: a storage element (SE), a high voltage blocking transistor (HVBT), and a data access transistor (DAT). In the programming mode, the target ROM cell will be selected by enabling word line (WL) and Data in (DI). The gate voltage of the SE in the target ROM cell will be pulled high by VPP to antifuse the gate oxide. HVBT will be turned on to relay the programming voltage to ground via DAT. The Read bar (RB), Data in (DI), and Ready to Program (RTP) will be pulled high to ensure the current path of target ROM cell in programming mode. In the mean time, HVBT of other ROM cells will be cut off for the protection of nearby circuitry.

Figure 6 The OTP ROM array

Figure 7 OTP ROM test key measurement statistics. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

Figure 8 Die photo of the proposed DDFS design. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

Figure 9 The postlayout simulation of a synthesized sinusoid. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]
to prevent the programming voltage from damaging their data. In
the reading mode, the binary digit stored in SE will be sensed from
the current through the DAT, and differentiated by the sense
amplifier (SA). In other words, the bit is stored in the SE in a
resistance state, which can be sensed by a transimpedance ampli-
fication circuits. The OTP ROM cell array in the proposed design
is shown in Figure 6.

To justify the feasibility of the CMOS OTP ROM, we have
taped out several CMOS test keys with different SE designs by a
typical 0.18 \textmu{}m CMOS process. The design parameters of SE,
including MOS types, sizes, and threshold voltages, have been
fully tested. Each type of the SE test key has been supplied with
high VPP until it is antifussed to find the most appropriate pro-
gramming voltage and time. It is found that the most stable SE is
the NMOS with 0.25 V threshold voltage (N N type), and the
VPP voltage (programming voltage) is 6.5 V by the statistics
shown in Figure 7(a). Notably, the size of the SE MOS does not
really affect the VPP voltage. The resistance of SE before and after
antifussing is measured on silicon to be about 100 K \textOmega{} and 100
M\textOmega{}, respectively, as shown in Figure 7(b), which justifies that it
is suitable to construct an OTP ROM cell or array.

3. IMPLEMENTATION AND MEASUREMENT

TSMC (Taiwan Semiconductor Manufacturing Company) 0.18
\textmu{}m 1P6M CMOS process is adopted to carry out the proposed
DDFS design. The die photo of the proposed design is shown in
Figure 8, the size of the chip core area is 841 \textmu{}m \times 1262 \textmu{}m
(1719 \textmu{}m \times 1883 \textmu{}m with pads). Figure 9 shows the sinusoidal
waveform. Test Error is the output of a build-in self test, indi-
cating the correctness of the proposed design. The FFT result of
the waveform is shown in Figure 10, where the spurious free
dynamic range (SFDR) is 86.89 dB. The shmoo plot shown in
Figure 11 reveals that the proposed DDFS chip can work correctly
at the maximum frequency of 76 MHz with 2.2 V supply voltage.
The measurement result of the QSC output, that is, SINE, is the
same as the simulation result. Partial of the detailed readout
measurement result of OTP ROM array is shown in Figure 12. The
characteristics of the proposed design as well as the comparison
with prior ROM-based DDFS designs are tabulated in Table 2. The
proposed DDFS has the smallest ROM size and the best SFDR
without sacrificing the amplitude resolution. Most important of all,
the proposed DDFS is the only solution to integrate the digital
DDFS with on-chip ROM on a single typical CMOS logic process.

4. CONCLUSION

We have proposed a DDFS with error-compensation OTP ROM
on a typical logic CMOS process. The straight line approximation
for the quadrant sinusoid has been adopted in addition to the error
compensation with small look-up ROM table without any loss of
resolution, and the proposed DDFS design provides a better solu-
tion in terms of ROM size and SFDR.

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\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|}
\hline
Process (\textmu{}m) & 0.35 & 0.35 & 0.25 & 0.35 & 0.18 \\
\hline
Amplitude resolution (bits) & 12 & 9 & 12 & 12 & 12 \\
\hline
Phase resolution (bits) & 28 & 32 & 24 & 8 & 5 \\
\hline
ROM size (bits) & 448 & 368 & N/A & 3072 & 256 \\
\hline
SFDR (dB) & 84.2 & 55 & 80 & 78 & 86.89 \\
\hline
\end{tabular}
\caption{The Comparison of the Proposed DDFS with Prior Works}
\end{table}
A SMALL PRINTED DUAL-BAND ANTENNA FOR MOBILE PHONES

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ABSTRACT: A small printed antenna is proposed for dual-band applications. The antenna is patterned on the front of an 0.8-mm FR4 substrate to obtain a low-frequency resonance and a stub is patterned on the back of the substrate to obtain a high-frequency resonance. The antenna without ground plane is small (8 \times 35 \text{mm}), and it is suitable to operate as an internal antenna. For \(S_11\) less than -6 dB, the antenna operates at 900 MHz with a bandwidth of 66 MHz, and at 1.8 GHz with a bandwidth of 130 MHz. Maximum radiation efficiencies were 52% at both 900 MHz and 1805 MHz. © 2009 Wiley Periodicals, Inc.

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Key words: inverted-F antenna; dual-band; printed antenna; mobile phone

Figure 1 Configuration of the proposed printed dual-band antenna. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]