A Transceiver Front End for Electronic Control Units in FlexRay-Based Automotive Communication Systems

Chua-Chin Wang, Senior Member, IEEE, Gang-Neng Sung, Student Member, IEEE, Po-Cheng Chen, Student Member, IEEE, and Chin-Long Wey, Senior Member, IEEE

Abstract—This paper presents an in-car networking transceiver front end that is compliant with FlexRay automotive electronic standards. A low-voltage differential-signaling-like transmitter is proposed to drive the twisted pair of the bus. Furthermore, a three-comparator scheme is used to carry out bit slicing and state recognition at the receiver end. In order to resist process and temperature variation, a 20-MHz clock generator with process, supply voltage, and temperature compensation is proposed in this paper. A prototype system as well as a chip implemented by using a typical 0.18 μm single-poly six-metal CMOS process is reported in this paper. The proposed prototypical transceiver front end has been tested by the thermo chamber and a FlexRay development board to certify its operation in the [-40 °C–+125 °C] temperature range and FlexRay standards. The power consumption of the whole chip is 43.01 mW at a 10 Mbit/s throughput. The core area of this design is 0.117 mm². The maximal throughput of the proposed prototypical transceiver front end can reach 40 Mbit/s.

Index Terms—Automobile electronic, FlexRay, in-car networking, low power, transceiver.

I. INTRODUCTION

CAR ELECTRONICS has been deemed as the fourth “C” right after computer, communication, and consumer electronics. Many novel electronic devices have been introduced and installed in recently publicized cars. Therefore, an in-car network has been proposed to control and supervise all of the automobile electronics. Owing to the fast evolution of semiconductor technology, devices with an electronic control unit (ECU) have been installed in automobiles. In 1990, the average quantity of ECUs in an automobile was 14. By now (2008), the number of ECUs reaches 40 to 60. Notably, certain luxury automobiles can even have over 100 ECUs. According to the prediction of the marketing research institution Gartner, the market scale of global automobile-used ECU will grow up to $5300 million in 2008 and grow up to $6300 million further in 2012.

The FlexRay standard [1] is designed for in-car networks. It will not replace existing networks. By contrast, it can combine or integrate with these networks, including controller area network, local interconnection network [2], Media Oriented System Transport [3], [4], J1850 protocol [5], etc. FlexRay requires 10 Mbit/s data rate in either one of the two channels of an ECU. If a single channel is used alone, the total data rate should reach 20 Mbit/s. Therefore, even the video signals, multimedia, and control signals can communicate via the FlexRay system with such a high-bandwidth benefit. The goal of FlexRay is that the automobile is X-by-wired (X = steer, brake, accelerate, audio/video, safety, etc.), i.e., all of the current machine-based mechanisms, e.g., steer, brake, accelerate, etc., can be controlled by electronics through FlexRay-based networks. Fig. 1 shows a scenario when FlexRay is used in a car. Notably, different networking systems can be integrated by the FlexRay backbone.

As well known by car industry and business, “safety” and “reliability” are the primary design requirements. Otherwise, we can put it another way: “fault tolerance” is a must. Therefore, instead of using some novel or even radical design or circuitry, it is better to select well proven but a little bit old designs to ensure safety and reliability. The major contribution of this work is that we successfully integrate several prior circuits with our circuitry and make them work and function together to meet the requirements set by FlexRay standards.

II. TRANSCEIVER FRONT-END DESIGN FOR IN-CAR NETWORKING SYSTEMS

Fig. 2 shows the block diagram of ECU nodes in a FlexRay system. The component of each node contains a host microcontroller (μC), a communication controller (CC), a bus guardian, and two bus drivers (BDs). Traditionally, the transceiver front end in the BD should be implemented by a high-voltage silicon process [6], [7]. However, our design can be implemented by a typical 0.18 μm mixed-signal CMOS process instead. Hence, the proposed design can be integrated with other digital blocks easily besides the advantage of reduced cost.

According to the FlexRay standards [1], there are two signals of the BD, denoted as Bus Plus (BP) and Bus Minus (BM). BP and BM are, in fact, a pair of differential signals which can reduce the noise on a connection by rejecting common-mode interference and have tolerance of ground offsets. The timing and amplitude characteristics of BP and BM required by the FlexRay standards are shown in Fig. 3.
The block diagram of the proposed design is shown in Fig. 4, including the regulators, a transmitter (Tx) circuit, and a receiver (Rx) circuit. Data0C, Data1C, Idle_C, and Idle_LP_C are one-hot decoded control signals for the Tx to transmit the data and the state. On the other hand, Rdata and Ridle are control signals generated by the Rx after the received differential signals are recovered and decoded. The functions associated with those control signals and the differential-bus signals are summarized in Table I.

A. Tx

There are a total of four types of “Signals” in the FlexRay systems, which are the Data1 Signal and Data0 Signal in the Active State, and the Idle_LP Signal and Idle Signal in the Idle State. We propose a low-voltage differential-signaling (LVDS)-like Tx design as shown in Fig. 5. LVDS is a differential-signaling scheme, which means that it transmits two different voltages that will be compared at the Rx. LVDS utilizes the voltage difference between the two wires to encode the information [8], [9]. In the proposed Tx design, Data0C, Data1C, Idle_Lo, and Idle_LP_Lo are control signals decoded by a one-hot decoder and fed into the BD. Data0_C and Data1_C are a pair of digital differential signals generated by a CC to notify the bit to be transmitted over the bus. Idle_C and Idle_LP_C are a pair of idle signals. When the Idle_C is asserted, BP and BM must be locked on the same Vref, which is 2 V in this work. By contrast, as soon as the Idle_LP_C is asserted, indicating that the low-power mode is chosen, then BP and BM are pulled down to GND. Notably, VDD denotes that the supply voltage is 3.3 V. En and EnB are enable and disable signals, respectively, generated by Idle_C and Idle_LP_C to select the gate drives of M101, M102, M103, and M104. The relationship between the control signals BP and BM is presented in Table I. For instance, if Data1_C = 1, Data0_C = 0, Idle_C = Idle_LP_C = 0, then En = 0 and EnB = 1 such that M103 and M102 are both turned on, which will pull down BM and pull up BP to generate Data1 signal. Then, logic “1” is transmitted.

In order to conform to all the required specifications of the FlexRay standards with rigorous automotive environmental temperature, the dimensions of the MOSs are selected carefully after thorough simulations. For the same reason, the variation of differential voltages caused by the process, supply voltage, and temperature (PVT) should be taken into account. Similarly, the rejection to the process and temperature drifting can be achieved by tuning the aspect of each transistor. The derivation steps of each transistor size is described as follows.

First of all, we select 0.8 V as the voltage difference between the central voltage and the maximal voltage of each differential signal, which is compliant with the FlexRay standards, as shown in Fig. 3. According to the FlexRay specifications, the physical bus wire should be loaded with a small resistor of 40 or 45 Ohm in parallel with a large capacitor of 100 pF. Therefore, the current

---

**Table I**

FUNCTIONS OF THE CONTROL SIGNALS, BP, AND BM

<table>
<thead>
<tr>
<th>Control signal of transmitter</th>
<th>Differential signal of BP</th>
<th>Differential signal of BM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data0</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Data1</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Idle</td>
<td>Idle_bias(^1)</td>
<td>Idle_bias</td>
</tr>
<tr>
<td>Idle_LP</td>
<td>Idle_LP_bias(^2)</td>
<td>Idle_LP_bias</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Differential signal on the bus</th>
<th>Rdata</th>
<th>Ridle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data0</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Data1</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Idle</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Idle_LP</td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>

**Diagram**

- Fig. 1. FlexRay used as an in-car network.
- Fig. 2. Block diagram of ECU nodes in a FlexRay system.
Fig. 3. Characteristics of BP and BM required by FlexRay standards [1].

Fig. 4. Block diagram of the proposed design.

Fig. 5. Schematic of the proposed Tx

\[ I = \frac{0.8 \text{ V} \times 2}{40 \Omega} = 0.04 \text{ A} = 40 \text{ mA}. \]  

Referring to the drain current in (2), we can estimate the dimension of each transistor, where \( V_{GS} = 3.3 \text{ V}, V_{DS} = 2 - 0.8 = 1.2 \text{ V}, \) and the channel-length-modulation factor, denoted as \( \lambda, \) is assumed as 0.01 by using at least five times of the feature length. Notably, the process parameters are tabulated in Table II, i.e.,

\[ I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \]  

where \( \mu \) is the mobility of the MOS, \( C_{ox} \) is the oxide capacitance which is given as \( \varepsilon_{ox}/t_{ox}, \) and \( V_{th} \) is the threshold voltage.

Considering environmental temperature and reliability, several factors that might affect the characteristics of (2) should be taken into account. Two of the most critical parameters that vary with temperature are the mobility of the charge carriers and the threshold voltage. The variation of these two factors are shown in (3) and (4), respectively, where the temperature coefficient \( \alpha_{V_{th}} \) is negative [10], [11]. Other major factors affecting the threshold voltage and the mobility are variations of gate-oxide thickness and doping concentrations.

\[ \mu \propto T^{-2.2} \]  

\[ V_{th}(T) = V_{th} - K(T - T_0) = V_{th}(1 + \alpha_{V_{th}} T). \]  

Process variation mainly due to variations in gate-oxide thickness and doping concentrations might also slightly affect the threshold voltage and the mobility of the MOS transistor.

The mismatch between the raising time and the falling time of the differential signals are also defined strictly \( \leq 4 \text{ ns} \) which

<table>
<thead>
<tr>
<th>Demanded Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{th}^{NO} )</td>
<td>0.741</td>
</tr>
<tr>
<td>( V_{th}^{FO} )</td>
<td>-0.697</td>
</tr>
<tr>
<td>( \mu^{NO} )</td>
<td>0.040</td>
</tr>
<tr>
<td>( \mu^{FO} )</td>
<td>0.013</td>
</tr>
<tr>
<td>( t_{ox,n} )</td>
<td>6.80 \times 10^{-9}</td>
</tr>
<tr>
<td>( t_{ox,p} )</td>
<td>6.77 \times 10^{-9}</td>
</tr>
</tbody>
</table>

Fig. 6. Schematic of the proposed Rx.
means that the aspect ratio of the p-type and n-type transistors should be carefully selected. By iteratively employing the operating point analysis and simulation, accurate dimensions of each MOS transistor can be derived.

**B. Rx**

Apart from the Rx circuits’ design of traditional buses, the Rx for FlexRay systems must recognize the Idle State besides slicing the received bits. Therefore, we propose a three-comparator scheme to achieve the required functions. Comparator0 is used to determine if Data0 or Data1 is in the Active State. Comparator1 and Comparator2 are used to detect whether the input signals on the bus are in the Idle State or not. For instance, if BP = BM, the outputs of Comparator1 and Comparator2 are reversed and Ridle is asserted. Meanwhile, the Rdata is asserted as well. Then, the Rx is able to recognize the Idle State on the bus. The source–drain (S-D) connected MOS M201 is used as a capacitive filter to remove the glitches that occurred resulting from switching between Comparator1 and Comparator2. Fig. 6 shows the schematic of the proposed Rx.

These three comparators are constructed by low-power comparator circuits [12]. The circuit mainly consists of three blocks: Preamplification, Decision circuit, and Output buffer, as shown in Fig. 7. Fig. 8 shows the schematic of the comparator. A differential pair and active loads are used to achieve the Preamplification function. The Decision circuit needs to distinguish in a few millivolt level the difference between the differential inputs in order to have a high precision. Therefore, the resolution of the output currents of the preamplifier is critical. By (5), we attain

\[ I_{O+} = \frac{g_m}{2} (V_+ - V_-) + \frac{I_{SS}}{2} = I_{SS} - I_{O-} = 20 \mu A - I_{O-}. \]  

\[ (5) \]

The Decision circuit needs to distinguish in a few millivolt level the difference around the GND voltage in order to have a high precision. We use a positive feedback network composed of M11 and M12 to increase the gain of the Decision circuit.

If \( I_{O+} \gg I_{O-}, \beta_{10} = \beta_{13} = \beta_A, \) and \( \beta_{11} = \beta_{12} = \beta_B, \) where \( \beta_{10}, \beta_{11}, \beta_{12}, \) and \( \beta_{13} \) are the \( \beta \)’s of M10, M11, M12, and M13, respectively, then transistor M10 and M12 are turned on, and M11 and M13 are turned off. We can derive \( T_{V+} \) by (6), where \( V_{\text{thm}} \) is the threshold voltage of the NMOS.

\[ T_{V+} = \sqrt{\frac{2I_{O+}}{\beta_A}} + V_{\text{thm}}. \]  

\[ (6) \]

When \( I_{O-} \) increases and \( I_{O+} \) decreases at the same time, the output voltage of the Output buffer will be inverted, given that the gate voltage of M7 is equal to \( V_{\text{thm}} \) of M6. In the meantime, the drain current of M11 increases, and the drain current of M10 decreases. Then, M12 will be turned off because the \( V_{DS} \) of M10 decreases. Then, we can derive the \( I_{O-} \) as follows:

\[ I_{O-} = \frac{\beta_B}{2} (T_{V+} - V_{\text{thm}})^2 = \frac{\beta_B}{\beta_A} \cdot I_{O+}. \]  

\[ (7) \]
Based on (7), if $\beta_B = \beta_A$, we can observe that the output voltage will be inverted when $I_{O+} = I_{O-}$. Besides, we can add the hysteresis effect by regulating $\beta_A$ and $\beta_B$ to reject the noise coupled from the power supply.

The Output-buffer stage is used to slice the output signal of the Decision circuit into digital signals. The circuit accepts a differential input signal without any limitation regarding slew rate. A self-biasing differential amplifier and an inverter are used in this Output buffer, as shown in Fig. 8. The inverter, composed of M21 and M22, increases the gain of the Output buffer and avoids the load effect of the self-biasing differential amplifier. Notably, a hysteresis design is included to reject the coupled noise.

C. Design of the Voltage Regulator

Since stable reference voltages are needed in Tx and Rx, respectively, to serve as the common-mode bias voltages in the differential signaling on the bus, we utilize a low-dropout voltage regulator to provide these stable voltages [11]. Fig. 9 shows the schematic of the voltage regulator. The regulator provides a stable voltage reference to reject the variation and noise from the supply voltage.

A bandgap bias circuit generates a PVT-independent reference voltage $V_{bg}$. The series resistors $R_{301}$ and $R_{302}$ monitor the output voltage by a simple voltage division. A feedback voltage $V_{fb}$ is fed back to be compared with the output voltage of the bandgap circuit by an error amplifier. The error amplifier then feeds a control voltage into the pass transistor $M_{316}$ to regulate the output voltage according to the difference between the feedback and output voltages of the bandgap circuit. The faster speed of the feedback loop comes along with the more stable output voltage. The loop gain of the voltage regulator feedback loop is 68.7 dB. It is measured by $V_{ref}$ over $V_{bg}$, given a small testing signal at $V_{bg}$.

III. 20-MHz Clock Generator With PVT Compensation

When it comes to vehicle applications, reliability and safety are classified as among the most important issues. Since the time-triggered scheme is required by FlexRay systems, several conscientious and careful timing characteristics are defined. Thus, a high-precision clock generator with reliable PVT compensation is very much needed in FlexRay-based ECUs. Fig. 10 shows the architecture of the proposed 20-MHz clock generator. The regulator provides a stable voltage reference, which could reject the variation and noise from the supply voltage. A three-stage differential ring oscillator is used in this design with a replica bias circuit generating a stable bias to the active load. The last part of this design is a differential-to-single converter, which could provide a 50% duty-cycle output [13]. The compensation scheme for both process and temperature variations adopts a threshold-voltage compensation mechanism [14]. The details of each block of the proposed 20-MHz clock generator are described as follows.

A. Differential Ring Oscillator

The ring oscillator with differential delay cells is preferred due to its better substrate and supply-noise rejection capability.
Fig. 11. Schematic of the three-stage ring oscillator.

Fig. 12. Schematic of the proposed delay cell.

Fig. 13. Schematic of the proposed replica bias circuit.

The delay of each stage can be tuned by changing $V_{\text{current}}$ or/and the output swing, which means changing $V_{\text{ctrl}}$.

### B. Replica Bias Circuit

To generate a constant oscillator amplitude regardless of process and temperature conditions, a replica bias circuit is used to provide the required bias voltages for each delay cell. Fig. 13 shows the schematic of the proposed replica bias circuit. $V_{\text{comp}}$ is the compensation voltage generated from the process and temperature compensation circuit. A feedback bias loop using OPA1 forces the voltage drop on M604 to be equal to $V_{\text{comp}}$ by tuning the current bias $V_{\text{current}}$. The symmetric structure (M605 ~ M608) replicates $V_{\text{comp}}$ to $V_{\text{ctrl}}$. The bias current could be derived approximately by using the standard square-law method, i.e.,

$$I_{\text{ref}} \approx K_{\text{L004}} \frac{W_{\text{L004}}}{L_{\text{L004}}} (V_{\text{Regu18}} - V_{\text{thr004}} - V_{\text{comp}})^2.$$  \hspace{1cm} (9)

The delay produced and the frequency of the ring oscillator are derived, respectively, as follows:

$$t_d = \frac{C_{\text{out}} (V_{\text{Regu18}} - V_{\text{comp}})}{I_{\text{ref}}}$$  \hspace{1cm} (10)

$$f = \frac{1}{N \cdot t_d}$$  \hspace{1cm} (11)

where $N$ is the number of stages in the ring oscillator, which is three in our design.

By substituting $I_{\text{ref}}$ in (10) with (9), $t_d$ is derived. Then, $t_d$ is plugged into (11). Finally, the frequency of the ring oscillator could be expressed as a function of $V_{\text{comp}}$, i.e.,

$$f \approx K_{\text{L004}} \frac{(W/L)_{\text{L004}}}{N \cdot C_{\text{out}}} (V_{\text{Regu18}} - V_{\text{thr004}} - V_{\text{comp}})^2.$$  \hspace{1cm} (12)

### C. Process and Temperature Compensation Circuit

Two critical parameters that vary with temperature, namely, mobility of carriers and threshold voltage, have been mentioned in (3) and (4). Notably, the junction capacitance model in BSIM 3.3.2 [16] is usually modeled as

$$C_x = C_{x0}(1 + \alpha_{C_{x0}} T),$$  \hspace{1cm} (13)

where the temperature coefficient $\alpha_{C_{x0}}$ is negative.
Referring to [14], the compensated control voltage is derived approximately as follows:

\[ V_{\text{comp}} \approx A' - C'T \]  \hspace{1cm} (14)

where \( A' \approx V_{\text{Regul18}} - V_{\text{th}0} \) with \( V_{\text{th}0} \) denoting the threshold voltage of the PMOS at temperature 0 K and \( C' \approx -(1/2) \cdot (N \cdot C_{\text{20}}/\mu C_{\text{ox}} (W/L))_{0\Omega} \).

According to (14), the slope of the compensated control voltage is negative with respect to the temperature. By using the \( V_{BE} \) of the bipolar junction transistor (BJT), the negative slope can be realized. In other words, the linear approximation in (14) must be satisfied at all process conditions. Fig. 14 shows the schematic of the process and temperature compensation circuit. The self-bias reference \( V_{\text{SB}} \) provides a temperature-independent current source. M708 acts as a \( V_{\text{th}} \) sensor, offering a threshold-sensitive voltage \( V_{\text{STH}} \), with a temperature-independent current source load (M707). The amplifier OPA2 boosts the voltage \( V_{\text{STH}} \) to \( V_{\text{TREF}} \). The compensated control voltage is generated by the transistor M709, resistor R703, and the two diode-connected p-n-p transistors Q704 and Q703. By adjusting the aspect ratio of M709 and the resistor R703, the temperature slope of the control voltage \( V_{\text{comp}} \) can be tuned. Equation (15) shows the expression of the control voltage [11]. Replacing the current \( I_{\text{comp}} \) in (15) with the expression in (16) and assuming \( \xi = (V_{\text{TREF}} - V_{\text{th}709}) - (1/(R_{703} \cdot C_{\text{ox}} (W/L)_{709})) \), (17) is then attained [14]. The \( V_{BE709,704} \) term in (17) offers the negative temperature coefficient. The proposed circuit is designed to give the required temperature slope across multiple process corners by adjusting the aspect ratio of M709 and R703. 

\[ V_{BE} \] varies with the collector current \( I_C \), i.e., \( |I_C| = I_S \cdot e^{V_{BE}/V_T} \), where \( I_S \) is the saturation current and \( V_T \) is the thermal voltage. However, \( I_C = (1/2)I_{\text{comp}} = (1/2)I_{D709} \), where \( I_{D709} \) is the drain current of M709. Therefore, \((1/2)I_{D709} = I_S \cdot e^{V_{BE}/V_T} \) is attained. Then, the equation can be rewritten as \( V_{BE} = V_T \cdot \ln(I_{D709}/2I_S) = V_T \cdot \ln(K_{T0}(W/L)_{709} \cdot (V_{\text{TREF}} - V_{\text{comp}} - V_{\text{th}709})^2) \). Therefore, the \( V_{BE} \) of the BJT can be tuned by the aspect ratio of M709.

Furthermore, \( V_{\text{comp}} \) can be written as follows:

\[ V_{\text{comp}} = I_{\text{comp}} \times R_{703} + V_{BE} \]  \hspace{1cm} (15)

Finally, by adjusting the aspect ratio of M709 and the resistor R703, the temperature slope of the control voltage \( V_{\text{comp}} \) can be tuned, i.e.,

\[ V_{\text{comp}} = V_{\text{TREF}} - [V_{\text{th}709}] - \sqrt{2I_{\text{comp}}} \mu C_{\text{ox}} (W/L)_{709} \]  \hspace{1cm} (16)

D. Differential-to-Single Converter

Fig. 15 shows the schematic of the proposed differential-to-single converter. It is composed of two out-of-phase

![Fig. 14. Schematic of the process and temperature compensation circuit.](image)

![Fig. 15. Schematic of the process differential-to-single circuit.](image)
NMOS-pair differential amplifiers, two common-source PMOS amplifiers, and an output buffer. To ensure the correct common-mode input-voltage level, a pair of symmetric load buffer is used (M801  M809). It provides amplified signals and dc bias to the PMOS common-source amplifier (M811 and M812) with a current mirror load (M813 and M814). The signals are amplified again by these two common-source amplifiers and converted into a single-ended output signal through the current mirror. Such a two-step amplification with a large bandwidth provides the same transition time for the two differential signals. Therefore, the 50% duty cycle for the output signal is attained. Notably, the output buffer provides a sufficient output driving current, i.e.,

\[
V_{\text{COMP}} = \xi + \sqrt{\xi^2 - V_{\text{TREF}}} - V_{\text{ih700}} + \frac{2V_{BE703,704}}{R_{703}/C_{\text{ce}}(W/L)_{709}}.
\]

### IV. IMPLEMENTATION AND MEASUREMENT

The proposed design is carried out by a typical 0.18 μm single-poly six-metal CMOS technology. Verified by all-PVT-corner postlayout simulations, the throughput of the Tx and the data rate of the Rx can reach 40 Mbit/s in a single channel.

![Die photograph of the proposed transceiver front-end design.](image1)

**Fig. 16.** Die photograph of the proposed transceiver front-end design.

![Waveforms of the proposed design alternately in Active state and Idle state.](image2)

**Fig. 17.** Waveforms of the proposed design alternately in Active state and Idle state.

![Implemented and measured results.](image3)

**TABLE III** MEASUREMENT OF THE TX IN DIFFERENT TEMPERATURES

<table>
<thead>
<tr>
<th>Measurement Result</th>
<th>-40°C</th>
<th>25°C</th>
<th>125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absolute value of uBus, while sending(*)</td>
<td>1528 mV</td>
<td>1398 mV</td>
<td>1169 mV</td>
</tr>
<tr>
<td>Absolute value of uBus, while Idle(*)</td>
<td>≈30 mV</td>
<td>≈30 mV</td>
<td>≈30 mV</td>
</tr>
<tr>
<td>Transmitter delay negative edge(***</td>
<td>3.189 ns</td>
<td>4.713 ns</td>
<td>4.045 ns</td>
</tr>
<tr>
<td>Transmitter delay positive edge(***</td>
<td>3.709 ns</td>
<td>6.296 ns</td>
<td>5.229 ns</td>
</tr>
<tr>
<td>Transmitter delay mismatch</td>
<td>0.52 ns</td>
<td>1.583 ns</td>
<td>1.184 ns</td>
</tr>
<tr>
<td>Fall time differential bus voltage(***</td>
<td>12.909 ns</td>
<td>6.911 ns</td>
<td>11.959 ns</td>
</tr>
<tr>
<td>Rise time differential bus voltage(***</td>
<td>13.898 ns</td>
<td>5.147 ns</td>
<td>11.733 ns</td>
</tr>
</tbody>
</table>

![Implemented and measured results.](image4)

**TABLE IV** MEASUREMENT OF THE RX IN DIFFERENT TEMPERATURES

<table>
<thead>
<tr>
<th>Measurement Result</th>
<th>-40°C</th>
<th>25°C</th>
<th>125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiver delay, negative edge(</td>
<td>22.076 ns</td>
<td>20.577 ns</td>
<td>21.033 ns</td>
</tr>
<tr>
<td>Receiver delay, positive edge(</td>
<td>19.981 ns</td>
<td>22.109 ns</td>
<td>21.914 ns</td>
</tr>
<tr>
<td>Receiver delay mismatch</td>
<td>2.0950 ns</td>
<td>1.5320 ns</td>
<td>0.8810 ns</td>
</tr>
<tr>
<td>Idle reaction time(</td>
<td>40.227 ns</td>
<td>45.007 ns</td>
<td>69.807 ns</td>
</tr>
<tr>
<td>Active reaction time(</td>
<td>46.710 ns</td>
<td>39.977 ns</td>
<td>32.622 ns</td>
</tr>
</tbody>
</table>

![Implemented and measured results.](image5)

**Fig. 16** shows the die photograph of the proposed transceiver front end on silicon. **Fig. 17** shows the waveforms of the proposed design alternately in Active state and Idle state. The signals BP and BM are modulated by the proposed Tx, and the RIdle is decoded by the proposed Rx. **Fig. 18** shows the shmoo plot of this work. The minimum operating supply voltage can be as low as 2.2 V, and the maximum throughput is more than 40 Mbit/s. The measurement results of Tx and Rx operation in different temperatures are shown in Tables III and IV. We ran the same measurement over 30 samples and got almost the same result. Last but not least, we physically connected our chip with a commercial TJA1080 and made them communicate with each other successfully. **Fig. 19** shows the waveforms of the proposed Tx. The eye size can be measured from the output waveforms, which is 47 ns (width) × 1.4 V (height).

In the FlexRay standards, all the FlexRay physical layer devices shall support the operation under automotive environmental temperature range of $-40^\circ\text{C} \leq +125^\circ\text{C}$. A reliability test over such a wide temperature range is carried out by a thermo chamber, which is used to provide these harsh temperature suites. **Fig. 20** shows the chip in the thermo chamber, and **Fig. 21** shows the thermo test between $-40^\circ\text{C} \leq +125^\circ\text{C}$. Tables V and VI show the comparison of measurement results between the FlexRay specification and our Tx/Rx design. **Table VII** shows the clock generator comparison with the prior work [14].

A TZM FlexEntry development board is used to build a FlexRay system test environment as shown in **Fig. 22**. The FlexEntry (1) generates the standard FlexRay frames to the
The proposed Rx via uBus (1). The proposed Rx transforms the differential signals into digital signals and passes it to the proposed Tx directly. At the same time, the proposed Tx generates a pair of differential signals and passes it to FlexEntry (2) via uBus (2). Notably, the measured data frames on uBus (1) and uBus (2) are exactly the same, as shown in Fig. 23. The input
signal “TxD” of FlexEntry (1) and the output signal “RxD” of FlexEntry (2) shown in Fig. 24 are also identical. Therefore, we conclude that the functions of the proposed transceiver front end is compliant with the FlexRay standards.

V. CONCLUSION

In this paper, we have proposed a transceiver front-end design which can be used in a FlexRay-based automotive system. The design is implemented in a typical TSMC 0.18 μm mixed-signal CMOS process, which justifies the integration feasibility of various ECUs. The prototype device was fabricated and measured in rigorous automotive environmental temperature conditions. Our design is proven to be compliant with the FlexRay standards.

ACKNOWLEDGMENT

The authors would like to thank CIC of NSC for their professional chip-fabrication service, and the NXP Semiconductors (Taiwan) Ltd. for their strong support of the thermo chamber equipment.

REFERENCES

Chua-Chin Wang (SM’04) was born in Taiwan in 1962. He received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1984, and the M.S. and Ph.D. degrees in electrical engineering from the State University of New York at Stony Brook, Stony Brook, in 1988 and 1992, respectively.

He has been a Full Professor with the Department of Electrical Engineering, National Sun Yat-Sen University (NSYSU), Kaohsiung, Taiwan, since 1998, where he founded the SOC group in 2005 and where he is currently also serving as the Director of Engineering Technology Research and Promotion Center. His recent research interests have included mixed-signal circuit design, low-power and high-speed circuit design, communication interfacing circuitry, and biochips.

Dr. Wang was Chair of IEEE Circuits and Systems Society (CASS), Tainan Chapter, from 2007 to 2008. He was also Chair of IEEE Solid-State Circuits Society, Tainan Chapter, from 2007 to 2008. He was the founding Councillor of IEEE NSYSU Student Branch. He is also a member of the IEEE CASS Multimedia Systems and Applications, VLSI Systems and Applications, Nanoelectronics and Giga-scale Systems (NG), and Biomedical Circuits and Systems Technical Committees. He was a Guest Editor of International Journal of Electrical Engineering and Journal of Signal Processing Systems. Currently, he is also serving as the Associate Editor of International Journal of VLSI Design, IEICE Transactions on Electronics, and Journal of Signal Processing Systems. He is IEEE CASS NG Technical Committee Chair from 2008 to 2009. He was the General Chair of 2007 VLSI/CAD Symposium.

Gang-Neng Sung was born in Taiwan in 1981. He received the B.S. degree from the Department of Computer and Communication Engineering, National Kaohsiung First University of Science and Technology, Kaohsiung, Taiwan, in 2004, and the M.S. degree from the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, in 2006, where he is currently working toward the Ph.D. degree in the Department of Electrical Engineering.

His recent research interests have included VLSI design and low-power design.

Po-Cheng Chen was born in Taiwan in 1984. He received the B.S. and M.S. degrees from the Department of Electronic Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2006 and 2008, respectively.

He is currently serving a military duty in Taiwan and is planning to work on the Ph.D. degree in the U.S. in 2010. His recent research interests have included VLSI design and low power design.

Chin-Long Wey received the Ph.D. degree in electrical engineering from Texas Tech University, Lubbock, in 1983.

He was a tenured Full Professor with the Electrical and Computer Engineering Department, Michigan State University (MSU), East Lansing, and had worked with MSU for 20 years (1983–2003). He has been with the National Central University, Jhongli, Taiwan, where he was Dean of the College of Electrical Engineering and Computer Science in 2003–2006 and where he is currently the TSMC Distinguished Chair Professor of electrical engineering. He is also the Vice President and Director General of National Chip Implementation Center, Hsinchu, Taiwan. He has published more than 200 technical journal and conference papers in these areas. His research interests include design, testing, and fault diagnosis of analog/mixed-signal VLSI circuits and systems; digital circuit design automation; defect/fault-tolerant and reliable embedded computing systems; and reliable real-time embedded computing systems.