HIGH-PSR NTSC VIDEO SYNC SEPARATOR

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ABSTRACT

This paper presents a novel NTSC video sync separator (NSS) with a high-PSR (power supply rejection) bias generation circuit (BGC) which comprises a temperature compensation circuit. The proposed BGC utilizes step-down regulators and a bandgap-based bias with cascode current control. The clamping voltages required for sync separation from an NTSC signal are generated. Detailed PSR analysis of the proposed BGC is also derived to circumvent the clamping voltage variation. The worst variation of the proposed design verified by HSPICE post-layout simulations is 5% given a [–0°C, +150°C] temperature range, and a VDD(±5 V)±10%.

Keywords: NTSC signal, clamping levels, PSR, bandgap bias, sync separation

1. INTRODUCTION

Video decoders NTSC TV products, e.g. [5], heavily rely on precise clock sources, particularly HSYNC, VSYNC, color burst, even/odd field, and back porch [3],[4]. However, these clock sources built in the TV-related products, particularly the compact hand-held or mobile TVs, will be drastically affected by the ambient temperature as well as the highly unreliable power supplies. Those mentioned clock signals existing in the NTSC composite signals might not be extracted correctly. On top of that, the generated heat will be very likely to drift the clock edges if there is no compensation mechanism. Severe damages are possibly made, e.g., fuzzy image and ghost shadow problems. Lots of work have been done to develop design methods of the NTSC sync separation circuitry. Most of the product datasheets, e.g., [6], were focused on the functionality of video signal processing. On the other hand, most of the related prior works were focused on either the bandgap designs [1], [2], or simple clock generations [5], [6], [7]. A fact which has been long ignored is that the hostile environment jeopardizes the clock locking and the voltage clamping of a video decoder [8]. Besides, the peak-to-peak amplitude of the received NTSC signals, called \( V_{pp} \), will be varied from 2V to 5V. A temperature-insensitive bias generation circuitry, thus, is required to provide stable reference voltages for clock tracking, data slicing, and noise rejection. Hence, we present a NTSC sync separator with a robust temperature-insensitive bias with high PSR (power supply rejection) comprising regulators and a reference voltage generator to resolve the problem. The worst-case variation of the bias is estimated to be less than 5%.

2. ROBUST NTSC SYNC SEPARATOR

Although EIA (Electronic Industries Alliance) has announced that the \( V_{pp} \) of the NTSC signal is set to 140 IREs [3], the amplitude of \( V_{pp} \) might still be varied from 2 ~ 5 V in hostile environments [4]. Besides, the power supply voltage is likely to be an unreliable source, particularly in those hand-held TV sets. However, several clamping voltages are needed to extract the clock information in the received NTSC signal such that the peak white, black level, clip level, and sync tips can be correctly extracted and separated. The architecture of the proposed sync separator is shown in Fig. 1. The bias voltages generated by the High-PSR Bias are fed to OSC as well as Sync Generator. OSC is in charge of generating a stable clock, which is set to 12.0 MHz in this work, to the following DSP core. On the other hand, the DAC (digital to analog converter) converts digital signals from the DSP core into a voltage which is monitored by AGC (auto-gain control) to dynamically adjust threshold voltages required in the Clamper.

2.1. High PSR Bias Generator

The performance of the entire NSS highly depends upon the sensitivity of the bias, i.e., Bias in Fig. 2. The proposed bias circuit comprising regulators, a bandgap bias (BB) with high PSR, and a resistor string, is proposed to resolve the difficulty of providing the required clamping voltages.

The temperature independent bias generated by the BB, called \( V_{ref} \), is fed into the plus input of the OP-AMP in Regulator 1 as well as the minus input of the OP-AMP in Regulator 2. Meanwhile, the BB also supplies a pair of bias voltages to control the gate drives of the cascode pair in Regulator 1 which in turn stabilizes the source current (tail current) of the built-in OP-AMP in the regulator.

A. High PSR bandgap

The bandgap reference, i.e., BB, is shown in Fig. 3. Notably, the cascode configuration comprising PM31, PM32, PM33, PM34, PM35, and PM36, and the feedback loop consisting of OP-AMP \( A_{OP} \) and NM34 are employed to resist the noise coupled with the power supply, VDD. The output impedance from \( V_{ref} \) looking into the drain of PM34 will be increased to \( \approx g_{m34}r_0 \) at the sacrifice of the "headroom" of the output swing. However, since the the
circuitry is aimed at the clamping voltage generation which is usually below 2.0 V, it will not introduce any problem. Meanwhile, A0P1 monitors the voltage difference at node V0 and V0 to control the current via NM31, which in turn stabilizes the voltage of the PMOS cascade configuration.

Assume A1 and A2 are the area of the BJTs, Q1 and Q2, respectively. The expected \( V_{ref} \) is analyzed as follows:

\[
V_{ref} = I_2 \cdot R_2 + V_{EB} = V_{EB} + L \cdot V_T \cdot \ln(K),
\]

where \( K \) is the BJT area ratio, i.e., \( A_1/A_2 \), the ratio of \( R_2/R_1 \) is assumed to be L. Hence, the bandgap reference can be determined by tuning \( L \) and \( K \).

B. PSR analysis

Since the NM31 acts as a current subtractor to control the gate drives of PM32, PM34, and PM36, we simply analyze the voltages applied to the plus and minus inputs of the OP-AMP A0P1 to find out the PSR which is defined as:

\[
PSR = \frac{V_{DD} - V_{V3}}{A_{OP1}} \approx \frac{1}{A_{OP1}} \left( \frac{I_1}{g_{mPQ1}} \right)
\]

(2)

The \( A_{OP1} \) is supposed to be an ideally large gain to avoid other side effects. Hence, we can reduce \( g_{mPQ1} \) to increase the PSR by a small \( R_1 \) and a cascade configuration.

C. Regulators

One of the most efficient approaches to avoid the effects of unstable power supplies is to employ step-down bandgap-referenced voltage regulators to supply a temperature-independent reference voltage, \( V_{ref} \), to the rest of the circuitry [7]. Since the received \( V_{pp} \) might be as low as 2.0 V, the generated \( V_{ref} \) should be no higher than this lower bound. Referring to Fig. 4, Regulator 1 is composed of PM41, PM42, NM41, R0, and OP-AMP A0P2. Notably, PM41 and PM42 are cascaded to provide a high output impedance and two stable reference voltages, \( V_{P1}, V_{P2} \) to the following OP Bias Generator (OBG). With large \( g_{mP1} \) (\( V_{ref} \) is the voltage at NODE A), the loading effect at NODE A can be reduced. Assume \( R_{m11} \) is the output impedance from OBG looking into NODE A, \( g_{mP1} \) and \( g_{mNM1} \) are the transconductances of PM41 and NM41, respectively. Since PM41 and PM42 are sized equally, the transconductance of PM42 is equal to \( g_{mP1} \). The relationship between \( \frac{\partial I_1}{\partial V_{ref}} \) and \( R_{m11} \) can be derived as:

\[
\frac{\partial I_1}{\partial V_{ref}} = R_{m11} \approx \frac{g_{mP1}}{g_{mNM1} \cdot R_{A2}}
\]

(3)

By substituting all of the parameters in the above equation and setting \( L = 10, K = 8, R_1 = 140 \Omega \), the \( V_{ref} \) is found to be approximately 1.15 V. Then, we select the most common clamping voltages for the NTSC signal given a 5 V power supply: \( V_{Vref} = 3.30 \) V, \( V_{syn} = 1.92 \) V, and \( V_{rest} = 1.69 \) V, to design the entire bias circuitry. Fig. 6 shows the layout of the designed bias.

The post-layout simulations are revealed, respectively, in Fig. 9 (HSYNC) and Fig. 10 (Vfull data), given all of the PVT corners.

3. SIMULATION AND IMPLEMENTATION

TSMC (Taiwan Semiconductor Manufacturing Company), 0.35 μm CMOS processes were adopted to carry out the proposed design. According to Eqn. (1), the following equality for a temperature-independent bandgap reference is derived.

\[
\frac{\partial V_{ref}}{\partial T} = L \cdot \ln(K) \cdot \frac{\partial V_T}{\partial T} + \frac{V_{ref}}{V_T} = 0
\]

(3)

By substituting all of the parameters in the above equation and setting \( L = 10, K = 8, R_1 = 140 \Omega \), the \( V_{ref} \) is found to be approximately 1.15 V. Then, we select the most common clamping voltages for the NTSC signal given a 5 V power supply: \( V_{Vref} = 3.30 \) V, \( V_{syn} = 1.92 \) V, and \( V_{rest} = 1.69 \) V, to design the entire bias circuitry. Fig. 8 shows the layout of the proposed design.

The post-layout simulations are revealed, respectively, in Fig. 9 (HSYNC) and Fig. 10 (Vfull data), given all of the PVT corners.

4. CONCLUSION

We have proposed a temperature-insensitive high-PSR bias generation circuitry for the sync separation of
NTSC signals in this paper. The cascade configuration as well as the regulators stabilize the clamping levels to cope with hostile receiving environments. Besides the physical implementation, the detailed PSR analysis of the proposed design is also revealed to illustrate the methodology. All of the required sync signals are successfully extracted for any later digital signal processing. The accuracy of the chip is enhanced to be less than 5 percent in all of the critical conditions.

5. REFERENCES


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Table 1: Truth table of the digital control block

![Figure 1: Architecture of the proposed NTSC sync separator](image1)

![Figure 2: The proposed high-PSR bias circuit](image2)

![Figure 3: The bandgap reference](image3)

![Figure 4: The circuitry of Regulator 1](image4)
Figure 5: The circuitry of Regulator 2

Figure 6: Architecture of the Clamper

Figure 7: Schematic of the Clamper

Figure 8: Layout of the proposed sync separator

Figure 9: HSYNC post-layout simulation result

Figure 10: V_all data post-layout simulation result