A low-cost quadrature decoder/counter interface integrated circuit for AC induction motor server control

CHUA-CHIN WANG†‡, PO-MING LEE†, YI-LONG TSENG† and CHI-FENG WU†

An AC motor server control IC which performs the quadrature decoder, counter, and bus interface function is presented in this paper. This interface IC employing TSMC 0.6 µm SPTM technology has been fabricated and tested and the results indicate that its function fully works. A novel noise filter logic is included in the design which allows reliable operations in noisy environments. It also contains a quadrature decoder such that the phase lag of an external clock and the input signal can be determined.

1. Introduction

Although advanced microprocessors with higher computing capability and execution speed are used in motor control (Tzou and Hsu 1997), certain interface integrated circuits (ICs) are still required in the build-up of control systems (Jahkonen *et al.* 1991, Hoang 1994). Figure 1 shows the H/W architecture of an AC induction motor motion controller is shown. A critical component of the motor motion controller is the decoder/counter interface between the induction motor and the DSP microprocessor. The function of this interface IC is to read the output signals delivered from motor encoder, and then decode/count into a 16-bit data which in turn is sent to the S/W controller, e.g. a digital signal processing (DSP) processor, to compute the angle of the rotor of the induction motor. Several problems need to be resolved. First, the reduction or the removal of the noise since the motor usually operates in such an imperfect environment. Second, the rotational direction of the rotor must be determined. In prior designs for such an interface (Chung 1995), a total of eight 74193s (4-bit counter), four 74373s (8-bit latch), and certain noise filter and decoder (Hewlett Packard) are needed to achieve the required functions. A large portion of board area is thus wasted. We have designed and fabricated this interface chip and tested it by Integrated Measurement System (IMS) testing equipment to verify its functions correctly. It turns out to be a simple turn-key solution for such an interface.

2. AC induction motor control interface IC

2.1. *Required functions*

2.1.1. *Digital noise filtering.* Since motors are usually operating in noisy environments which might introduce unwanted digital noise in the encoder's output owing
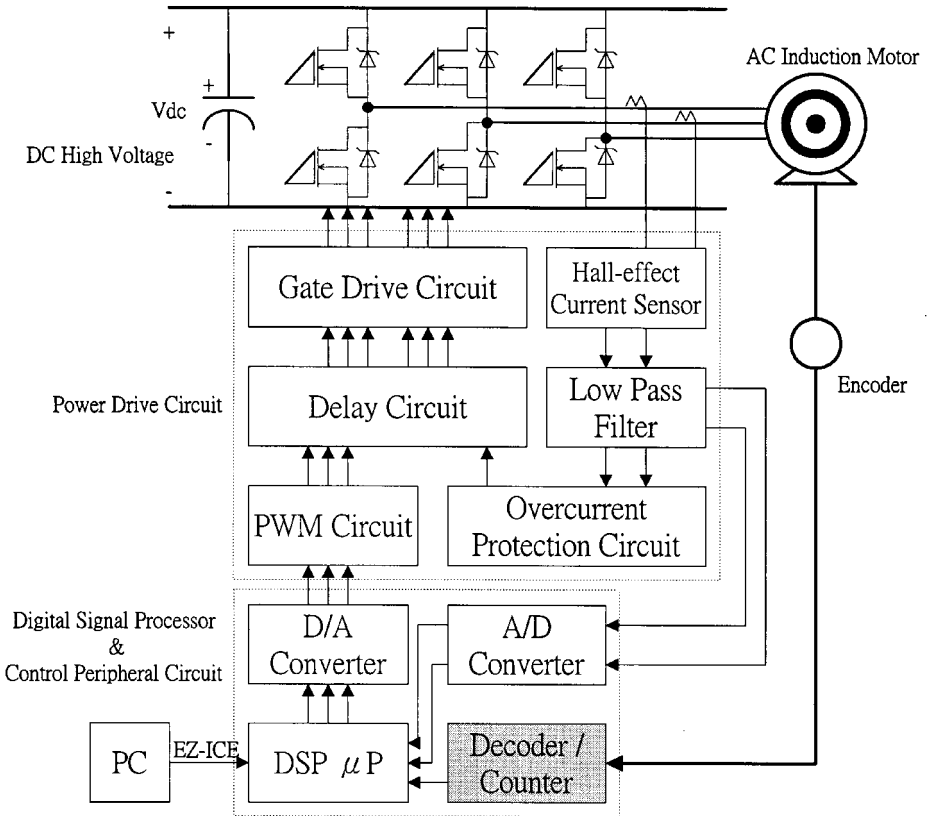
Figure 1. The H/W architecture of an AC induction motor motion control.

to coupling or vibration, a digital noise filter is responsible for rejecting noise on the incoming signals. There are two methods to improve noise rejections: Schmitt-trigger inputs and a multi-clock-cycle delay filter which can be combined to reject low-level noise and short-duration spike noise that typically occur in motor system applications.

2.1.2. *Quadrature decoder*. The rotation direction of the rotor is important for many applications. A decoder is required to decode the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four. When using an encoder for motion sensing, the user will bene-fit from higher resolution by being able to provide a better control system.

2.1.3. *Position counters*. 16-bit counters which counts on rising clock edges are needed. The system can utilize the counters in several ways. First, if the system total range is less than 16-bit range, the count represents the absolute position of the rotor. Second, if the system count is larger than 16-bit range, the count data can be used as relative or incremental position input for a system S/W computa-tion of absolute position.

2.2. *Architecture of motor control interface IC*

The general spatial relationship of motor, control circuits, and the interface IC is presented in figure 2. The entire design is named as counter10053 which consists of two counter circuits, counter10051 and counter10052. The functions of counter10051 are to receive a pair of signals sent by the encoder of motor sensor, CHA and CHB, and then quadratually decode them to determine the rotation direction of the motor. The 16-bit counter of counter10051 records the position of motor which will be passed to the motor indirect control circuit, e.g. a DSP processor. In contrast, the functions of counter10052 are employed to receive the command signals of the motor indirect control circuitry to generate the count up or count down signals to the motor direct control circuitry, e.g. a motor driver. The 16-bit counter of counter10052 then records the destination position of the motor.

Besides the mentioned two major components, the proposed interfacing circuit also contains certain glue logic, including inhibit logic, output drivers, and mode selection MUXz. The schematic of entire counter10053 is shown in figure 3.
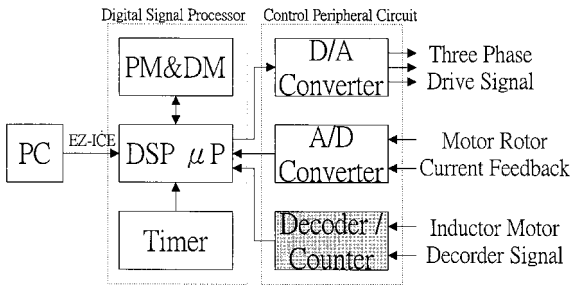

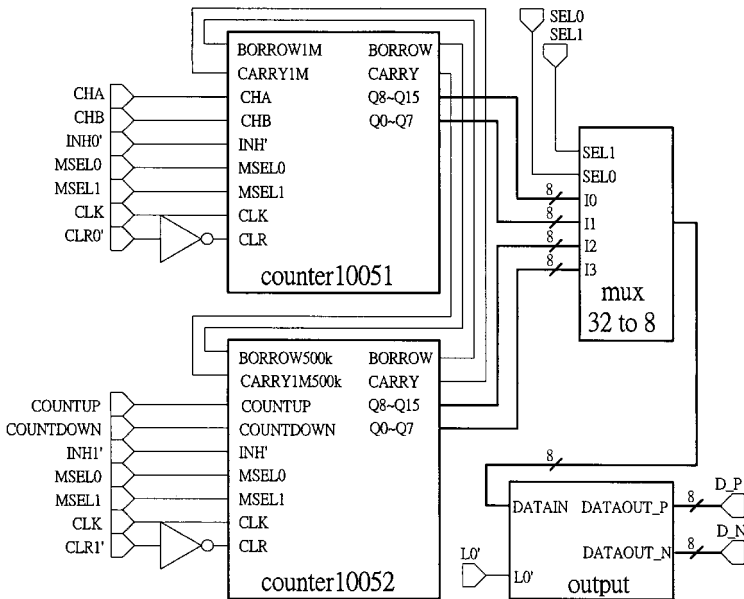Figure 2. General spatial relationship of motor, control circuit, and the interface IC.

Figure 3. The schematic of entire counter10053.

2.2.1. *Internal circuits of counter10051.* The major function of counter10051 is to quadratually decode the pair of signals from the motor encoder and record the position of motor. As shown in figure 4, it contains the following modules.

newfilter_500k.   This filters out the noise that is over 500 kHz. The upper part of figure 5 is used to divide the 10 MHz clock frequency to 5 MHz. After passing through a Schmitt trigger buffer, the input signal is cleaned up which in turn is passed to a five-bit delay filter. The filter is composed of five DFF, i.e. new_dff, a NAND, a NOR, and an XOR such that the output of the XOR is 0 if all of the five sampled data on DFFs are all 0s or all 1s. Thus, when the O/P of XOR is 0, a new signal will be generated. Otherwise, the old signal (last state) of the output will be repeated again through the feedback loop at the DATAOUT of figure 5.
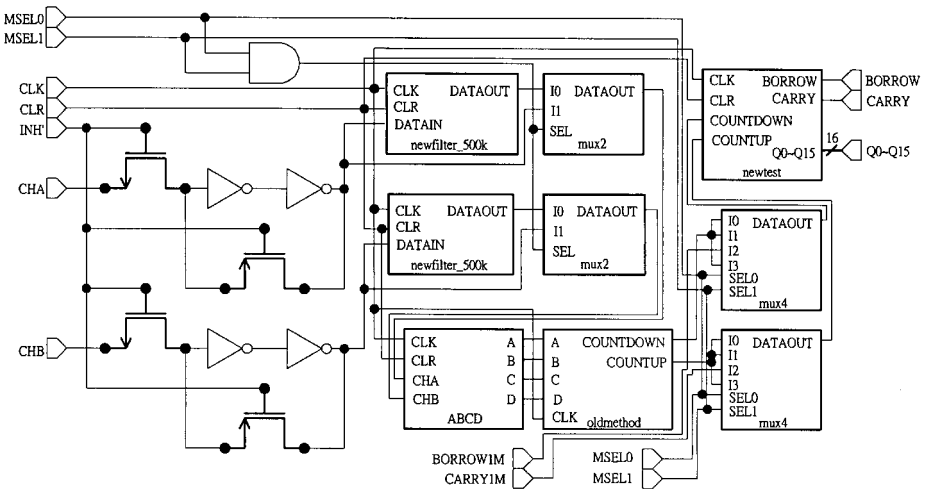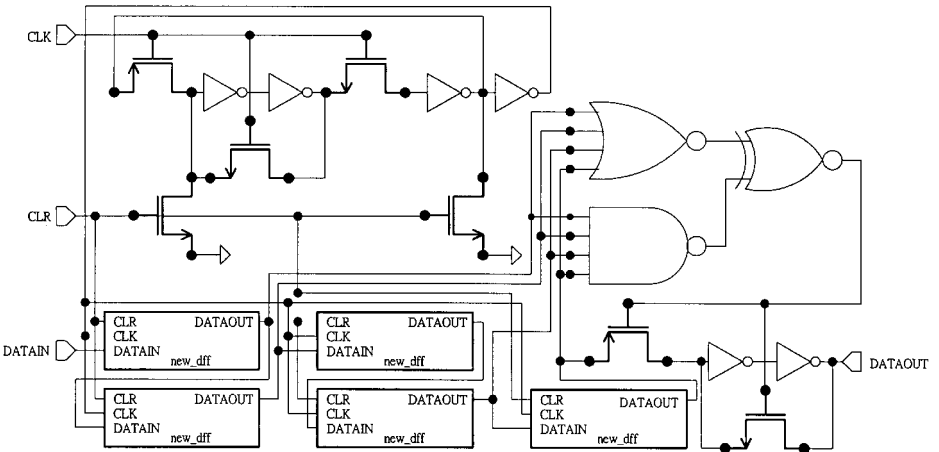

Figure 4.   The schematic of counter10051.

Figure 5.   The schematic of newfilter_500k.

ABCD.   Referring to figure 6, this circuit stores the values on CHA and CHB in two consecutive clocks, which are provided to the oldmethod block to determine the rotation direction of the motor.

oldmethod.   Based on the signals delivered from ABCD module, the circuit shown in figure 7 decodes them and provides the count up or count down information.

(1) If the sequence of (CHA CHB) is $(00) \rightarrow (01) \rightarrow (11) \rightarrow (10) \rightarrow (00)$, the motor rotates counter clockwise (i.e. reversely). The output is countdown $= 0$ and countup $= 1$

(2) If the sequence of (CHA CHB) is $(00) \rightarrow (10) \rightarrow (11) \rightarrow (01) \rightarrow (00)$, the motor rotates clockwise. The output is countdown $= 1$ and countup $= 0$.

newtest.   The module shown in figure 8 consists of 16 toggle flip-flops (TFF), two NORs, and two NANDs. In fact, it is a 16-bit positive edge-triggered counter. Notably, in order not to misjudge the signals sent from the oldmethod module during the initialization of the chip, a filter circuit is inserted at the inputs. The filter circuits locks the countup and countdown in the first two clock cycles after the reset or initialization. The 16-bit counter, thus, starts to count after two cycles.

output & output buffer.   Referring to figure 9, the high impedance output is achieved by driving the PMOS of output pad by logic 1 and the NMOS by logic 0. Thus, these
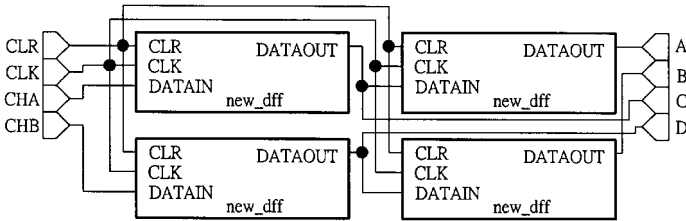

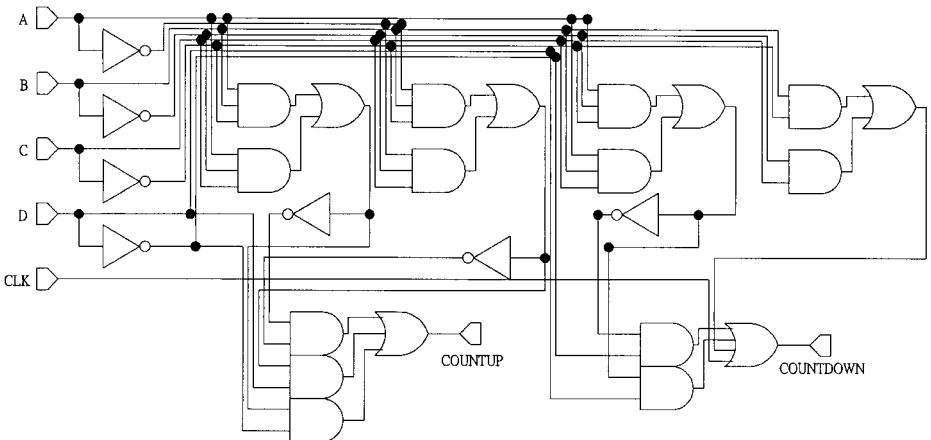Figure 6.   The schematic of ABCD.

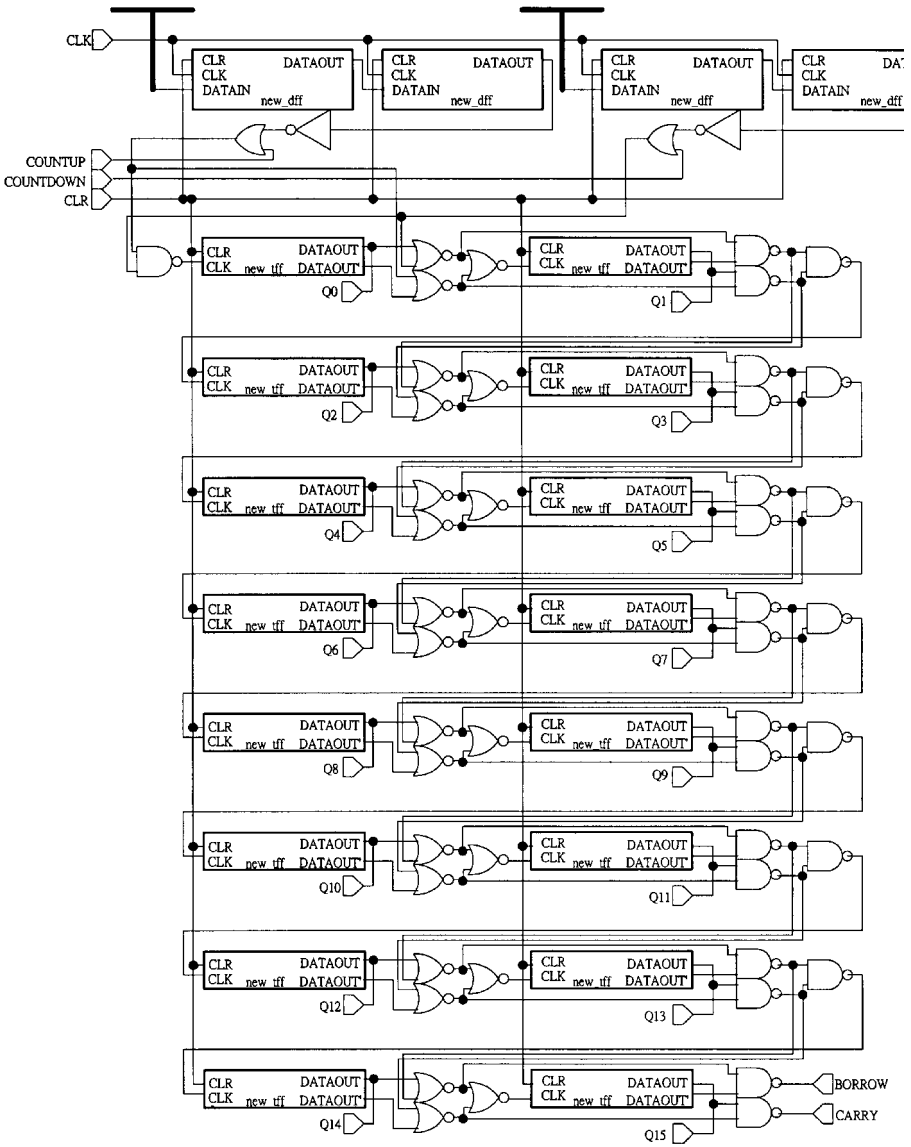

Figure 7.   The schematic of oldmethod.
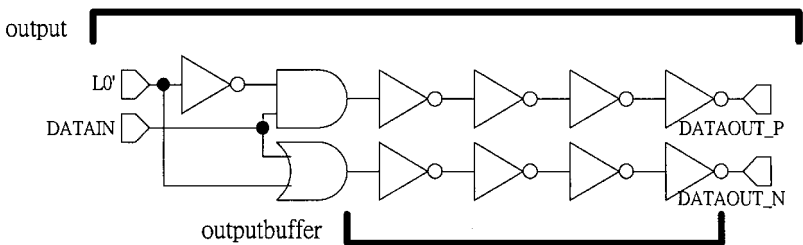
Figure 8.   The schematic of newtest.

Figure 9.   The schematic of output and outputbuffer.

driving signals have to be split before arriving at the pad. The splitting of the driving signals is controlled by $L0'$ at logic 1. Note that the L/W ratios of the output buffers are tuned to be able to drive the pre8h cell (an inverter to drive a pad) provided by CIC.
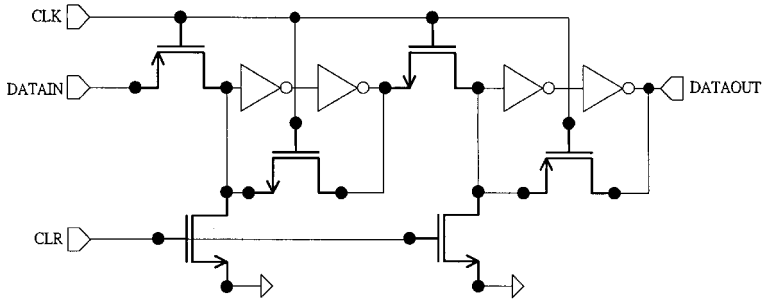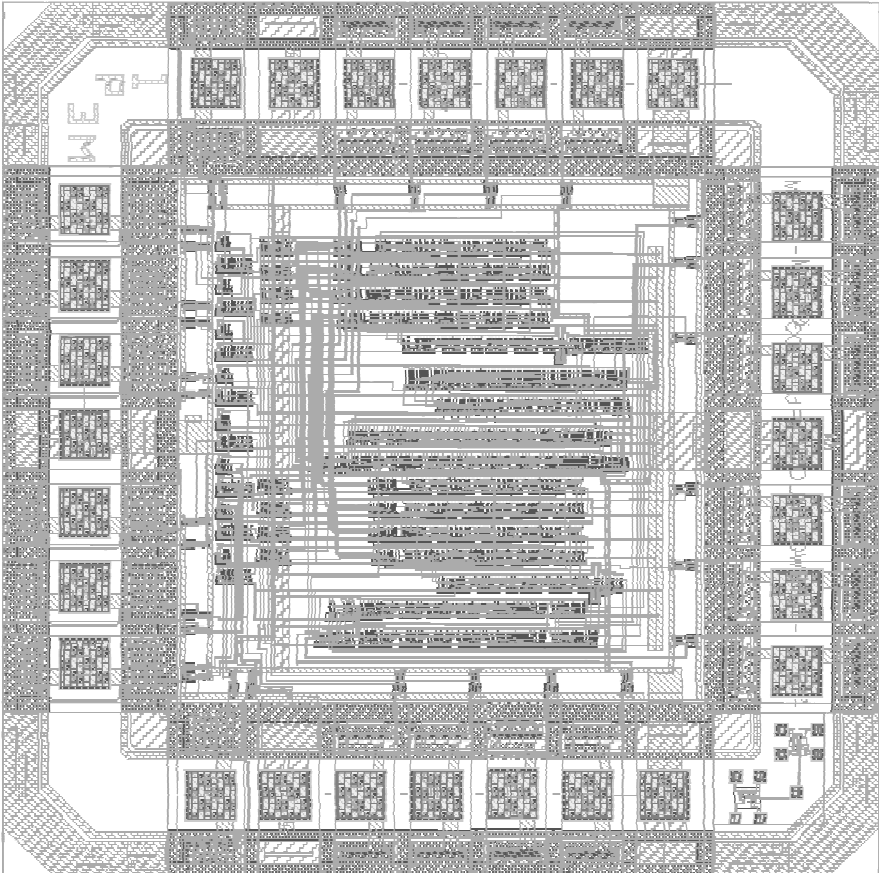

Figure 10. The schematic of new_dff.

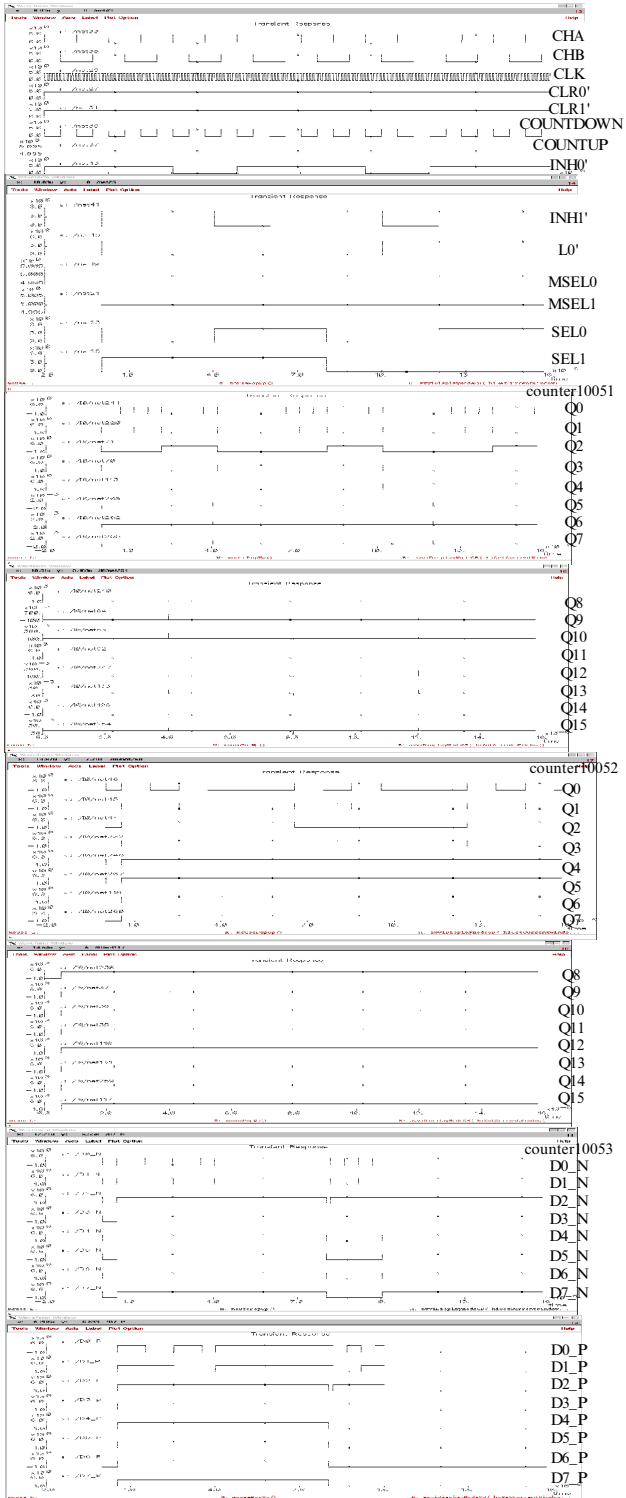Figure 11. The layout of the proposed interface IC.

Figure 12.   The HSPICE simulation results.

2.2.2. *Internal circuits of counter10052.* The design of counter10052 is similar to that of counter10051 except that filter module, newfilter_1m, is different from the filter employed in counter10051. 'newfilter_1m' is tuned to filter out any noise over 1 MHz frequency.

2.2.3. *Special cells for motor applications.* In order to consume less chip area, the DFF and TFF required in the above circuits are re-designed. We give up the static CMOS style. In contrast, we adopt a CPL-like design to develop a new_dff as shown in figure 10. A total of 14 transistors are used in the proposed new_dff, while 36 transistors are needed if a traditional DFF design is used. Similarly, a new_tff is also proposed to replace the traditional TFF.

3. HSPICE simulation and chip testing

The entire chip is custom designed with TSMC 0.6 μm SPTM technology. The layout is shown in figure 11. Before the layout was signed off, we had simulated the chip with HSPICE. The result is illustrated in figure 12 which shows that the function is correct in any case. This chip was fabricated through the help of CIC and TSMC. The IC number in CIC is T06-87B-04e. The chip area is 1.8×1.8 mm^2.

The chip in the DIP package then was tested by the IMS (Integrated Measurement System) of National Cheng-Kung University. The results are shown in figures 13 and figure 14. Figure 13 indicates that the expected vector is identical to
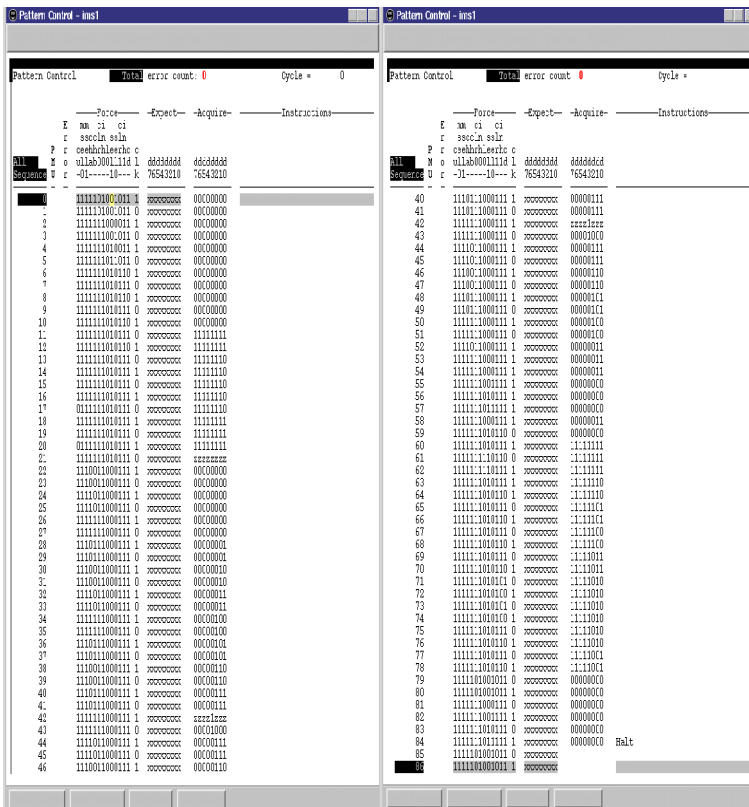

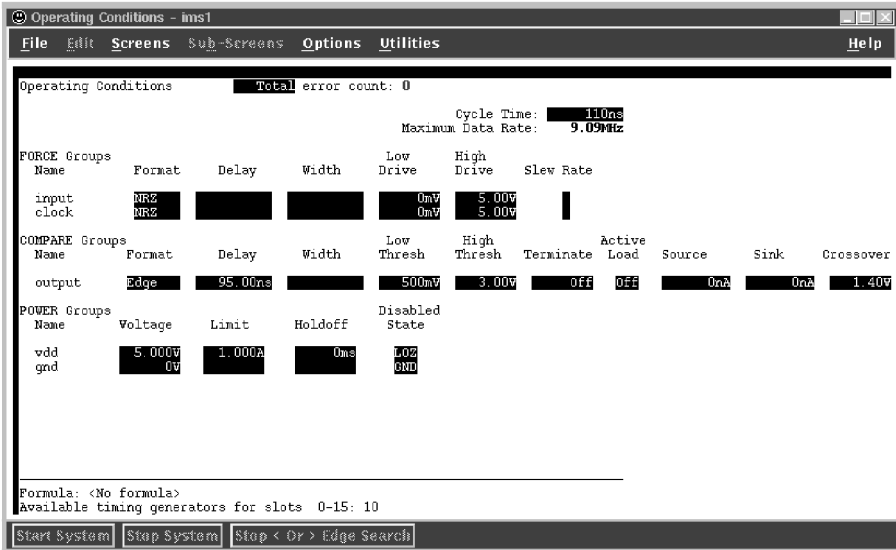Figure 13. The IMS test result of mode 4.

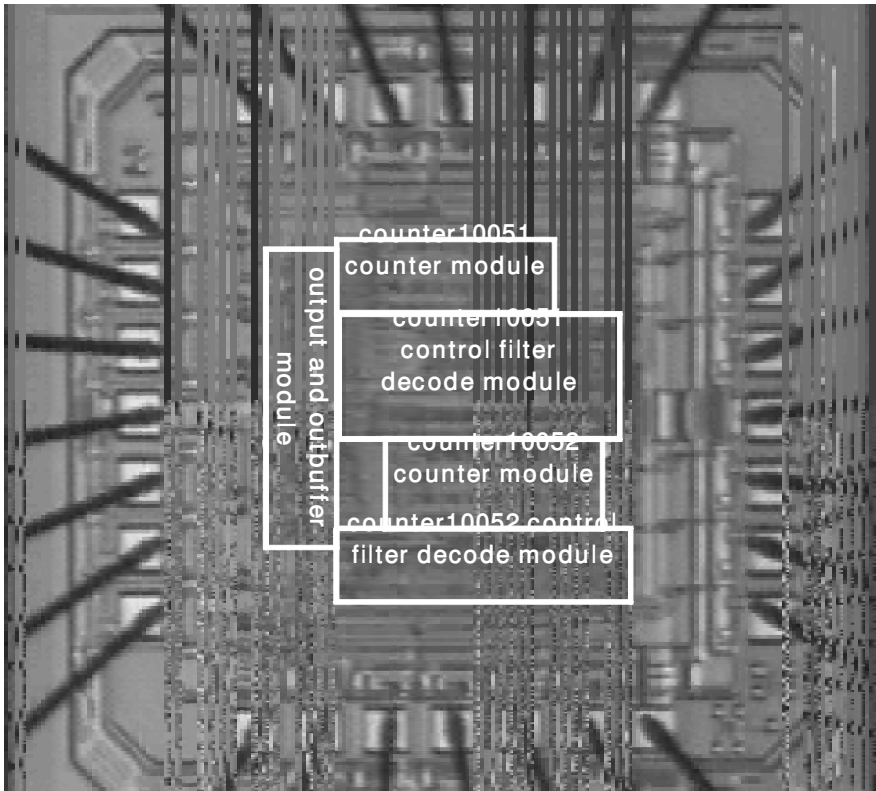Figure 14.   The IMS testing condition settings.

Figure 15.   The die photo of the proposed interface IC.

the outputs of the chip. We thus conclude that the function of the design fully works. Figure 14 shows the testing parameters. The major delay stems from the pads which introduce about 8 to 10 ns delay. However, the operating clock frequency is still adequate for normal motor operations. Figure 15 is the die photograph of the physical chip.

4. Conclusion

We propose a novel design for the motor server control interface in which the quadrature decoder, the counter, and the bus interface functions are all integrated in a chip. The areas of the proposed design turn out to be less than those of another chip which contains identical functions, HCTL-2020. The chip has also been tested by Philips Semiconductor Ltd. (Taiwan) and the results turn out to be very appealing.

References

CHUNG, C.-F., 1995, Integral variable structure model following control for vector-controlled AC induction motor drivers, M.S. thesis, Dept. of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan.

HEWLETT PACKARD, Quadrature Decoder/Counter interface ICs HCTL-2000, 2016, 2020.

HOANG, L.-H., 1994, Microprocessor and digital IC/s for motion control. *Proceedings of the IEEE,* **82**, 1140–1163.

JAHKONEN, P. P., OVASKA, S. J., VAINIO, O., and TENHUNEN, H., 1991, An integrated digital motion control unit. *IEEE Transactions on Instrumentation and Measurement,* **40**, 654–657.

PEATMAN, J. B., 1998, *Design with PIC Microcontroller* (Englewood Cliffs, NJ: Prentice Hall).

TZOU, Y.-Y., and HSU H.-J., 1997, FPGA-based SVPWM control IC for PWM inverters. *IEEE Transactions on Power Electronics,* **12**, 953–963.

WANG, C.-C., and FAN, C.-L., 1997, Digital design of discrete exponential bidirectional associative memory. *Journal of VLSI Signal Processing,* **15**, 247–257.

WANG, C.-C., and TSENG, Y.-L., 1998, A quadrature decoder/counter interface IC for AC induction motor server control. *The 9th VLSI Design/CAD Symposium*, Nantou, Taiwan, pp. 281–284.

WANG, C.-C., WU, C.-F., HWANG, R.-T., and KAO, C.-H., 1997, A low-power and high-speed dynamic PLA circuit configuration for single-clock CMOS. *1997 National Computer Symposium (NCS'97)*, vol. 2, Taichung, Taiwan, pp. C-57–C-62.