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High Fan-In Dynamic CMOS Comparators With Low Transistor Count

Chua-Chin Wang, Po-Ming Lee, Chi-Feng Wu, and Hsin-Long Wu

***Abstract*—In this brief, we propose several high fan-in dynamic CMOS comparators with low transistor count, high speed and low power. Major features of the proposed comparators are the rearrangement and reordering of transistors in the evaluation block of a dynamic cell. These comparators can be used as equality comparators, mutual comparators and zero/one detectors, which are widely used in build in self test and memory testing. Furthermore, a 64-bit fast dynamic CMOS comparator is implemented using the proposed dynamic comparator. The measured worst delay of the physical chip with pads is 12 ns.**

***Index Terms*—Dynamic comparator, high fan in, build in self test (BIST), zero/one detector, testing.**

I. Introduction

Wide bit comparators are required in modern circuits design and design for testability such as equality comparison, mutual comparison, and zero/one detection. The comparator is also a key component in the design of parallel testing, signature analyzer, and build in self test (BIST) circuits [1], etc. When a large fan in is required, serial static CMOS gates or the most common high fan-in circuit, i.e., dynamic logic, has to be used [2]–[4]. The prior comparators either need a large area overhead, have long delays, or possess high power consumption [5]. In order to resolve the difficulties introduced by the prior comparators, we propose three types of dynamic comparators to overcome the mentioned problems. The proposed circuits are simulated with 0.35-μ m CMOS 1P4M technology. Their simulation results reveal appealing outcomes. Moreover, a physical 64-bit comparator chip is implemented and fabricated on silicon using 0.5-μm 2P2M CMOS technology to verify the feasibility of the proposed circuits.

II. Equality Comparator

A. Prior Equality Comparators

1) XOR-Based Equality Comparator: An example is shown in Fig. 1(a). The advantage of this structure is that the *XOR*-based comparator can be built by using standard cells. However, if lots of inputs are required, a high fan-in NOR gate is needed. Otherwise, the high fan-in NOR gate must be composed of a tree of smaller NOR gates.

2) Pass-Gate Logic Comparator: An example is given in Fig. 1(b). Transmission gates might be used in low-power circuit designs. This structure does not draw any dc current, but it is slow for long comparators. Besides, the output current will be reduced by the long series of pass transistors if the number of inputs increases. If the output current needs to be kept at a given magnitude, buffers must be inserted in the long chain of the pass transistors.

3) Pseudo-nMOS Comparator: As shown in Fig. 1(c), another kind of the comparator was proposed. This gate draws the dc current, but it is small and fast. The major shortcoming of this circuit is that it can't provide a full-swing output voltage. One solution is to add a buffer at the output side. However, it will then increase the area of the circuit and seriously jeopardize the speed.

B. Proposed Dynamic Equality Comparator

Our proposed dynamic CMOS 4-bit equality comparator is shown in Fig. 1(d). When the clock (CLK) is low, NODE_1 is precharged to the voltage of the power supply (VDD). If $A\langle 0\rangle$ and $B\langle 0\rangle$ are both high, then N1 and N2 are ON and P1 and P2 are OFF. Thus, no current path exists during the evaluation period, and then NODE_1 will be kept high. If $A\langle 0\rangle$ is high and $B\langle 0\rangle$ is low, then N1 and P2 are on. Thus, a current path is formed between NODE_1 and ground through P2 and N1 during the evaluation period. Then NODE_1 will be pulled down. The operation for $A\langle 1\rangle B\langle 1\rangle$, $A\langle 2\rangle B\langle 2\rangle$, and $A\langle 3\rangle B\langle 3\rangle$ is similar. In short, when any pair of $A\langle i\rangle B\langle i\rangle$ is not equal, a current path will be formed and NODE_1 will be low. By contrast, if $A\langle i\rangle$ is equal to $B\langle i\rangle$ for all i, NODE_1 will keep high [6].

The pull-up time is determined only by the pull-up transistor P0, but the ground switch N0 will increase the pull-down time. Note that the ground switch may be omitted if the inputs of every pair are guaranteed at the same states during the precharge period [2], [5].

III. Mutual Comparator

By a similar thought, we can also improve the mutual comparators. The term "mutual comparator" means that all inputs must be of the same value. Mutual comparators are usually used in the parallel testing of memory where the outputs of the memory cell arrays are mutually compared.

A. Prior Mutual Comparator

Fig. 1(e) shows a typical 4-bit mutual comparator circuit. $D\langle 0\rangle$ is compared with $D\langle 1\rangle$, $D\langle 1\rangle$ is compared with $D\langle 2\rangle$, $D\langle 2\rangle$ with $D\langle 3\rangle$, and optionally $D\langle 3\rangle$ may be compared with $D\langle 0\rangle$. The output of the comparators, consisting of XOR gates, are fed into an NOR gate in order to generate the error signal [7].

B. Proposed Dynamic Mutual Comparator

Our 4-bit mutual comparator is shown in Fig. 1(f). When the CLK is low, NODE_1 is precharged to VDD. If $D\langle 0\rangle$, $D\langle 1\rangle$, $D\langle 2\rangle$, and $D\langle 3\rangle$ are all high, then N0, N1, N2, and N3 are on and P0, P1, P2, and P3 are all off. Thus, no current path exists during the evaluation period, and then NODE_1 will remain high. If $D\langle 0\rangle$, $D\langle 1\rangle$, $D\langle 2\rangle$, and $D\langle 3\rangle$ are all low, then N0, N1, N2, and N3 are off, and P0, P1, P2, and P3 are all on. Again, no current path exists during the evaluation period, either. Then, the NODE_1 will be kept high. If any input is different from the others, there will be some NMOS and some PMOS turn on

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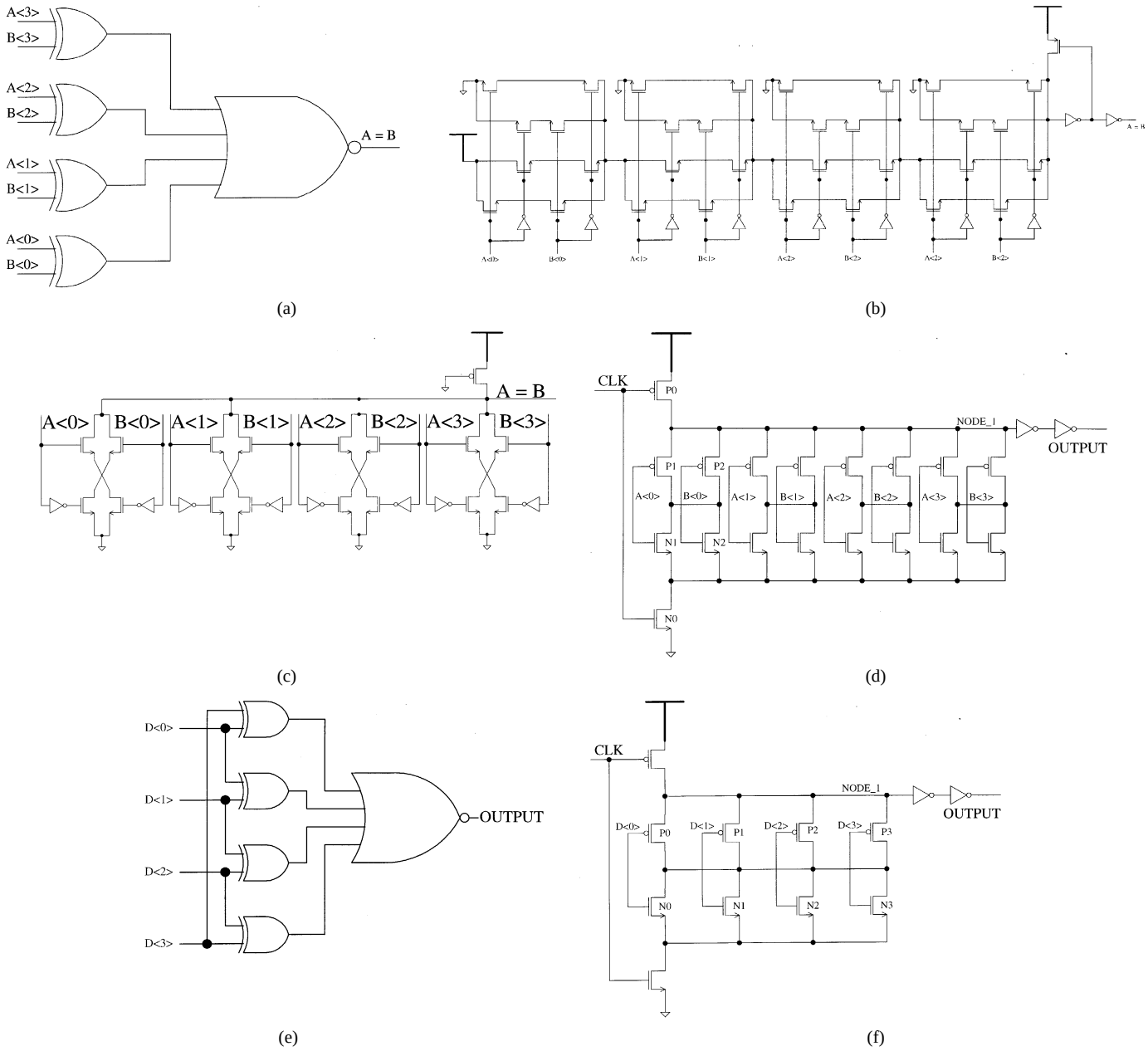

Fig. 1. Schematics of the comparators. (a) XOR-based equality comparator. (b) Pass-gate logic comparator. (c) Pseudo-nMOS based comparator. (d) Proposed 4-bit dynamic CMOS equality comparator. (e) Typical 4-bit mutual comparator. (f) Proposed 4-bit dynamic CMOS mutural comparator.

simultaneously. Consequently, a current path will be formed between NODE_1 and ground during the evaluation period. NODE_1 will then be discharged to low.

IV. Zero/One Detector

A. Prior Zero/One Detector

1) Tree Style: Constructing a tree of AND gates can detect the scenario when all inputs are "1," as shown in Fig. 1(g). The delay from input to output of this kind of design is proportional to log N, where N is the bit length of the word. Notably, if the scenario is detected when all inputs are "0," another AND tree is required.

2) Ripple Style: If the word being checked has a natural skew in the outputs, the designer might consider mimicking the delay in the "one" detector as shown in Fig. 1(h). Similar to the prior equality comparators, a small and fast zero/one detection circuit of pseudo-nMOS can be used for word length of up to 32 bits. As for large word length data, the pseudo-nMOS gate can be split into 8- or 16-bit chunks [5].

3) Deterministic Comparator: The deterministic comparator is similar to the zero/one detector. The only difference is that the deterministic comparator is used to detect whether all of the inputs have the same binary value or not instead of simply checking all 1's or all 0's. The deterministic comparator is also employed in the parallel testing of memory where the outputs of the arrays are compared against the expected data, referring to Fig. 1(i). Once again, this circuit will suffer scalability problem like the prior equality comparators. If there are a large number of inputs, a high fan-in NOR gate is needed. Otherwise, the NOR gate must be realized by a tree of smaller NOR gates.

B. Proposed Dynamic Deterministic Comparator

The proposed circuit of a 4-bit deterministic comparator is shown in Fig. 1(j). When the CLK is low, NODE_1 is precharged to VDD.

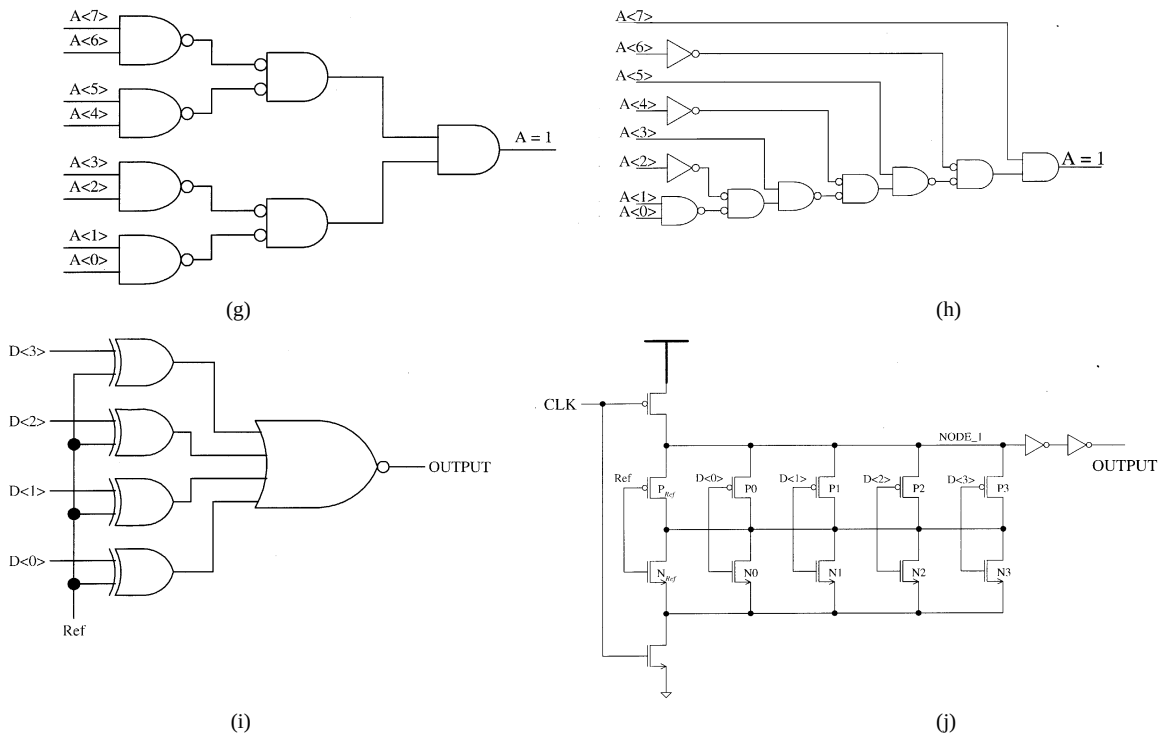

Fig. 1. *(Continued)* Schematics of the comparators. (g) Prior zero/one detector: Tree mode. (h) Prior zero/one detector: Ripple mode. (i) Prior deterministic comparator. (d) Proposed 4-bit dynamic CMOS zero.one compartor.

TABLE I
COMPARISON OF ALL COMPARATORS (SPEED, POWER DISSIPATION, AND INPUT CAPACITANCE: Cg IS THE GATE CAPACITANCE, AND Cs IS THE SOURCE CAPACITANCE)

Equality comparator	Input Capacitance	Delay (ns)	Power (W)
(10T XNOR)	2 Cgp + 2 Cgn		
(4T XNOR)	Cgp + Cgn + Csn		
(6T XOR A terminal)	2 Cgp + Cgn + Csp		
(6T XOR B terminal)	Cgp + Cgn + Csp + Csn		
Fig. 1(a)	3 Cgp + 2 Cgn + Csp + 2 Csn	0.71923	4.649×10^{-5}
Fig. 1(b)	Cgp + 3 Cgn	1.2469	4.987×10^{-5}
Fig. 1(c)	Cgp + 2 Cgn	0.081813	1.272×10^{-3}
Fig. 1(d) proposed	Cgp + Cgn	0.83817	2.806×10^{-4}
Mutual comparator	**Input Capacitance**	**Delay (ns)**	**Power (W)**
12T XOR A terminal	2 Cgp + 2 Cgn + 2 Csp + Csn		
12T XOR B terminal	2 Cgp + 2 Cgn + Csp + 2 Csn		
Fig. 1(e) Tiny XOR-based	4 Cgp + 4 Cgn + 3 Csp + 3 Csn	0.52956	1.115×10^{-4}
Fig. 1(f) proposed	Cgp + Cgn	0.3804	1.458×10^{-4}
Zero/one comparator	**Input Capacitance**	**Delay (ns)**	**Power (W)**
Fig. 1(g) (A0 A2 A4 A6 terminal)	Cgp + Cgn + Csn	0.69875	1.068×10^{-4}
Fig. 1(h) (A1 A3 A5 A7 terminal)	Cgp + Cgn + Csp	1.079	1.838×10^{-5}
Fig. 1(h) (A0 terminal)	Cgp + Cgn + Csn		
Fig. 1(h) (A1 $\sim$ A7 terminal)	Cgp + Cgn + Csp		
Fig. 1(i) Tiny XOR-based	2 Cgp + 2 Cgn + 2 Csp + Csn	0.72024	6.222×10^{-5}
Fig. 1(j) proposed	Cgp + Cgn	0.87786	2.661×10^{-4}

If "Ref," the reference data, is set high and $D\langle 0\rangle, D\langle 1\rangle, D\langle 2\rangle$, and $D\langle 3\rangle$ are all high, then $\mathrm{N_{Ref}}$, N0, N1, N2, and N3 are on while $\mathrm{P_{Ref}}$, P0, P1, P2, and P3 are all off. Thus, no current path exists during the evaluation period, and then NODE_1 will be kept high. Similarly, if Ref is low and $D\langle 0\rangle, D\langle 1\rangle, D\langle 2\rangle$, and $D\langle 3\rangle$ are all low, then $\mathrm{N_{Ref}}$, N0, N1, N2, and N3 are off and $\mathrm{P_{Ref}}$, P0, P1, P2, and P3 are all on. Thus, no current path exists during the evaluation period either, and then NODE_1 will be kept high, too. If any input is different from input Ref, there will be some NMOS and PMOS turned on simultaneously, then, a current path will be formed between NODE_1 and ground during the evaluation period. NODE_1 will then be discharged to low.

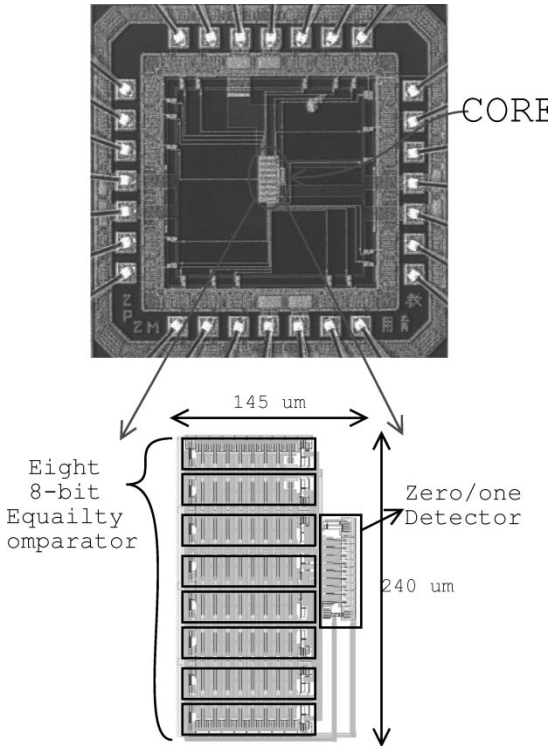

Fig. 2. Sixty-four-bit comparator chip die photo and core layout (2P2M 0.5 μm technology).

V. Simulation and Comparison

To verify the characteristics of the proposed comparators, we perform several detailed tests and comparisons. All the simulation results are given by HSPICE and TimeMill. Notably, it is not easy to prove that all the comparators are properly optimized. Hence, we employ the same 0.35-μm 1P4M CMOS technology to compare the prior comparators with the proposed comparators. Identical optimization constraints of HSPICE are used for all circuits to refine the sizes of the MOS devices.

Because of the low input capacitance provided by the dynamic logic, the speed performance is better than that of the static logic in the same category. The comparisons of input capacitance of different comparators are tabulated in Table I. Besides, there are only two stages in the proposed circuits, which make the total delay time even shorter. Thus, the speed performance is expected to be better than most of the prior designs. In order to verify the theoretical speed comparison, we physically implement and simulate each circuit using simulation results are tabulated in the right two columns of Table I. Meanwhile, since the circuits use two inverters at the output, they cannot be cascaded in a multilevel logic configuration.

VI. Physical IC Implementation

A 64-bit dynamic comparator chip is implemented to prove the feasibility of the proposed comparators. However, owing to the cost consideration, we design and fabricate this chip by using 0.5-μm 2P2M CMOS process. Nevertheless, the result is still very impressive. The entire 64-bit comparator simulated by HSPICE reveals a very short delay as tabulated in Table II. The clock rate can run up to 200 MHz with 0.01 ps rise/fall time.

The TimeMill (post-layout) simulation results indicate a 2.5-ns delay without pads as well as 4.5 ns with pads. The die photo is shown in Fig. 2 which occupies 1.8×1.8 μm^2 while the core is only 145×240 μm^2. Notably, the data are serially byte-wide I/Oed. In order to make a fair contrast, we also simulate several prior comparator designs using different logics. Note that since the adders/substractors are also often used as comparators, we also include them in the comparison. The overall results are tabulated in Table III.

TABLE II
Delays of Proposed 64-Bit Comparator

I/O path	Delay	I/O path	Delay
clk $\rightarrow$ output	2.126 ns	input $\rightarrow$ output	2.120 ns

TABLE III
Performance Comparison of Different Designs

Logic	delay	No. of transistors
64-b PLA-ANT CLA [8]	4.0 ns	8352
32-b EMODL adder [9]	2.7 ns	1537 (gates)
8-b TSPC adder (1 μm)[10]	7.5 ns	1832
All-N-logic [10]	Failed	2062
The proposed	2.5 ns	328

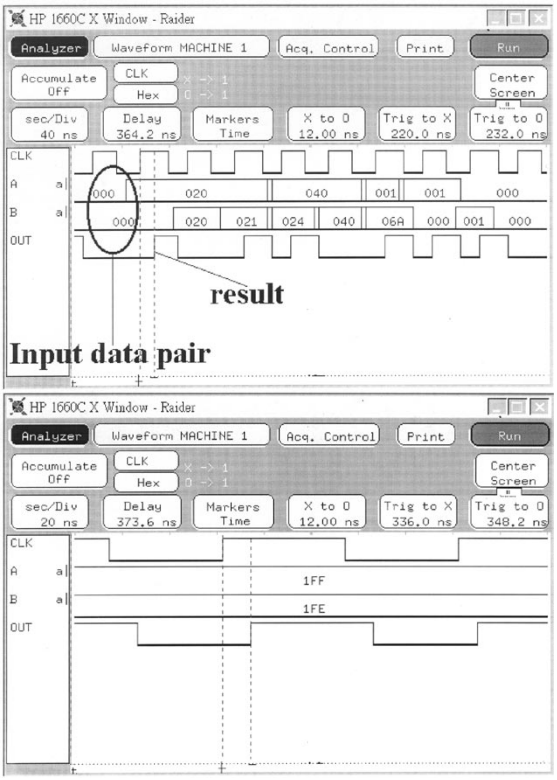

Fig. 3. Sixty-four-bit comparator test results.

This chip is tested by HP 1660 CP logic analyzer/pattern generator. When given random patterns, the outputs are all correct. The result is shown in Fig. 3(a). Besides the random test, we also measure the delay in four worst-case scenarios. The result is shown in Fig. 3(b). The maximum rise delay is 12 ns and fall delay is 16 ns, and the maximum operating frequency is 35 MHz (with pads).

It is interesting that the physical chip has a maximum delay of 16 ns while TimeMill simulation result reveals only 4.5 ns as the maximum delay. The difference between simulation and physical measurement is rather significant. In order to find out a reasonable explanation of this phenomenon, we use layout parameter extraction (LPE) tool to resimulate the delay. A netlist which includes all parasitic effects will be

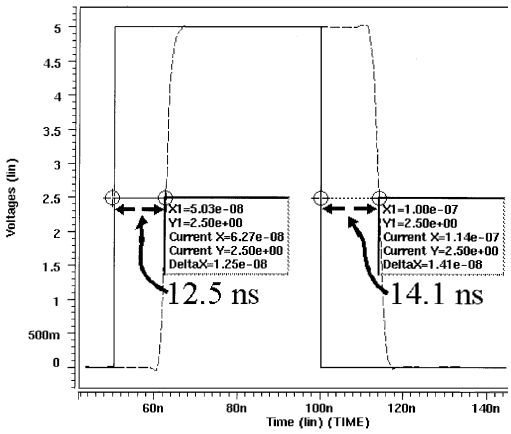

Fig. 4. Simulation result using LPE netlist.

produced. HSPICE is then used to resimulate the delay of this LPE extracted netlist. The simulation result is shown in Fig. 4. The maximum rise delay is 12.5 ns while the maximum fall delay is 14.1 ns. It gives a reasonable explanation that parasitic effects are to be blamed for the degradation of the speed performance.

VII. Conclusion

Several dynamic CMOS comparators are proposed with a number of advantages. The transistor count is much less than that of the other similar designs, and the total area size is less than that of the prior comparators. Furthermore, the noise immunity is better than the prior comparators. Although it has high fan in, the number of series transistors in the N-transistor evaluation block is two, which in turns reduce the pull down delay.

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Analysis of Three-Phase Rectifiers With Constant-Voltage Loads

Vahe Caliskan, David J. Perreault, Thomas M. Jahns, and John G. Kassakian

***Abstract*—This brief presents a quantitative analysis of the operating characteristics of three-phase diode bridge rectifiers with ac-side reactance and constant-voltage loads. We focus on the case where the ac-side currents vary continuously (continuous ac-side conduction mode). This operating mode is of particular importance in alternators and generators, for example. Simple approximate expressions are derived for the line and output current characteristics as well as the input power factor. Expressions describing the necessary operating conditions for continuous ac-side conduction are also developed. The derived analytical expressions are applied to practical examples and both simulations and experimental results are utilized to validate the analytical results. It is shown that the derived expressions are far more accurate than calculations based on traditional constant-current models.**

***Index Terms*—Alternator, commutation, converter, generator, load matching, load regulation, .**

I. Introduction

In a number of power-electronics applications, one encounters a three-phase bridge rectifier that is supplied from an inductive ac source and drives a constant-voltage load,[1] as illustrated in Fig. 1. For example, this often occurs in battery-charger/power-supply systems, such as employed in automotive and aerospace applications. The three-phase source with series inductance represents the alternator back emf and synchronous inductance, while the constant-voltage load represents the battery and system loads. A similar situation can occur when a transformer-driven rectifier is loaded with a capacitive output filter when the dc-side impedance is much lower than the ac-side impedance (as may occur during heavy- or over-load conditions). Here, the ac-side inductance is due to line, filter, and transformer leakage reactances, while the dc-side filter and load act as a constant-voltage load. In all such applications, the rectifier input and output currents are functions of the system voltage levels and the ac-side reactance.

While one might expect that analytical models for the operational characteristics of the system of Fig. 1 would be readily available in the literature, this appears not to be the case. The behavior of single-phase diode rectifier circuits with ac-side impedance and capacitive loading have been treated in the work of Schade and others [2]–[7]. Most treatments of three-phase rectifier circuits only consider operation with inductive (or constant-current) loading of the rectifier (e.g., [1], [8], and

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[1]In "constant-voltage" loads, we also include "zero-ripple-voltage" loads where the dc-side voltage (e.g., a filter capacitor voltage) may vary over time *but not substantially within an ac cycle*. In such cases, the results presented here describe the *local average* operating behavior of the system [1].