Clock-and-Data Recovery Design for LVDS Transceiver Used in LCD Panels

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***Abstract*—This brief presents the design and implementation of a clock-and-data recovery (CDR) design for low-voltage differential signals (LVDS) transceiver operations. Instead of using an oversampling scheme which requires a high-speed clock generator, we adopt an interpolation scheme which relaxes the demand of a high-speed phase-locked loop with very high precision. A dual-tracking design is proposed to precisely align both edges of a data eye. Hence, the center of a data eye can be optimally sampled. A standard foundry 0.25-μm 1P5M CMOS technology is used to realize the proposed dual-tracking CDR for 7×100 (bit-MHz) LVDS signaling. The post-layout-extracted simulation reveals that the worst-case jitter of the sampling clocks is less than 450 ps (peak-to-peak) and 250 ps (rms) at all process corners.**

***Index Terms*—Clock-and-data recovery (CDR), dual tracking, eye diagram, low-voltage differential signals (LVDS) signaling, phase interpolation.**

I. Introduction

DATA communication with liquid crystal display (LCD) panels is achieved through asynchronous low-voltage differential signals (LVDS) serial links because it has characteristics of low-voltage swing, low power, high data rate, and differential technology. Designing a clock-and-data recovery (CDR) module in the receiver is challenging because the data received in the system are asynchronous and noisy. Regarding the CDR designs for LVDS signaling, there were two major design schemes : oversampling, and interpolation, [1], [2]. One method of the oversampling scheme uses a voltage-controlled oscillator (VCO)-based phase-locked loop PLL to generate a much higher sampling frequency than that of the LVDS signals themselves [5]. Several oversampling schemes then use the phase interpolation scheme to generate $3\times$-oversampling clocks [3], [6]. We adopt the phase interpolation design scheme to design the CDR for LVDS signaling circuitry which requires a PLL possessing the same output frequency as the data rate. Instead of assuming symmetric jitter environment and tracking only one side of the eye as in prior works [7], we use 14-phase clocks to trace and track two edges of an eye, called dual-tracking, to align data sampling at the middle of the eye. Hence, the detection of the data is ensured to be optimal and the bit-error rate (BER) is drastically reduced. The proposed CDR is fully compliant with the IEEE STD. 1596.3. A typical 0.25-μm 1P5M CMOS technology is used to realize the proposed CDR. The post-layout-extracted simulation reveals that the jitter is 450 ps (peak-to-peak) and 250 ps (rms), while the BER is less than 10^{-13}.

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II. Dual-Tracking CDR Design for LVDS Signaling

A very bold assumption in prior CDRs is that the jitter environment is symmetrical all the time. Hence, the sampling is naturally assumed to be aligned at the middle of the eye in these CDR designs. We, however, observe that most of the jitter environment are not really symmetrical in the LVDS data transmission due to the random jitters occurring at both sides of the eyes. It is then required to track two adjacent eyes such that the middle of the eyes can be correctly positioned. The architecture of the proposed dual-tracking CDR is shown in Fig. 1. The entire CDR data processing flow can be illustrated by Fig. 2.

A. CDR System Architecture

1) BLOCK-1 (PLL): Referring to the multi-phase PLL in Fig. 1, the PLL receives an external 20- to 100-MHz clock and generates a bank of clocks with seven different phases, respectively, to sample seven data in one PLL cycle, as shown in Fig. 2. We use a differential 7-stage voltage-controlled ring oscillator to construct the PLL.

2) BLOCK-2 [Eye Edge Finder (EEF)]: The data edge generator (DEG) generates pulses aligning to the edges of the incoming bit stream. We define the pulsewidth of a single cycle (mark level) as the right eye and the ground portion (space level) as the left eye in this brief without any loss of robustness. The right-eye phase early/late detector (PELD-R) generates RW0 to RW5 and their complements depending on the right-eye samples of the current edge compared with the previously detected edge, which was produced at the output of the right-eye phase interpolator (PI-R) and its associative right-eye differential-to-single signal converter (DSC-R). On the other hand, the left-eye PELD (PELD-L), left-eye PI (PI-L), and left-eye DSC (DSC-L) executes the same function to the left eye.

3) BLOCK-3 [Eye Center Generator (ECG)]: Referring to Fig. 1, the possibly locked left and right edges of the eye are, respectively, denoted by LW0 to LW5 and their complements, and RW0 to RW5 and their complements. These signals are fed into center PI (CPI) which generates a pair of control signals, i.e., BP0 and BN0, to drive the following 7-stage voltage-controlled delay loop (VCDL). The VCDL, thus, generates seven sampling pulses aligning the individual centers of the eyes.

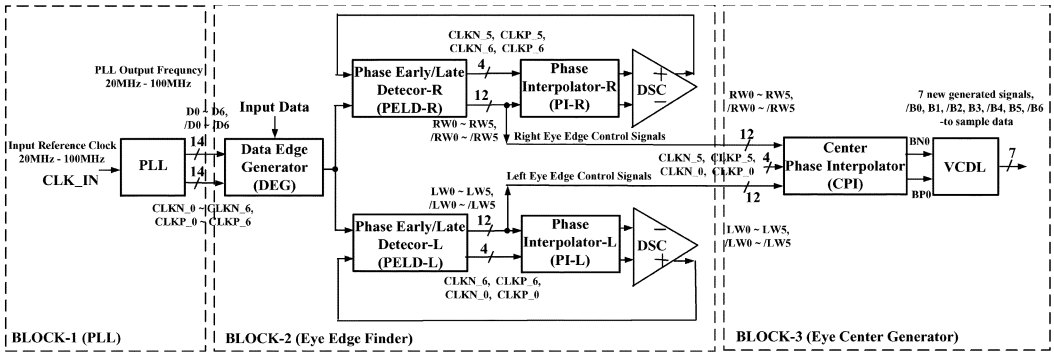

Fig. 1. Architecture of the proposed dual-tracking CDR.

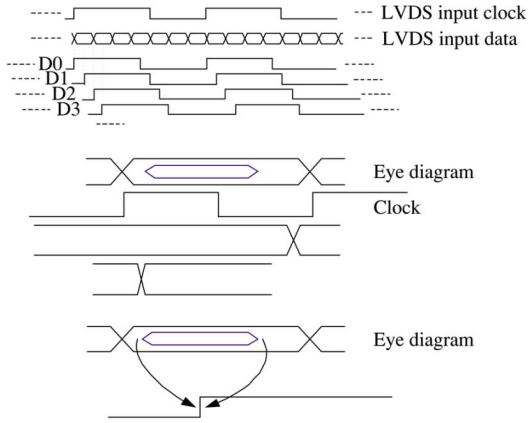

Fig. 2. Data flow of the proposed dual-tracking CDR.

B. Data Processing Flow

A total of seven data bits are transferred in one LVDS clock cycles. Thus, the PLL in BLOCK-1 locks the LVDS clock and generates 1×7 clocks with the same frequency and equally spaced phases. The edge-finding of the eye's right edge is summarized as follows.

R1). PELD-R samples the current edge and compares with the previous detected edge which was produced at the output of PI-R and its associative DSC-R. If the current edge is found to be at the left side of the previously detected edge, then the right edge of the eye is set to be the last detected edge.

R2). On the contrary, if the current edge is found to be at the right of the previously detected edge, we need to compare the current edge with the output of PI-R. If the current edge lags (that is, falls at the right of the PI-R's output), the right edge of the eye is "locked" by a DFF which is the DFF-R1 in Fig. 3 which, in turn, disables the advancing of the 6-bit right-eye shift register (SR-R). If the current edge leads the PI-R's output and the SR-R is not locked, the SR-R advances by 1 bit to move the next PI-R's output toward the center of the eye.

R3). The locked right edge of the eye can only be released by the next detected edge appearing at the left of the PI-R's output.

The edge-finding of the eye's left eye is similar to that for the right edge. As soon as both edges of the eyes are detected, the center of the eye, which is the optimal sampling edge, will be determined by the ECG.

C. Circuit Implementation

1) PLL in BLOCK-1: Referring to Fig. 4, the PLL comprises a bias generator, a replica bias, a charge pump (CP) containing two individual charge pumps which controls the voltages, VP and VN, fed into the seven voltage-controlled delay cells. The seven voltage-controlled delay cells constitute a VCO. The differential output pair of each delay cells, namely CLKN_i and CLKP_i, where $i = 0, 1, \ldots, 6$, are, respectively, through seven DSCs converted into a pair of single-ended voltage pulse trains, i.e., Di and /Di, where $i = 0, 1, \ldots, 6$. Notably, Di and /Di are complementary to each other.

2) EEF in BLOCK-2: The EEF is composed of the reset control circuit, DEG, the right-edge detector consisting of PELD-R, SR-R, PI-R, and DSC-R, and the left-edge detector including PELD-L, SR-L, PI-L, and DSC-L, as shown in Fig. 3. SR-R and SR-L are typical SRs. What is left to be addressed is the PI-R, PI-L, and the reset control circuit.

a) PI : All of the PI-R, PI-L, and CPI in BLOCK-3 are identical. Fig. 5 shows the schematic of the PI. CLK1 and /CLK1, CLK2 and /CLK2 are two pairs of differential signals, while Wi and $/Wi$, where $i = 0, \ldots, 11$, are current control signals. More Wi's are 1's, a larger current will be induced via the VP-controlled current sources and the VN-controlled current sinks. Hence, the transition at the OUT and /OUT will be faster. For instance, CLK1 and /CLK1, CLK2 and /CLK2 of PI-L are, respectively, coupled to CLKN_6 and CLKP_6, CLKP_0 and CLKN_0. Meanwhile, the Wi's are coupled to the outputs of the 6-bit SR-L as the lower right part of Fig. 3. Fig. 6 shows the simulation results that curve A, B, C, D, E, respectively, denotes the phase slicing given 5, 4, 3, 2, 1, of 1's in the SR-L between curve $\langle 0 \rangle$ and $\langle 1 \rangle$. It should be noted that curve $\langle 0 \rangle, \langle 1 \rangle, \langle 2 \rangle, \langle 3 \rangle$, etc., are the generated CLKP_0, CLKP_1, CLKP_2, CLKP_3, etc., of the PLL. Hence, the duration between CLKP_0 and CLKP_1 can be divided into six phase intervals, so are the rest of the generated clocks.

b) Reset Control Circuit: To avoid a possibility that an edge of incoming data completely falls outside the range of the eye which will lead to at least one of the PIs not aligning corresponding edge with the data edge, a reset control circuit comprising a 4-bit counter as shown in Fig. 3 is required to resolve this problem. After counting 15 cycles and PI-R or PI-L can not spot the correct

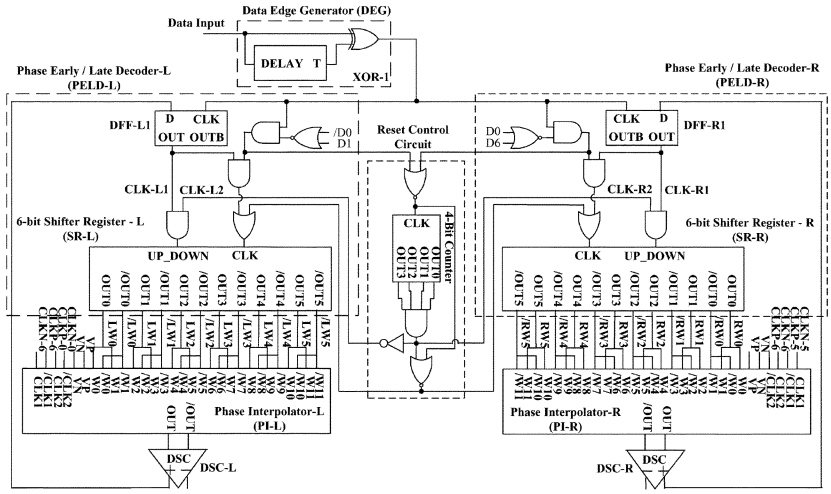

Fig. 3. BLOCK-2.

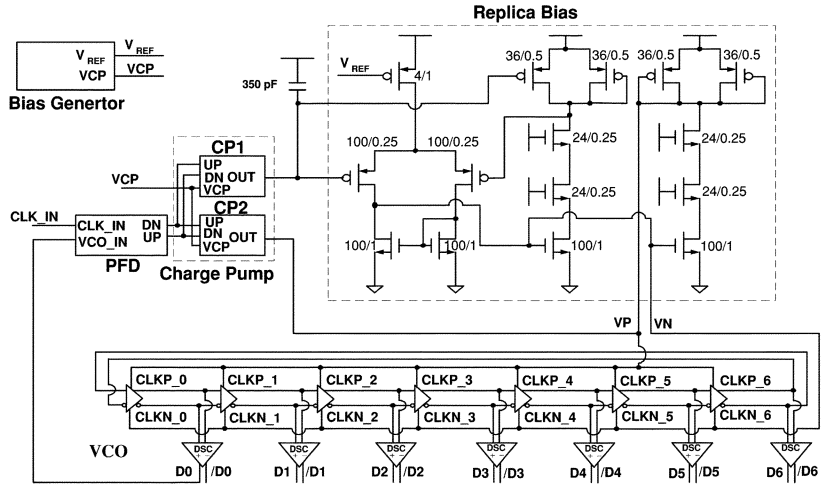

Fig. 4. BLOCK-1.

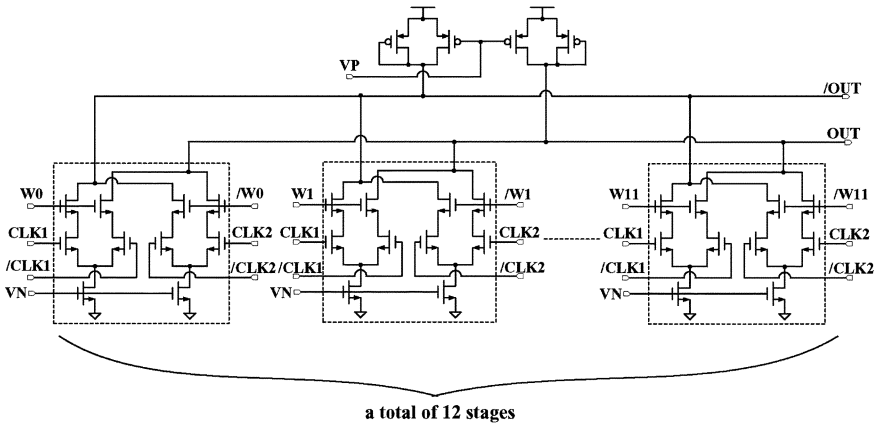

Fig. 5. Schematic of a PI.

position of the current, a "1" and a "0" are generated and propagated to the UP_DOWN pin of SR-R and SR-L, respectively, via CLK-R2 and CLK-L2. The former forces the PI-R to shift its range to the right, i.e., widen its searching range. On the other hand, the "0" at the UP_DOWN of SR-L makes the PI-L shift its range to the left. The entire scenario is shown in Fig. 7.

3) VCDL in BLOCK-3: Referring to Fig. 8, the CPI receives a total of 24 signals delivered by SR-R and SR-L, including RWi and $/RWi$, and LWi and $/LWi$, where $i = 0, \ldots, 5$. They denotes where the right and left edges of the eye are positioned. The difference between CPI and PI-R, PI-L is that CPI is used to generate sampling pulses. Thus, its input clocks must

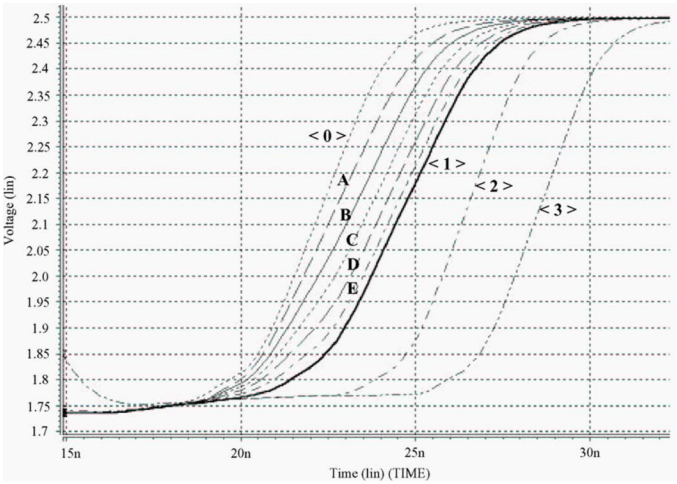

Fig. 6. Phase interpolation between two clock edges.

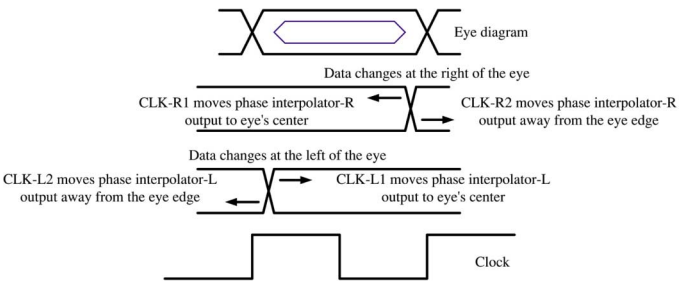

Fig. 7. Dual-tracking operations.

be two phase pitches apart, e.g., using CLKP_5 and CLKN_5, CLKP_0 and CLKN_0, not like those CLKN_6 and CLKP_6, CLKP_0 and CLKN_0 used in PI-L. A voltage-controlled delay line (VCDL) which is identical to the VCO in the PLL is included. Notably, a dummy cell should be added at the end of the VCDL to equalize the load at the output of each stage. A total of seven sampling pulses at the output of the seven DSCs are generated, /B0, B1, /B2, B3, /B4, B5, and /B6.

III. Simulation and Implementation

The proposed CDR is implemented in Taiwan Semiconductor Manufacturing Company (TSMC) 0.25-μm 1P5M CMOS technology to verify the performance. Notably, all of the process corners : [0 °C, +100°C], (SS, SF, TT, FS, FF) models, and $V_{\rm DD} \pm 10\%$, are simulated. Besides, in order to observe the limited PI resolution and PI differential nonlinearity, Monte Carlo analysis is carried out. Figs. 9 and 10 show the Monte Carlo simulation results for PIs $(\text{iteration} = 30 \text{ times})$. The nonlinearity between every two adjacent interpolator signals' space is demonstrated. For example, the space between $\langle 0 \rangle$ and A consumes nearly 28% of all of the interval between $\langle 0 \rangle$ and $\langle 1 \rangle$. On the other hand, the minimum spacing is between E and $\langle 1 \rangle$, which is roughly 6.5%. The layout of the proposed CDR is shown in Fig. 11. Fig. 12 shows the output waveforms of the post-layout-extracted simulations. On top of Fig. 12, it is a normal data bit and the corresponding sampling edge given a 100 MHz data rate. By contrast, if a data is delayed or interfered and the edge of incoming data completely falls outside the range

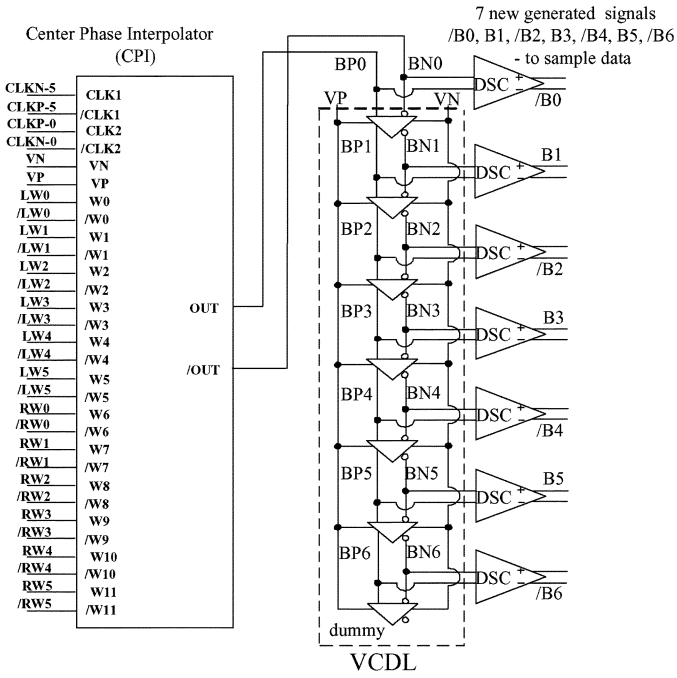

Fig. 8. BLOCK-3.

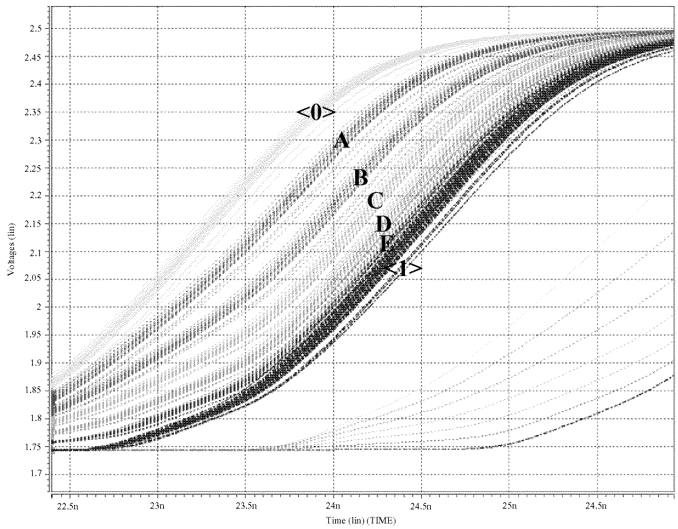

Fig. 9. Monte Carlo simulation result for the interpolator signals.

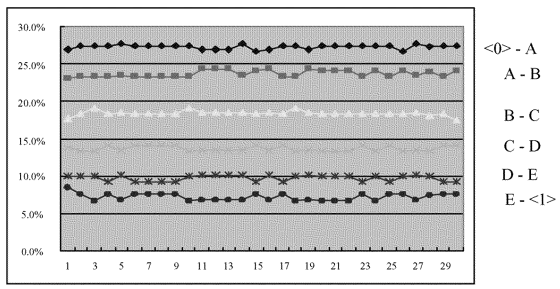

Fig. 10. Monte Carlo simulation result of spacing between every two adjacent interpolator signals.

of the eye, the 4-bit counter will generate CLK-R2 which controls a logic 0 shift left through SR-R such that the eye's right

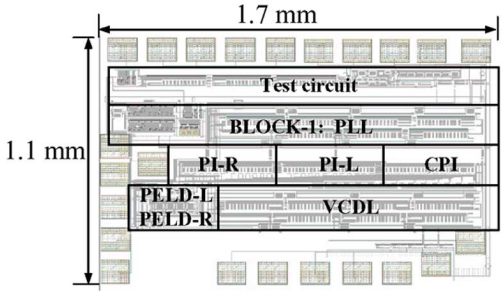

Fig. 11. Layout of the proposed dual-tracking CDR.

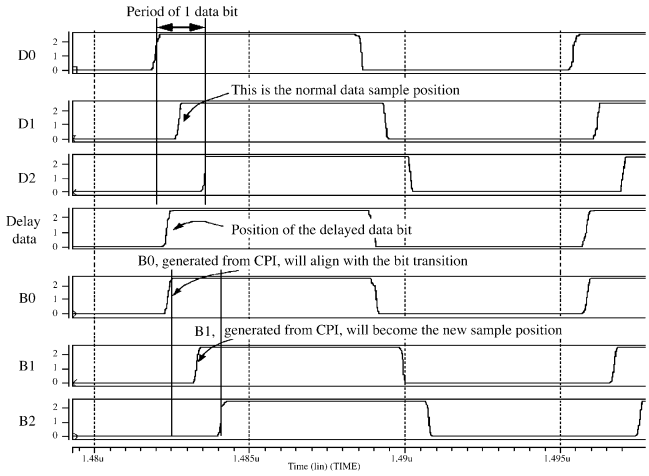

Fig. 12. Post-layout-extracted simulations of the proposed dual-tracking CDR.

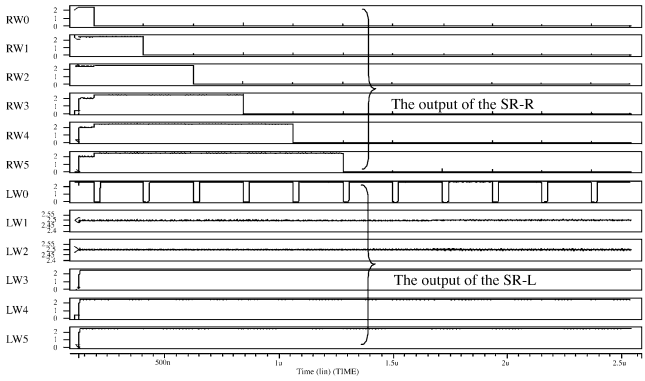

Fig. 13. Simulation result of the SR-R.

edge expand to outer until all outputs of the SR-R are logic 0. Finally, the CPI will track the edge of the delayed data. The simulation outputs of the SR-R is shown in Fig. 13. In the bottom half of Fig. 12, the B0 generated at BLOCK-3 will align with the edge of the delayed data bit. Then, B1 becomes the new sampling pulse to latch the data correctly. The characteristics of the proposed dual-tracking CDR is summarized in Table I. It is fully compliant with the requirements of IEEE STD. 1596.3.

TABLE I
CHARACTERISTICS OF THE PROPOSED DUAL-TRACKING CDR

	STD 1596.3	Our Design
VDD	2.2 ∼ 2.8 V	2.2 ∼ 2.8 V
input clock	25 ∼ 100 MHz	25 ∼ 100 MHz
max. current	20 mA	20 mA
jitter (p-to-p)	N/A	450 ps
jitter (rms)	N/A	250 ps
area	N/A	1.7×1.1 mm^2

IV. CONCLUSION

We propose a novel dual-tracking CDR design by detecting both edge of an eye such that the center of the eye can be precisely sampled. The proposed CDR is immune to the asymmetry of data eyes. Besides, the phase interpolation design scheme is adopted to avoid the necessity of a very high sampling clock to relax the jitter accumulation problem.

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