



## A low-power 2.45 GHz WPAN modulator/demodulator

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### ABSTRACT

This paper presents the architecture as well as the circuit implementation of a wireless personal area networks (WPAN) modulator/demodulator using 2.45 GHz band compliant with the physical layer standard of IEEE 802.15.4. A noncoherent demodulation scheme is employed to resolve the complexity and power dissipation problem, where a phase-shift down sampling method is adopted to detect the maximum phase accumulation which is the location of the correct data. A prototypical system on silicon with core area of 0.39 mm<sup>2</sup> has been realized by using 0.18 μm CMOS process. The packet error rate (PER) is measured to be < 1% given the SNR of 9 dB. The total power consumption is merely 1.37 mW (included Tx and Rx) given a 8.0 MHz system clock.

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### 1. Introduction

Wireless personal area network (WPAN) standard [1] is a wireless standard aiming at a low data rate, low cost, and low power wireless data transmission. The major applications of WPAN are focused on short-range wireless sensor networks, such as industry control, building automation, [2–5], ecology monitoring, and personal healthcare. Particularly, WPAN is an excellent solution for biotelemetry technique [6–9]. Regarding the biotelemetry applications, several important issues should be addressed, including the modulation scheme of the wireless link and the power consumption of the device. WPAN possesses edge of the low cost and low power consumption in addition to a better signal quality due to the adopted modulation scheme compared with the conventional AM (amplitude modulation) based biotelemetry. The WPAN can also be integrated with the existing network infrastructures, such as wireless local area network (WLAN) and general packet radio service (GPRS), to construct a comprehensive network for medical assistance as shown in the scenario in Fig. 1.

The WPAN uses the ISM bands at 868 MHz (European), 915 MHz (USA), or 2.45 GHz (International). It adopts the PSK (phase shift keying)-based modulation scheme. The WPAN standard specifies that 868/915 MHz band employs the BPSK (binary phase shift keying) modulation, while the O-QPSK (offset-quadrature phase shift keying) modulation is used in the 2.45 GHz

band. Although the bandwidth efficiency of the QPSK is better than that of O-QPSK, the large phase changes ( $\pm 180^\circ$ ) makes QPSK requires a linear power amplifier (PA) to maintain the signal spectrum within the desired band. Hence, the O-QPSK, which requires a less phase step ( $\pm 90^\circ$ ), is preferable in physical implementations. Besides, the WPAN adopts the direct sequence spread spectrum (DSSS) technique to improve performance and the capability to cope with the multipath problem. At the transmitter end, four bits are packed into one symbol, which is further spread as a 16-chip sequence in the 868/915 MHz band or a 32-chip sequence in the 2.45 GHz band, respectively. Prior modulator/demodulator designs for 868/915 MHz, e.g., [10], obviously cannot be applied to 2.45 GHz WPAN Tx/Rx due to different modulation schemes. Besides, since O-QPSK is a more complicated modulation scheme, low power design consideration is particularly needed to meet the low power dissipation requirement. The detailed specifications of the data rate and the corresponding frequency band are summarized in Table 1.

This paper presents the architecture as well as the hardware implementation of modulator/demodulator for a WPAN using the 2.45 GHz band as an efficient solution of personal medical assistance [11]. Particularly, a phase-shift downsampling method is used for the noncoherent scheme in the demodulator to find the maximum phase accumulation, to detect the location of the correct data [12].

### 2. WPAN transceiver for 2.45 GHz band

Fig. 2 depicts the structure of the WPAN physical layer protocol data unit (PPDU) packet compliant with IEEE 802.15.4.

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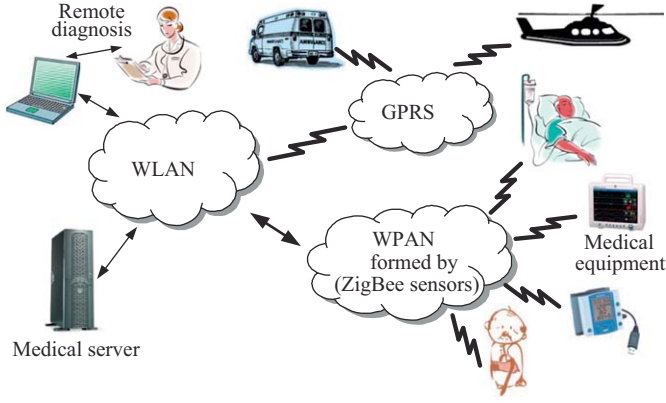


Fig. 1. Applications of WPAN in personal medical assistance.

Table 1 Specifications of data rate and frequency band.

Freq. band	868/915 MHz	2.4 GHz
Bit rate (Kb/s)	20/40	250
Symbol rate (Kchip/s)	20/40	62.5
Chip rate	300/600	2000
Modulation	BPSK	O-QPSK

Octets : 4	1	1	variable
Preamble	Start of frame delimiter	Frame length (7 bits)	Reserved (1 bit)
Synchronization header	PHY header	PHY payload	PSDU

Fig. 2. PPDU packet format.

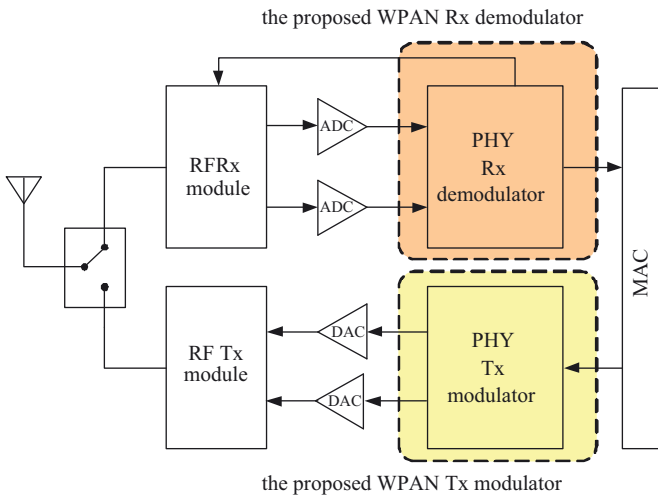


Fig. 3. Block diagram of a WPAN transceiver for 2.45 GHz band.

The preamble field containing 32 bits “0” is for the packet detection and the synchronization in the receiver. The start of frame delimiter (SFD) field denotes the start of the packet data, which is “11100101”. The frame length field indicates the number of octets of the physical layer service data unit (PSDU). The PSDU conveys the payload of the packet.

Fig. 3 shows the block diagram of a WPAN transceiver. The RF signal is down-converted to a baseband signal by the RF receiver

(Rx) and quantized by the analog-to-digital converters (ADC). These digital signals are sent to the MAC after the digital demodulation performed by the proposed Rx. The PSDU from MAC is modulated by the proposed transmitter (Tx), and the resultant PPDU packet is transmitted by the RF Tx. The details of Rx’s demodulator and Tx’s modulator are described in the following text.

### 2.1. Modulator of WPAN Tx

The modulation scheme specified in [1] is shown as in Fig. 4. The binary information from PPDU is mapped into data symbols by the bit-to-symbol block, where the four least significant bits of each octet are packed into one symbol, and the four most significant bits are packed into the next symbol. Then, the spreading function is performed by the symbol-to-chip block. Each symbol is spread as a 32-chip PN (pseudo-random noise) sequence. The chip sequences representing each symbol are modulated by the O-QPSK modulation block with the half-sine pulse shaping. The fundamental O-QPSK method is to sum the in-phase signal with quadrature phase signal delayed by half a cycle in order to avoid the sudden phase shift change that occurs in QPSK. The complex envelope of O-QPSK can be expressed as follows:

$$\tilde{s}(t) = \sum_i (-1)^i \cdot a_{2i-1} \cdot g(t-2iT_c + T_c) + j(-1)^i \cdot a_{2i} \cdot g(t-2iT_c), \quad (1)$$

where  $a_i$  is the binary data symbol,  $a_i = \pm 1$ ,  $T_c$  is the inverse of the chip rate, and  $g(t)$  is the half-sine pulse shape function:

$$g(t) = \begin{cases} \sin\left(\pi \cdot \frac{t}{2T_c}\right), & 0 \leq t \leq 2T_c \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

The O-QPSK with half-sine pulse shaping can be interpreted as the minimum shift keying (MSK). Since the MSK is the continuous phase frequency shift keying (CPFSK) with modulation index  $h=0.5$ , the complex envelope of the MSK can be expressed as

$$\tilde{s}_{MSK}(t) = \sum_i \exp\left(2\pi \cdot h \cdot d_i \cdot \int g_r(t) \cdot dt\right) \quad (3)$$

where the  $d_i$  is binary symbol,  $d_i = \pm 1$ ,  $g_r(t)$  is the rectangular pulse shape function with a amplitude of  $1/2T_c$ , and a period of  $T_c$ .

Notably, when the data symbol of O-QPSK is coded as  $d_i = a_i \cdot a_{i-1}$ , then MSK and the O-QPSK are identical. The MSK has the constant envelope feature, which allows the use of low-cost, nonlinear PAs in the transmitter design. Moreover, the MSK can be noncoherently demodulated. The noncoherent demodulation is preferred in cost-sensitive low-power applications, since it needs no complicated carrier recovery circuitry in the receiver design. Hence, we employ the MSK with the coding procedure,  $d_i = a_i \cdot a_{i-1}$ , to carry out the O-QPSK modulation.

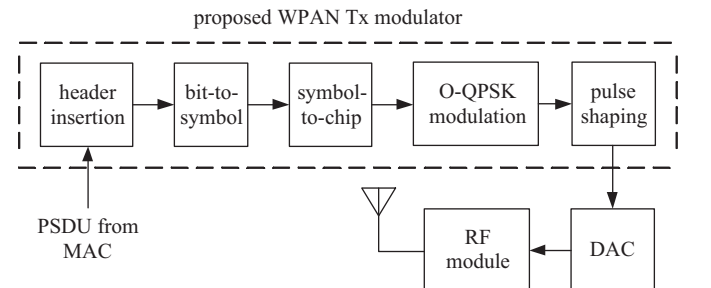


Fig. 4. Detailed block diagram of the proposed WPAN Tx modulator.

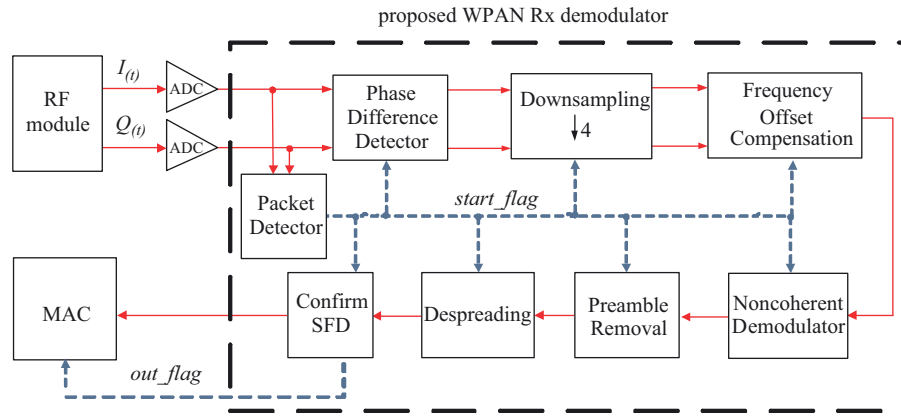


Fig. 5. Detailed block diagram of the proposed WPAN Rx demodulator.

## 2.2. Demodulator of WPAN Rx

Fig. 5 shows the block diagram of the WPAN Rx demodulator. The packet detector discriminates whether the incoming signal is data or noise. It enables the following stages if the incoming signal is determined to be data. The incoming signal are quantized to be 128 samples by the ADC. The downsampling stage computes the phase difference of each sample to find out the maximum phase difference and then performs the downsampling. The frequency offset compensation block computes the frequency offset and compensates the offset. The noncoherent demodulator stage utilizes the minimum shift keying (MSK) scheme to perform the demodulation process. The reason is that MSK is a special case of O-QPSK with sinusoidal symbol weighting, which can be noncoherently detected [13]. Hence, the proposed Rx adopts the MSK demodulation to implement a noncoherent receiver which possesses a low hardware complexity as well as low power consumption. The preamble removal stage acquires the preamble and removes it from PPDU packet. The despreading stage despreads each 32-chip PN sequence into 4-bit symbols. The confirm SFD stage acquires the length of the PSDU and notifies the MAC layer of receiving the PSDU from the receiver. The detailed description of each block is as follows.

### 2.2.1. Packet detector

Packet detector computes the energy of the incoming signal to determine whether it is data or noise. If the sum of the absolute values of incoming samples lied in a sliding window with length of  $L$  is greater than a predefined threshold, the incoming signal is determined as data. To reduce the complexity, the computation is accomplished by taking absolute value rather than square of the value. The window length,  $L$ , and the threshold are derived by detailed system simulations.

### 2.2.2. Downsampling

Since the proposed receiver design is based on the noncoherent scheme, the sampling clock of the ADC is not synchronized with the incoming signal. In order to acquire the correct data from the output of ADC, the sampling rate of the ADC in Fig. 5 is four times of the chip rate to provide sufficient samples for further processing. The block diagram of the downsampling block is shown in Fig. 6, where  $i=[n/4]$ . Firstly, we compute the phase difference between  $\theta$  and  $\theta$  delayed by  $T_c$ . By exploiting the property of MSK whose phase difference between two chips is  $\pm \pi/2$ , we accumulate the phase difference of  $128/4=32$  consecutive samples. Then, the path with the maximum sum into the MUX is the correct data. The best feature of the proposed

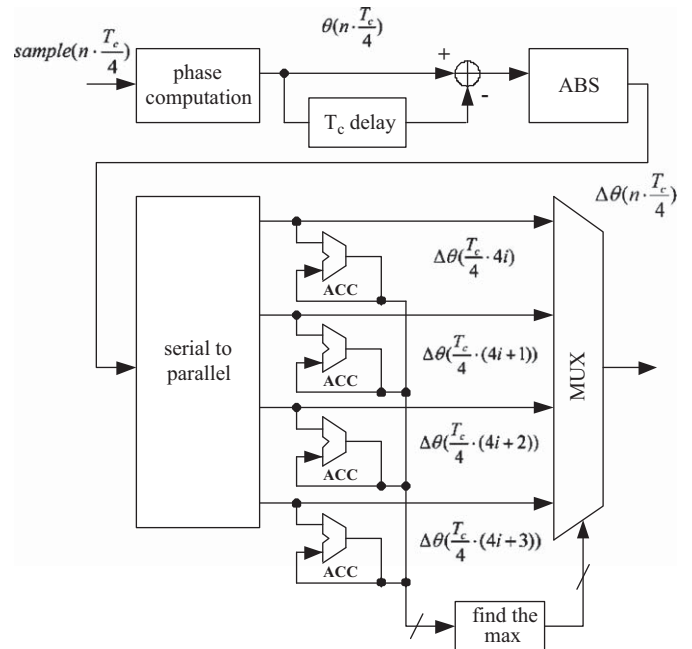


Fig. 6. The block diagram of the downsampling block.

downsampling design is that it is a feedforward design, where there is no feedback loop to slow down the system or cause any oscillation.

### 2.2.3. Frequency offset estimation

The frequency difference between the LO (local oscillator) at Tx and Rx results in the frequency offset. The frequency offset will cause a phase offset in the received data. As described above, the phase difference between two chips in the MSK is either  $\pi/2$  or  $-\pi/2$ . Thus, the frequency offset can be easily derived from the phase offset of each chip. Then, the frequency offset is compensated and the correct phase information is sent to the following blocks.

### 2.2.4. Noncoherent demodulator

The noncoherent demodulator is based on the differential detection [14], which is derived from the phase trellis state diagram of the MSK. The detailed block diagram is shown in Fig. 7. The demodulation is carried out by the sine phase comparator

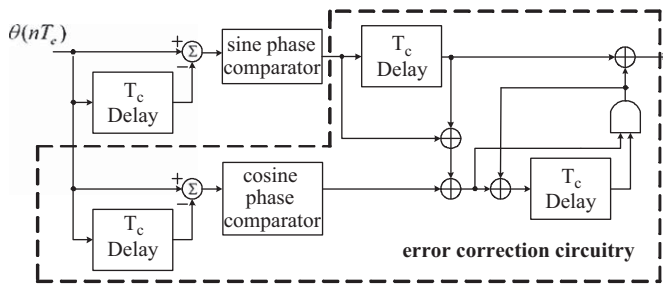


Fig. 7. The block diagram of the noncoherent demodulator.

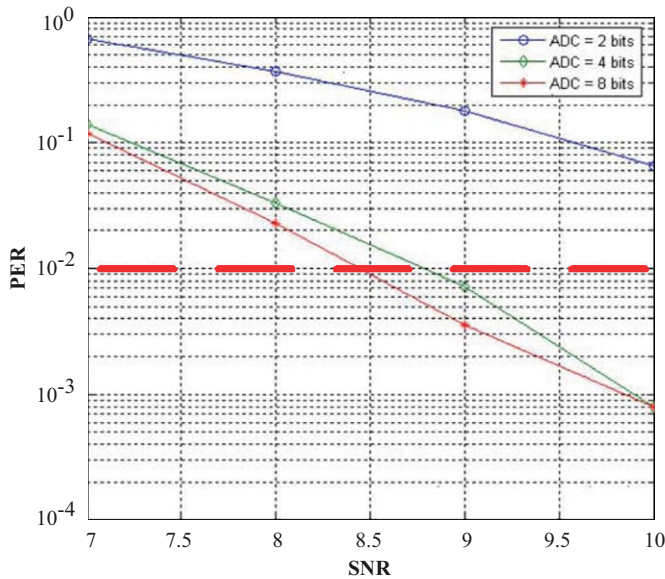


Fig. 8. The resolution requirement of the ADC derived by system simulation.

whose output is  $\sin(\theta(nT_c) - \theta((n-1)T_c))$ . The error correction circuitry is utilized to improve the PER and BER.

2.2.5. Confirm SFD

The Confirm SFD stage determines the frame length by acquiring the SFD field of the PPDU packet and notifies the MAC layer to receive the PSDU by sending an alarm signal.

2.3. ADC requirement

To provide sufficient samples for phase error estimation in the receiver, the sampling rate of the ADC is set to be four times the frequency of the input signals. Hence, the sampling rate of the ADC is at least 8 MS/s. The requirement of the ADC resolution can be derived by system simulations. According to [1], the packet error rate (PER) should be < 1% when the Eb/N0 is over 9 dB. Fig. 8 shows the MATLAB simulation results of the system performance given different ADC resolutions, where the 4-bit resolution is found to be sufficient to meet the system requirement. In summary, the ADCs are determined to be 4-bit, 8 MS/s ADCs.

3. Implementation and measurement

To evaluate the performance and the power consumption, the proposed design is implemented by using 0.18 μm single-poly six-metal CMOS technology. The die photo of the proposed prototype

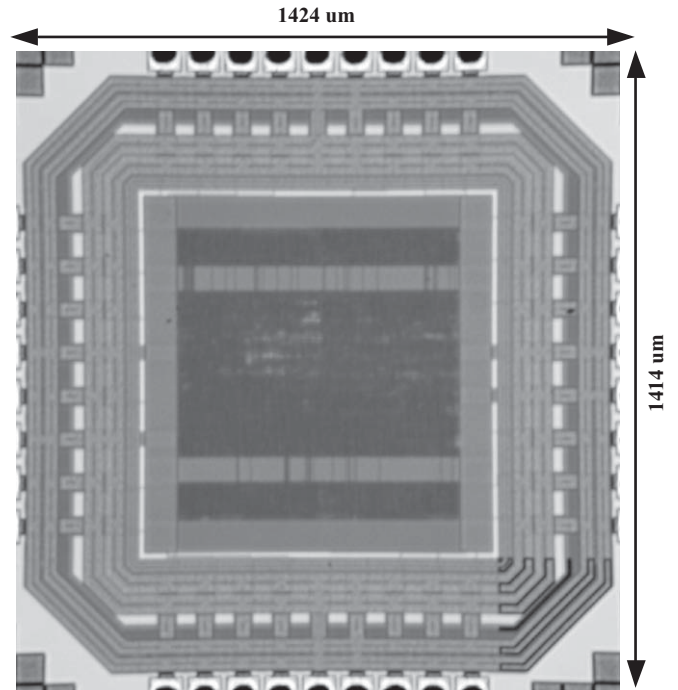


Fig. 9. Die photo of the proposed modulator/demodulator.

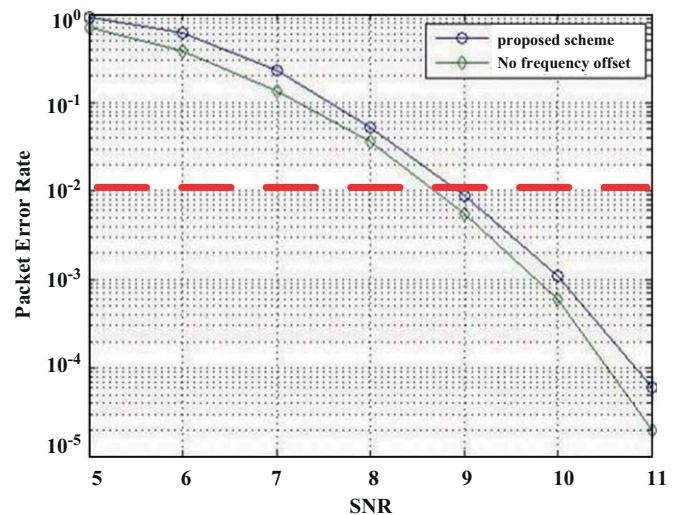


Fig. 10. PER of the proposed WPAN demodulator.

on silicon is shown in Fig. 9. A 48-pin S/B (Side Brazed) package is utilized.

The measurement is performed by the Agilent 93000 SOC series. The setup of the measurement follows the specification in [1], where the PSDU of each PPDU packet is set to be 20 bytes random numbers. Fig. 10 shows the PER of the proposed prototype, where the PER is < 1% at SNR of 9 dB when the frequency offset of a symbol (1 symbol = 15 chips), Δf, is 80 ppm. Fig. 11 shows the comparison of the simulated waveforms and the measured waveforms of the demodulator output, where the demodulator outputs the generated PSDU packet when the flag signal is asserted. The measured results exactly match the simulated results. The measured power consumption of modulator and demodulator at the clock rate of 8 MHz is 731 μW and 641 μW, respectively. Fig. 12 shows the Shmoo plot of the proposed design.

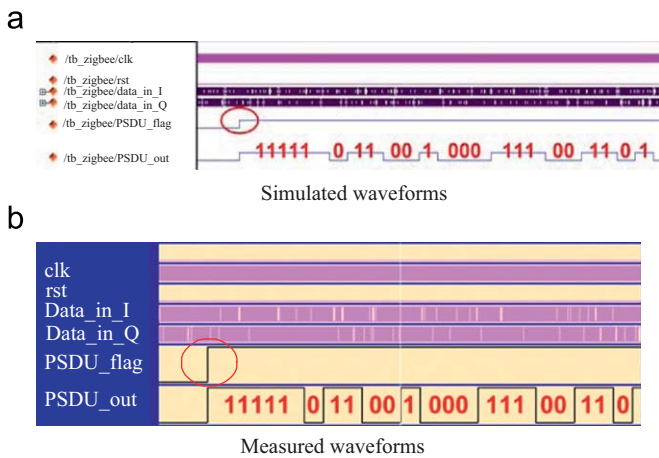


Fig. 11. (a) The simulated waveforms of the demodulator and (b) the measured waveforms of the demodulator.

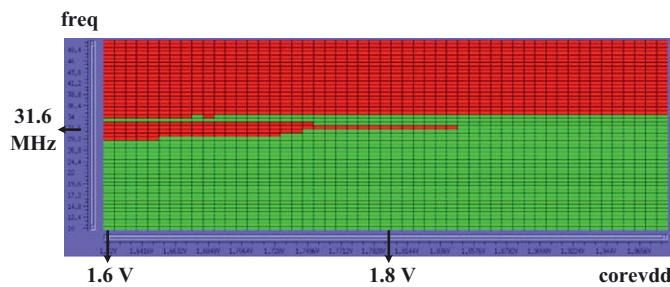


Fig. 12. Shmoo plot of the proposed design.

Table 2  
Specifications of the proposed WPAN modulator/demodulator.

Technology	0.18 $\mu\text{m}$ CMOS process
Power supply	1.8 V
System clock	8 MHz
Power consumption of modulator at 8 MHz	731 $\mu\text{W}$
Power consumption of demodulator at 8 MHz	641 $\mu\text{W}$
Core size	0.39 $\text{mm}^2$

Table 3  
Comparison between the proposed design and the prior work using 868/915 MHz band.

Design	[11]	ours
System	868/915 MHz	2.4 GHz
Power supply (V)	1.8	1.8
Modulator power ( $\mu\text{W}$ )	107	731
Demodulator power ( $\mu\text{W}$ )	144	641
FOM	1.594E8	1.822E8

The specifications of the proposed WPAN modulator/demodulator are summarized in Table 2. Eq. (4) shows a figure of merit (FOM) formula to compare the performance of the proposed work and the prior work [10]. The power dissipation of the modulator/demodulator using 2.45 GHz and 868/915 MHz is 1.327 mW and 251  $\mu\text{W}$  [10], respectively. The bit rate presented in Table 1 is 250 Kbps and 40 Kbps, respectively in these two designs. Therefore, Table 3 presents the FOM comparison of the proposed WPAN modulator/demodulator and the prior work

[10]. The FOM of the 2.45 GHz modulator/demodulator is better than that of [10].

$$FOM = \frac{\text{Bit rate}}{\text{Power dissipation}} \quad (4)$$

#### 4. Conclusion

In this paper, an architecture as well as hardware implementation of a low power WPAN modulator/demodulator for 2.45 GHz band is presented. The proposed design adopts the relatively simple algorithm to achieve the goal of a low power and low hardware complexity without sacrificing the performance. Hence, the overall power consumption of the proposed design is merely 1.37 mW at a 8.0 MHz system clock. It is highly suitable to be included in wearable or portable medical devices for the purpose of monitoring, analyzing, etc.

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