

All Digital Frequency Synthesizer Using A Flying Adder

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Abstract—This article presents an all digital frequency synthesizer (ADFS) based on the flying adder architecture. The flying adder (FA) is a fascinating architecture for frequency synthesizer designs due to its simplicity and effectiveness. The FA-based frequency synthesizer can simply use a set of multiple phase reference signals to generate a desired frequency to achieve fast frequency switching. In the proposed work, the frequency synthesizer adopts an all-digital phase-locked loop (ADPLL) to provide a steady reference signal for the FA. The proposed frequency synthesizer is implemented in a standard 0.18 μm CMOS cell-based technology and the core area is 0.16 mm^2 . The output frequency range is 39.38 MHz \sim 226 MHz and the peak-to-peak jitter is less than 130 ps.

Index Terms—ADPLL, flying adder, CMOS, low power, ADFS

I. INTRODUCTION

THE frequency synthesizer is an essential component for many systems to generate a desired frequency for frequency conversion in RF transceivers or signal synchronization in SOC (system on chip) systems [1]. Therefore, a good frequency synthesizer design should meet the requirements of fast frequency switching and wide output frequency range. The most popular architecture of the existing solutions can be classified into PLL(phase-locked loop)-based frequency synthesizers and DDFSs (direct-digital frequency synthesizer). The PLL-based frequency synthesizers can easily generate high output frequency, but they usually suffer from an inherent inability to simultaneously provide both fast frequency switching and high spectral purity [2]. Besides, the wide tunable output frequency range is still a challenging topic in the PLL designs. DDFSs adopt mathematical manipulations to directly synthesize the output frequency, where the implementation can be realized by either the memory-based phase-to-sine mapping or an algorithm-based phase-to-sine conversion [3] - [11]. Due to the absence of the feedback loop and VCO (voltage-controlled oscillator), DDFSs can accomplish the fast frequency switching and the wide output range more easily compared to the PLL-based solutions. DDFSs are also able to maintain the continuous phase during the process of frequency switching. The main drawback of the DDFS is that they need a high resolution DAC (Digital-to-Analog Converter) to convert

the digital signals into an analog signal. Therefore, how to design a high speed and high resolution DAC becomes another difficult topic.

The flying adder architecture was firstly introduced in [13] to overcome the problem associated with the conventional frequency synthesizers. By exploiting a set of n reference signals with the same frequency but a multiphase clock, i.e., with a fixed phase step of $360 \text{ degrees}/n$, the flying adder can generate the output frequency up to $n/2$ times of the reference frequency [12]. Notably, this architecture can generate a high output frequency using low frequency reference signals, which is a favorably effective and cost-efficient scheme for the demand for high speed clock generation in the modern SOCs. Prior works, [13] - [17], adopted the PLL to provide the reference signals. However, the traditional PLL design parameters of mixed-signal circuits seriously depend upon CMOS technology, which results in a poor reusability, particularly in the trend of the scaling down of the CMOS technology. This paper presents an all digital frequency synthesizer (ADFS) based on the flying adder architecture, where the reference signals is supplied by an all-digital PLL (ADPLL).

II. ALL DIGITAL FREQUENCY SYNTHESIZER ARCHITECTURE

Fig. 1 shows the block diagram of the proposed all digital frequency synthesizer architecture. The ADPLL [18] - [22] is employed to track the phase of the reference clock, CLK_IN , and generate a phase-locked clock signal, OUT_CLK , to the delay chain block. The delay chain produce 32 reference signals with an equal phase difference. The flying adder uses the multiple phase reference signals to synthesize the desired frequency according to the frequency control word, FCW . The details of each function block in Fig. 1 are described as follows.

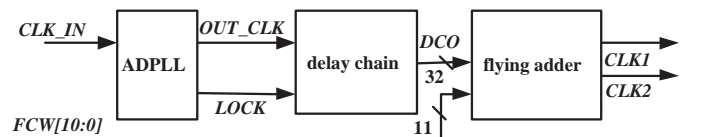


Fig. 1. The block diagram of the proposed all digital frequency synthesizer.

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A. All-digital phase-locked loop

The detailed block diagram of the ADPLL is shown in Fig. 2, where the ADPLL is composed of a phase frequency detector (PFD), a frequency divider (FDIV), two digital-controlled

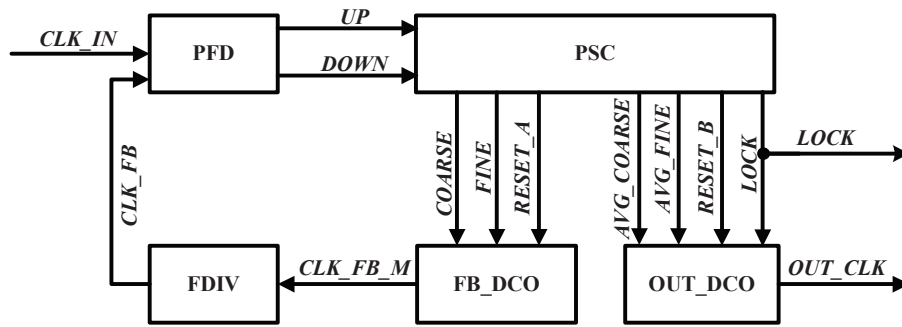


Fig. 2. Block diagram of the ADPLL.

oscillators (FB_DCO and OUT_DCO), and a phase searching controller (PSC). PFD detects the phase difference between the reference clock CLK_IN and the feedback clock CLK_FB . When CLK_FB lags CLK_IN , PFD generates a negative impulse on UP , while $DOWN$ remains at high to inform PSC to speed up the FB_DCO. On the contrary, a negative impulse on $DOWN$ is generated to slow down FB_DCO if CLK_FB leads CLK_IN . The PSC generates two signals, $COARSE$ and $FINE$, for FB_DCO to select an oscillating frequency of the multiplied clock signal in feedback loop, CLK_FB_M . The frequency of CLK_FB_M is divided by FDIV to generate the divided signal CLK_FB which is sent back to PFD.

If the phase of the CLK_IN is clocked, a signal $LOCK$ is generated by PSC to indicate that the frequency is locked successfully. To further reduce the jitter caused by deadzone of the PFD and the finite resolution of FB_DCO, the PSC computes the averaged values of $COARSE$ and $FINE$, i.e., AVG_COARSE and AVG_FINE , respectively, for OUT_DCO to generate the stable output signal OUT_CLK . The PSC uses a binary search scheme, as shown in Fig. 3 to control the DCOs to generate the oscillating frequency with desired phases for the locking process.

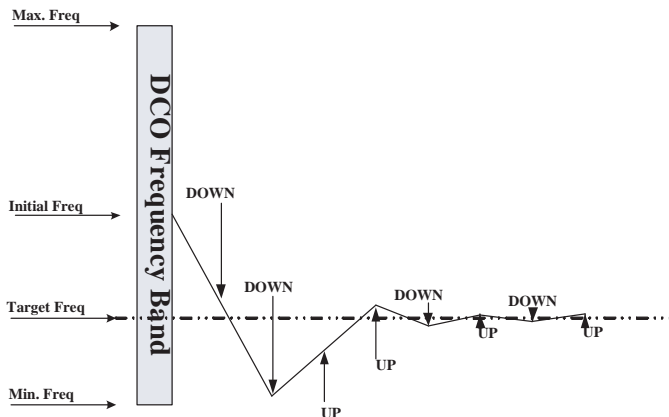


Fig. 3. The binary search for the target frequency [22].

Referring to Fig. 2, there are two DCOs, FB_DCO and OUT_DCO. The FB_DCO is located at the feedback loop, which is employed to lock the phase of the reference signal, and the OUT_DCO generates the output signal when the phase

is locked. Fig. 4 shows the block diagram of the FB_DCO. The control words, $COARSE$ and $FINE$, select the appropriate delay cells of the COARSE-TUNE and FINE-TUNE blocks, respectively, to generate the desired oscillating frequency. The operation of the OUT_DCO is similar to the FB_DCO. In [23], the tri-state buffers were used to switch the delay cells. However, using the tri-state buffer might cause timing violations. The reason is that the “high-Z” state caused by the tri-state buffers will be fed back to feedback loop of the ADPLL when the control signals to switch tri-state buffers do not arrive at the same time. As a result, it will cause the timing hazard during the locking process. Instead, we adopt multiplexers to switch the delay cells to resolve this problem. Additionally, a rising edge of the input signal of the multiplexer is pre-set to wait for $COARSE$ and $FINE$ signals and then switch the delay line such that the timing violation can be avoided.

B. Delay Chain

If the ADPLL successfully locks the phase of the reference clock, CLK_IN , the output of the ADPLL is passed to the delay chain to generate the multiple phase signals for the flying adder. The delay chain is composed of a series of the buffer cells as shown in the Fig. 5(a). Fig. 5(b) depicts the resultant reference signals, where Δ is the propagation delay of each buffer. A larger number of the resultant reference signals gives a finer frequency resolution. The number of the buffers is 32 in our design. For instance, if we need 120 MHz as the ADPLL output frequency, Δ should be 0.2625 ns. Therefore, the delay chain in the proposed design preferably consists of 32 buffers with a 0.2625 ns propagation delay.

C. Flying Adder

The flying adder architecture is adopted in the proposed frequency synthesizer. Fig. 6 shows the block diagram of the flying adder [14], where the PART_A and PART_B are similar circuits, where the major difference between these two function blocks is the size of the adders. Referring to PART_B, when $CLK2$ is high, the summation of ADD_1 and reg_1 is stored in the reg_2 , and the value previously stored in the reg_2 is passed to a 32-to-1 multiplexer, MUX1, to select one of the delay chain output signals, $DCO[31:0]$, as the input signal of the 2-to-1 multiplexer, MUX3. The

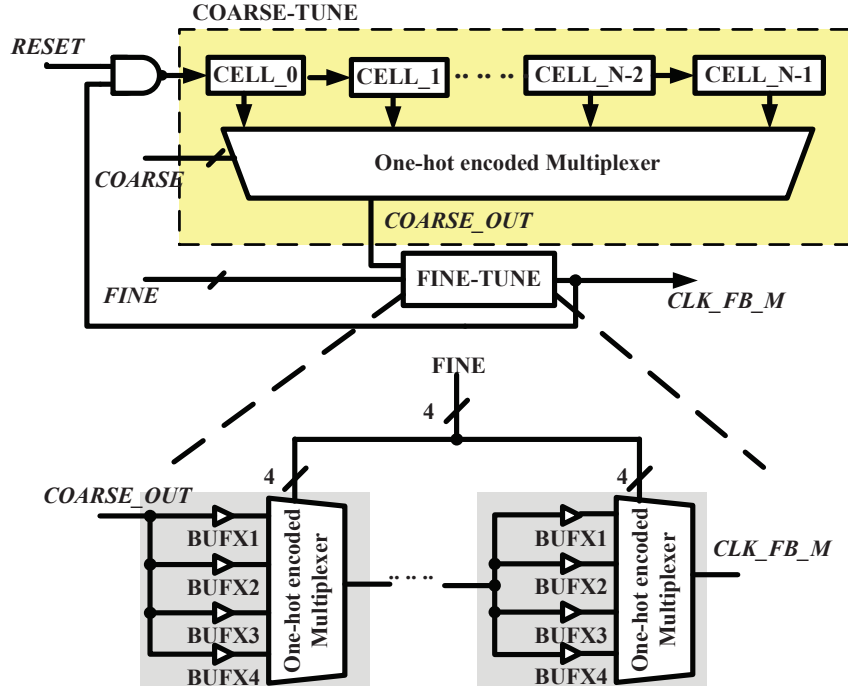


Fig. 4. The block diagram of the FB_DCO.

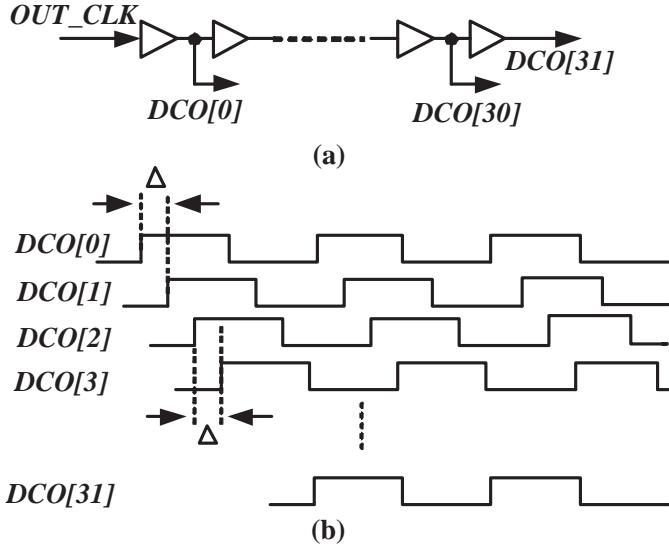


Fig. 5. (a) The schematic of the delay chain. (b) The resultant multiple phase reference signals.

accumulation step in PART_B is determined by the frequency control word, $FCW1$. The operation of the PART_A is similar to the PART_B except that the reg_4 is triggered by $CLK1$. Therefore, MUX3 always selects the signal generated at last half clock cycle, which can avoid the glitch caused by the transition of the input signal propagating through the MUXs. Eliminating the glitch can prevent the D-type flip-flop (DFF) from being triggered by false signals.

The desired frequency is synthesized by triggering the DFF with the signal selected from DCO . The relation between the frequency control word, FCW , and the desired frequency,

f_{out} can be expressed as follows:

$$\frac{1}{f_{out}} = \frac{T_{DCO}}{N} \times FCW, \quad (1)$$

where T_{DCO} is the period of the DCO signals, and N is the number of the DCO signals [24]. For example, to obtain an output frequency of 150 MHz given that the number and the frequency of the DCO signals are 32 and 150 MHz, respectively, the required FCW is around $25.371=(011001.01011)_2$. The longer length of the FCW 's decimal part results in a finer frequency resolution. The length of the FCW in the proposed frequency synthesizer is 11 bits, where $FCW[10:5]$ and $FCW[4:0]$ represent the integer part and the decimal part, respectively.

III. IMPLEMENTATION AND MEASUREMENT

The proposed ADFS is carried out by the standard 0.18 μm CMOS technology to verify the performance. All of the process corners : $[0^\circ\text{C}, +100^\circ\text{C}]$, and (SS, TT, FF) models, are simulated. Fig. 7 shows the waveform of the synthesized frequency. Referring to Fig. 7(a), when the phase of CLK_{IN} is locked, the ADPLL generates a 80 MHz clock signal, OUT_CLK , and the synthesized frequency, $CLK1$ is changed from 39.38 MHz to 170 MHz according to the change of the FCW , where the frequency switching latency is two $CLK1$ cycle. Fig. 7(b) shows a part of the multiple phase reference signals produced by the delay chain.

Fig. 8 shows the die photo of the proposed frequency synthesizer. Fig. 9 reveals that when the frequency of the ADPLL clock signal is locked, where the locked frequency is 187.5 MHz, the 3rd harmonic frequency is 570 MHz. At the same locked frequency, the voltage and time of the

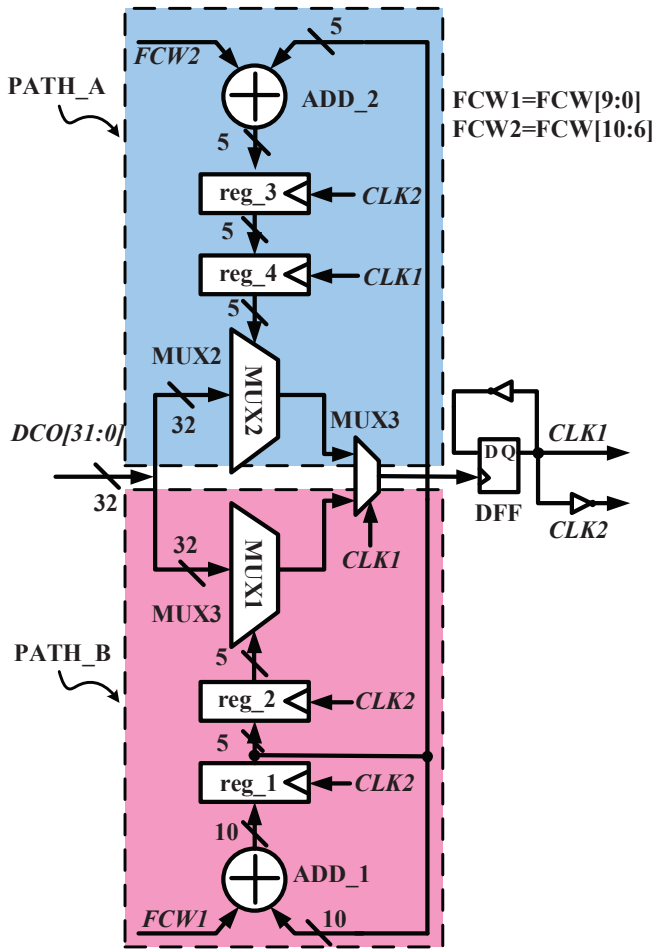


Fig. 6. The Flying Adder.

eye diagram depicted in Fig. 10 are 1.31 V and 2.43 ns, respectively. Referring to Fig. 11, which is a measurement result on Agilent SOC 93000, $CLK1$ varies from 80 MHz to 40 MHz when FCW is updated. It takes only four OUT_CLK cycles to re-lock. The performance comparisons of our design and several prior works are summarized in Table I. The proposed ADPLL attains the edge of low power and short lock time (cycles).

IV. CONCLUSION

The flying adder architecture was developed to resolve challenges encountered in the design of the conventional PLL-based frequency synthesizer. Although the flying adder architecture only needs a simple PLL to provide multi-phased signals, the integration of the mixed-signal circuits still needs efforts on both the design and the simulation stages. Besides, analog circuits are much more sensitive to the variation of the technology compared to the digital circuits. In this paper, we propose an all digital frequency synthesizer based on the flying adder architecture, where the mixed-signal PLL is replaced with a low-power ADPLL. Moreover, the glitch hazard on both the flying adder and the ADPLL is eliminated to ensure the stability of the frequency synthesizer.

TABLE I
PERFORMANCE COMPARISONS WITH SEVERAL PRIOR WORKS

ADPLL	[25]	[26]	[18]	[27]	Ours
Process (μm)	0.18	0.18	0.18	0.18	0.18
Year	2005	2008	2009	2009	2009
Maximum Frequency (MHz)	1500	725	250	560	226
Minimum Frequency (MHz)	520	70	87	53	39.38
Supply Voltage (V)	1.8	1.8	0.9	N/A	1.8
Maximum Lock Time (cycles)	≤ 96	≤ 72	≤ 72	N/A	≤ 4
Jitter (ps)	76	N/A	152	51	130
Power Dissipation (mW)	26.8	27	5.4	25.2	3.6
Area (mm^2)	0.27	0.174	0.76	0.14	0.16

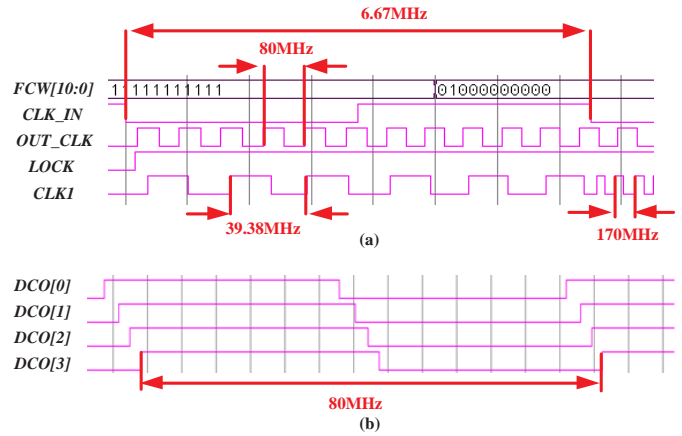


Fig. 7. The waveform of the generated output signal: (a) the output frequency is changed from 39.38 MHz to 170 MHz; (b) multiple phase reference signals generated by the delay chain.

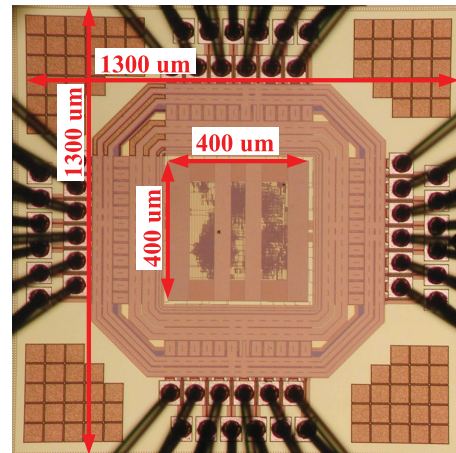


Fig. 8. The die photo of the proposed frequency synthesizer.

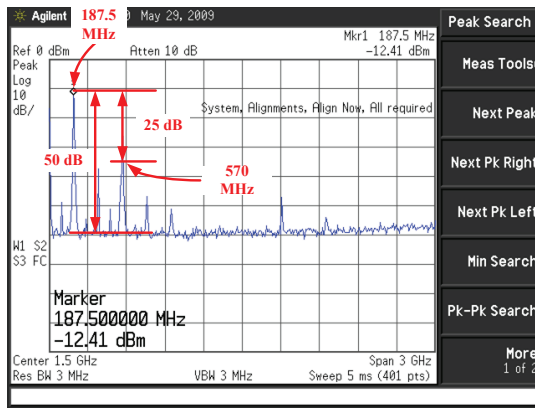


Fig. 9. The waveform of the output frequency locked on 187.5 MHz.

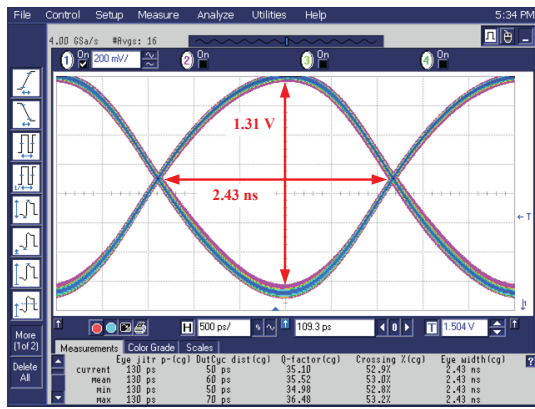


Fig. 10. The eye diagram for the output synthesized frequency, where locked frequency is 187.5 MHz.

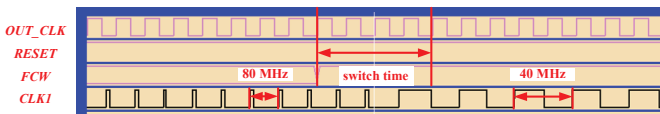


Fig. 11. The waveform of the output frequency switching from 80 MHz to 40 MHz.

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