A 800 Mbps and 12.37 ps Jitter Bidirectional Mixed-Voltage I/O Buffer With Dual-Path Gate-Tracking Circuit

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***Abstract*—This paper proposes a high speed bidirectional mixed-voltage I/O buffer using 90 nm 1.2 V standard CMOS process. By using a dynamic gate bias generator to provide appropriate gate drive voltages for the output stage, the I/O buffer can transmit/receive 2 × VDD voltage level signal without any gate-oxide overstress hazard. Most important of all, the gate-oxide overstress hazard is eliminated by adopting a dual-path gate-tracking circuit. The maximum data rate and jitter are measured to be 800 Mbps/12.37 ps and 704 Mbps/14.79 ps for 1.2 V and 2.5 V signal voltage, respectively, with a given capacitive load of 20 pF.**

***Index Terms*—Dual-path gate-tracking circuit, floating N-well circuit, gate-oxide reliability, I/O buffer, mixed-voltage-tolerant.**

I. Introduction

WITH the rapid development of semiconductor technologies, the dimensions and supply voltages of the integrated circuit (IC) are evolved to nano-meter scale so as to reduce the area cost and power consumption [1]. During such an evolution, many chips in a PCB-based system are fabricated by different technologies to meet the requirements of various interfacing specifications, e.g., PCI-X and PCI-express. A signal voltage level compatibility problem appears when those chips are used to communicate with one another, since the voltage levels of these chips might be different. Traditional I/O buffers are no longer adequate to these different voltage-level signals due to the hazards of gate-oxide overstress, hot-carrier degradation, and unwanted leakage current paths [1]–[5]. By contrast, mixed-voltage I/O buffers are considered as a better solution to reduce the time-to-market than extra off-chip level shifters. Another advantage is the reduction of PCB area thanks to the removal of the voltage level shifters. Three types of mixed-voltage I/O buffers have been reported in prior works.

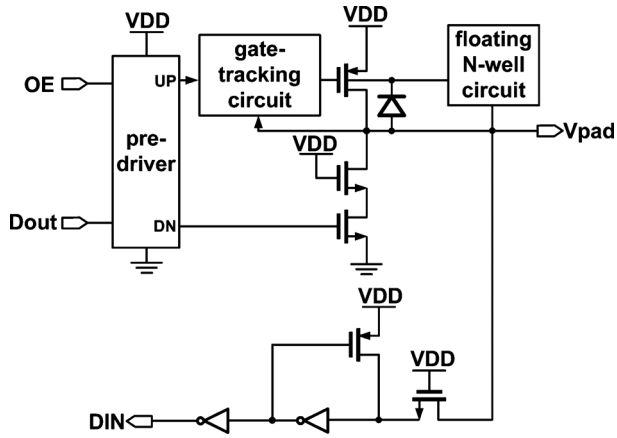

Fig. 1. Type I mixed-voltage I/O buffer with the gate-tracking and floating N-well circuits.

Type I mixed-voltage I/O buffer is able to receive the signals at 2 × VDD, as shown in Fig. 1 [6]–[9]. By using the stacked NMOS, the gate-oxide overstress at the output NMOS transistor can be avoided when 2 × VDD is received. Besides, the gate-tracking and floating N-well methodologies are used to remove the unwanted leakage current path through the output PMOS and its parasitic diode, respectively. The mentioned stacked NMOS and leakage elimination methodologies are only activated when 2 × VDD appears in the receiving mode. Thus, Type I mixed-voltage I/O buffer can only receive the high voltage signal, but it can not transmit a high voltage signal. Let alone a 2 × VDD signal.

Type II mixed-voltage I/O buffer, which can transmit high voltage signals, was disclosed in Fig. 2[10]–[12]. To avoid the gate-oxide overstress, two individual stacked PMOS and NMOS are used in the output stage. Besides, a level shifter and a bias circuit are employed to provide the appropriate gate bias voltages for the transistors in the output stage. However, these designs overlooked the problem of unwanted leakage current paths when a high voltage signal is biased at the PAD in the receiving mode.

Type III mixed-voltage I/O buffer can transmit and receive signals with high, typical, and low voltage levels (VDDH, VDD, and VDDL) by including the mentioned methodologies,

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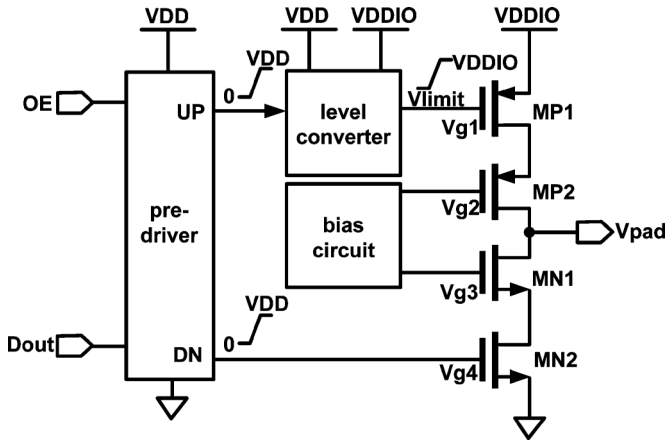

Fig. 2. Type II mixed-voltage I/O buffer with the level converter and bias circuit.

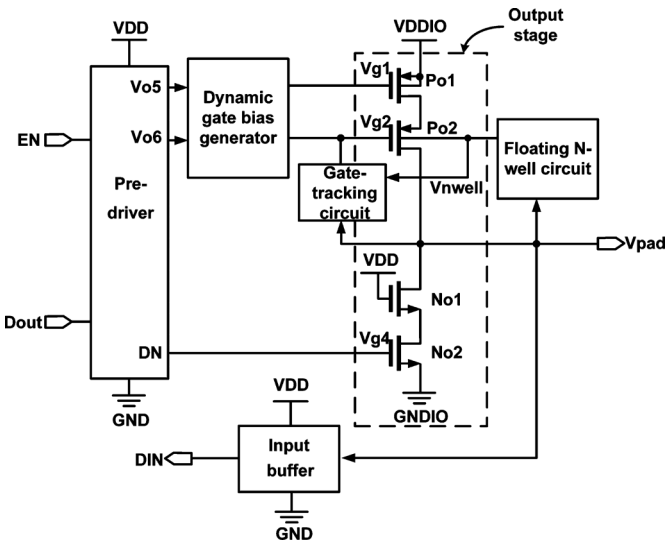

Fig. 3. Type III mixed-voltage I/O buffer with the gate-tracking circuit, floating N-well circuit and dynamic gate bias generator.

as shown in Fig. 3 [1], [13]. However, these reported I/O buffers can only communicate with the signal $\approx 1/2 \times$ VDD. When the supply voltage (VDDIO) is scaled down to be lower than $1/2 \times$ VDD, the output signal is difficult to be pulled up to the required I/O voltage (VDDIO) due to the body effect of the output PMOS and the low turn-on voltages (Vgs) of the output NMOS. On the other hand, the input stages of this type of I/O buffers could not receive the signals with amplitude lower than $1/2 \times$ VDD. It is the reason why a lower bound of $1/2 \times$ VDD appears in the state-of-the-art of the mixed-voltage I/O buffers.

Notably, in past several years, many mixed-voltage I/O buffers were reported to deal with the chip interface problems of different voltage levels [14]–[17]. However, the transmitting and receiving frequency of most previously mentioned works are not fast enough to meet the specification of PCI-express, which is up to 266 MHz. Therefore, a wide range I/O buffer with high speed able to simultaneously transmit and receive signal from VDD to $2 \times$ VDD is very much needed as a total solution for these scenarios.

This work proposes a high speed I/O buffer using 90 nm 1.2 V CMOS process, which can transmit and receive the signal of $2 \times$ VDD/VDD without any gate-oxide overstress and leakage current. To communicate the signal with $2 \times$ VDD swing, double stacked transistors and the dual-path gate-tracking circuit are used in the output stage to avoid the gate-oxide overstress. Notably, a simplified floating N-well circuit with low power consumption is adopted to avoid leakage current path produced by parasitic diodes. Meanwhile, no thick oxide layer is used. The higher bound of the operating voltage is expanded to be over $2 \times$ VDD. The output frequencies for VDDIO $= 2 \times$ VDD/VDD are measured to be 800/704 Mbps, respectively, at a given capacitive load of 20 pF. Besides, the current drive capability with ESD protection is also justified in this paper.

In Section II, the functions of each block in the bidirectional mixed-voltage I/O buffer are described in detail. In Section III, the proposed dual-path gate-tracking circuit is disclosed, including five modes. In Section IV, the measurement results, including die photo and eye diagrams, are given to justify the function of the proposed design. A brief conclusion is given in Section V.

II. VDD to $2 \times$ VDD Bidirectional Mixed-Voltage I/O Buffer

Fig. 4 shows the block diagram of the proposed VDD to $2 \times$ VDD Bidirectional Mixed-Voltage I/O buffer composed of a Pre-driver, an Input stage, an Output stage, a VDDIO detector, a Vg1 generator, a Floating N-well circuit, and a Dual-path gate-tracking circuit.

A. Pre-Driver

The details of Pre-driver in Fig. 4 are shown in Fig. 5, which is a decoder circuit to pre-drive Vg1 generator, Dual-path gate-tracking circuit (i.e., OE), and Output stage (i.e., Vg4). When the voltage of control signal (OE) is at logic 1, the I/O buffer enters the transmitting mode (Tx mode). The logic state of Vpad must be determined by DOUT. Besides, the current driving capability of the signal DOUT will be boosted by the Pre-driver to drive these transistors with large dimensions (i.e., Po1, Po2, No2). On the other hand, the I/O buffer is at the receiving mode (Rx mode) given that OE is logic 0. The receiving signal Din would be determined by Vpad. The details of Input stage will be disclosed in the following text. For the sake of clarification, the Boolean equations as well as the functionality of each output signals in Pre-driver are tabulated in Table I.

B. Output Stage

Since the supply voltage of the core circuit is 1.2 V in 90 nm CMOS process, the output stage must be realized with two stacked PMOS and NMOS, as depicted in Fig. 4. Besides, the appropriate gate voltages are needed for Po1, Po2, No1, and No2 to ensure the gate-oxide reliability and correct functions. The detailed gate drives of the Output stage are tabulated in Table II, including Vg1, Vg2, Vg3, Vg4, and Vnwell, which are described as follows.

Po1: Because the voltage difference between the gate and source (Vgs) must be smaller than 1.2 V, the Vg1 must be larger than 'VDDIO—1.2 V' in Tx mode. By contrast, Po1

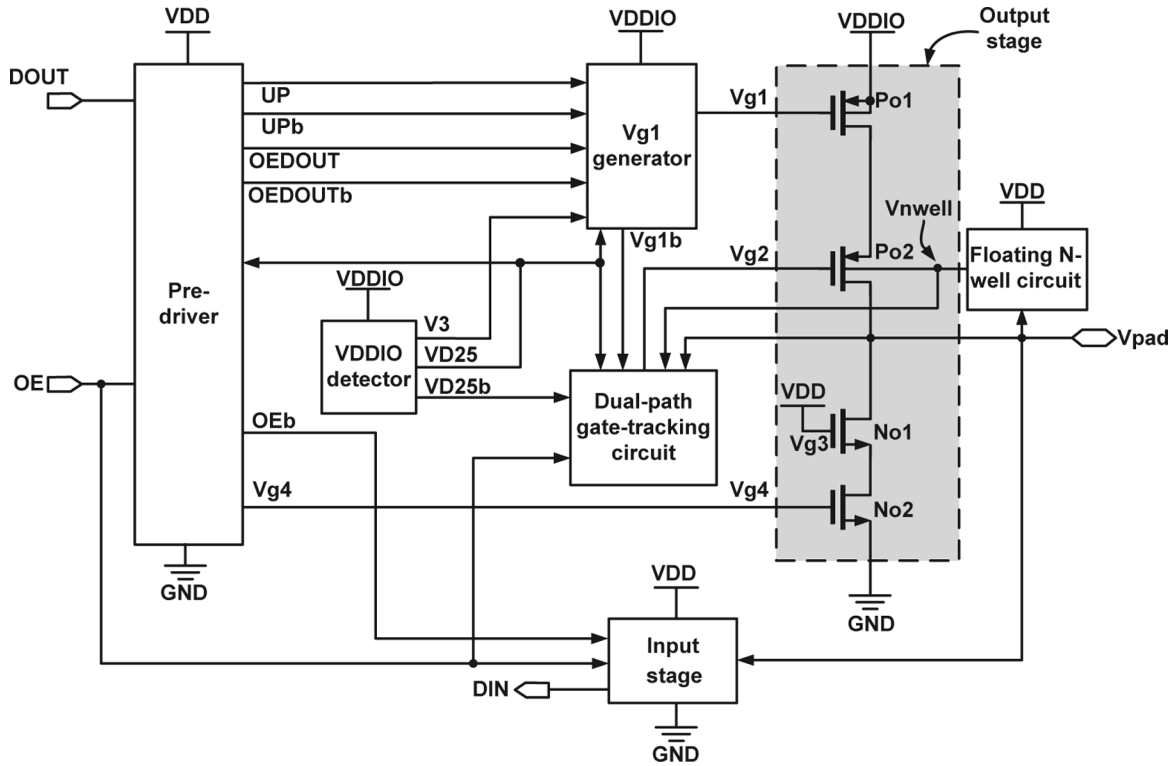

Fig. 4. The proposed mixed-voltage I/O buffer.

TABLE I
FUNCTIONALITY OF EACH OUTPUT SIGNALS OF PRE-DRIVER

	Boolean equation	Functionality
OEb	$\overline{OE}$	An inverted OE signal is generated.
OEDOUTb	$\overline{OE \,\&\, DOUT}$	When I/O buffer is operated in Tx mode, DOUT signal is sent to Vg1 generator.
OEDOUT	$\overline{OEDOUTb}$	An inverted OEDOUTb signal is generated.
Vg4	$OE \,\&\, OEDOUTb$	When I/O buffer is operated in Tx mode, Vg4 signal is the inverted DOUT signal.
UP	$\overline{VD25 \,\&\, OEDOUT}$	If I/O buffer is operated in 2×VDD, UP is sent to Vg1 generator.
UPb	$\overline{UP}$	An inverted UP signal is generated.

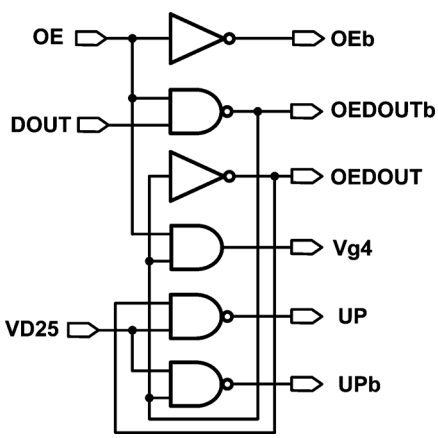

Fig. 5. Pre-driver.

must be turned off in Rx mode, which means the Vg1 must be equal to VDDIO.

Po2: Because the voltage difference between the gate and drain (Vgd) must be smaller than 1.2 V in Tx mode, Vg2 must be in the range between 'VDDIO—1.2 V' and '1.2 V'. By contrast, the I/O buffer detects the signal with high voltage in Rx mode, Vg2 is set to the same as the voltage of Vpad. Since the voltage difference between the bulk and drain (Vbd) must be smaller than 1.2 V, Vnwell should be varied with Vpad. If Vpad equals to VDDIO, Vnwell is pulled high to VDDIO in Tx mode. On the other hand, if Vpad is 0 V, Vnwell must be pulled low to 1.2 V in Tx mode. In Rx mode, Vnwell behaves like Vg2.

No1: No1 is always turned on in Tx and Rx modes to provide a voltage stress relaxation mechanism from Vpad. Therefore, Vg3 is driven by VDD, which still is in the tolerance of reliability.

No2: Because the Vgd and Vgs must be smaller than 1.2 V in Tx mode, Vg4 must be in the range between 'VDDIO—1.2 V' and '1.2 V'. Therefore, Vg4 can be directly driven by VDD = 1.2 V. No2 must be turned off in Rx mode when Vg4 is 0 V.

C. VDDIO Detector

VDDIO detector is mainly implemented using a string of diode-connected PMOS transistors to generate several voltage biases, V1–V6, as illustrated in Fig. 6. When VDDIO is at 2 ×

TABLE II
GATE VOLTAGES OF THE OUTPUT STAGE

	VDDIO (V)	Vg1 (V)	Vg2 (V)	Vg3 (V)	Vg4 (V)	Vnwell (V)
Rx mode	2×VDD	VDDIO	VDD/Vpad[a]	VDD	0 V	VDD/Vpad[a]
Rx mode	VDD	VDD	VDD	VDD	0 V	VDD
Tx mode	2×VDD	>'VDDIO-1.2'/VDDIO	>'VDDIO-1.2 V'	VDD	0 V/VDD	VDDIO/VDD
Tx mode	VDD	0 V/VDD	0 V	VDD	0 V/VDD	VDD

[a] When 2×VDD is received.
[b] The left side value is that I/O buffer transmits logic 1; the right side value is that I/O buffer transmits logic 0

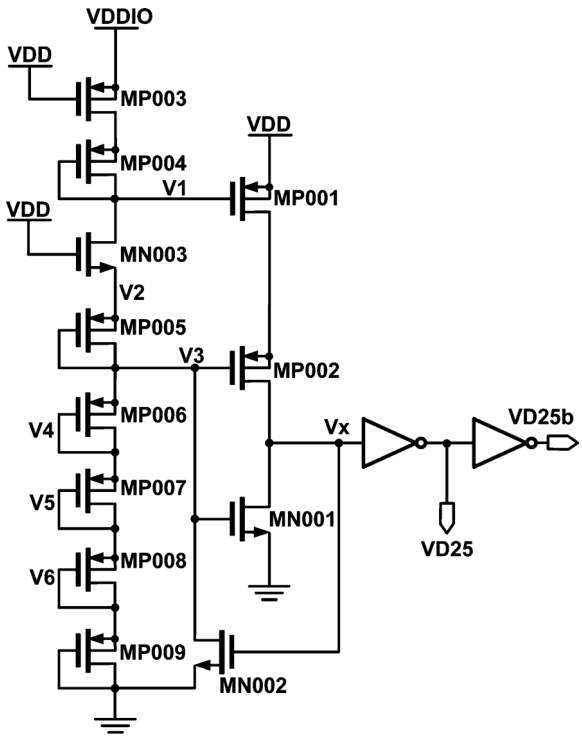

Fig. 6. VDDIO detector.

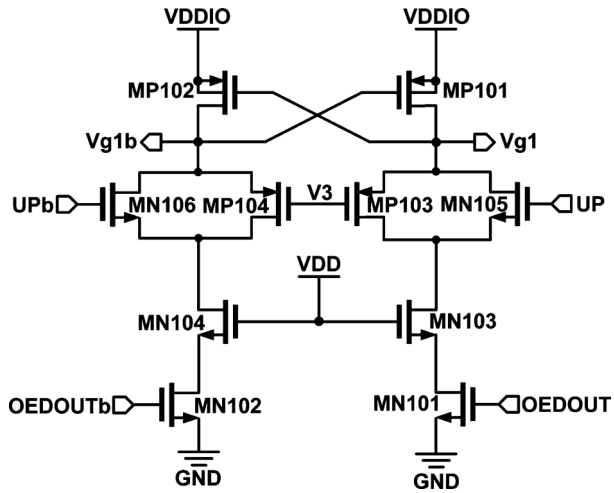

Fig. 7. Vg1 generator.

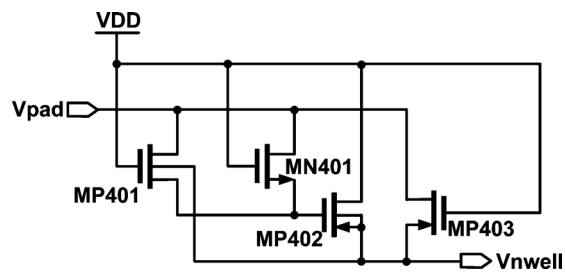

Fig. 8. Flaoting N-well circuit.

VDD, MP003 is turned on and V1 is high enough to turn off MP001. To keep the voltage drop between V1 and the voltage of node Vx less than 1.2 V, MP002 is inserted at the drain of MP003. The gate voltage of MP002, V3, is then maintained less than 'VDD – $\mathrm{Vthp}_{\mathrm{MP005}}$' ($\approx 0.8$ V), which is the threshold voltage of MP005, to avoid reliability problems. Meanwhile, MN001 is turned on to discharge the voltage of node Vx to 0 V. The state of VD25 is then pulled up to logic 1. On the other hand, when VDDIO is at VDD, MP003 is turned off so that MP001 and MP002 are both turned on to pull up the voltage of node Vx to VDD. The state of VD25 is then pulled down to logic 0. As soon as the voltage of node Vx is up to VDD, MN002 is turned on to shut off MN001 to eliminate the leakage current.

D. Vg1 Generator

Referring to Fig. 7, Vg1 generator in Fig. 4 is like a voltage level converter, which generates a pair of complementary signals, Vg1 and Vg1b. Vg1 generator is composed of two cross-coupled PMOS transistors as a latch with stacked NMOS transistors in series as discharging paths. In Rx mode, the voltage of OEDOUT is biased at 0 V to pull high Vg1 to VDDIO. Thus, Po1 of Output stage in Fig. 4 can be turned off to eliminate the risk of any leakage current. In Tx mode, when VDDIO is 2 × VDD and the signal Dout is at logic 1, the voltage of OEDOUT is logic 1 to turn on the MN101. Then, Vg1 can be discharged down to $\mathrm{V3} + \mathrm{Vthp}_{\mathrm{MP103}}$ through MP103, MN103, and MN101, where $\mathrm{Vthp}_{\mathrm{MP103}}$ is the threshold voltage of MP103. At the same time, the voltage of OEDOUTb is biased at 0 V, MN102 is turned off to pull Vg1b up to VDDIO, which can also turn off the MP101 to prevent any static leakage current path.

E. Floating N-Well Circuit

A simplified floating N-well circuit is adopted in this study, as shown in Fig. 8. When Vpad is higher than VDD, MP403 is turned on. Thus, Vnwell can be charged up to Vpad to avoid

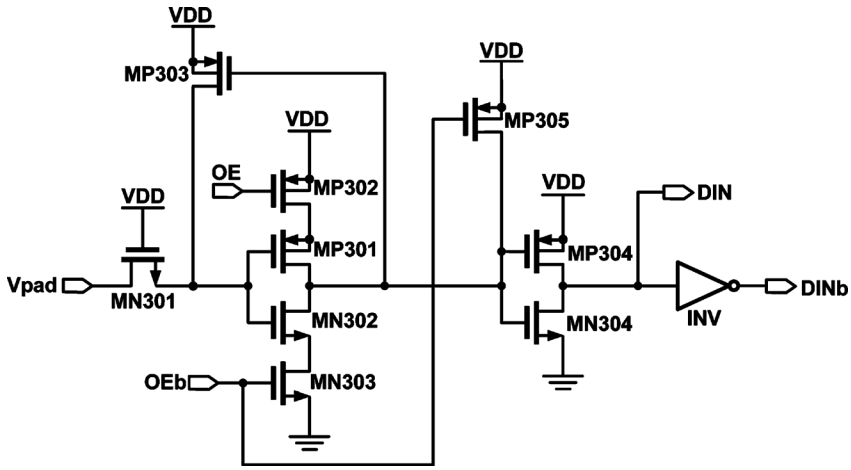

Fig. 9. Input stage circuit.

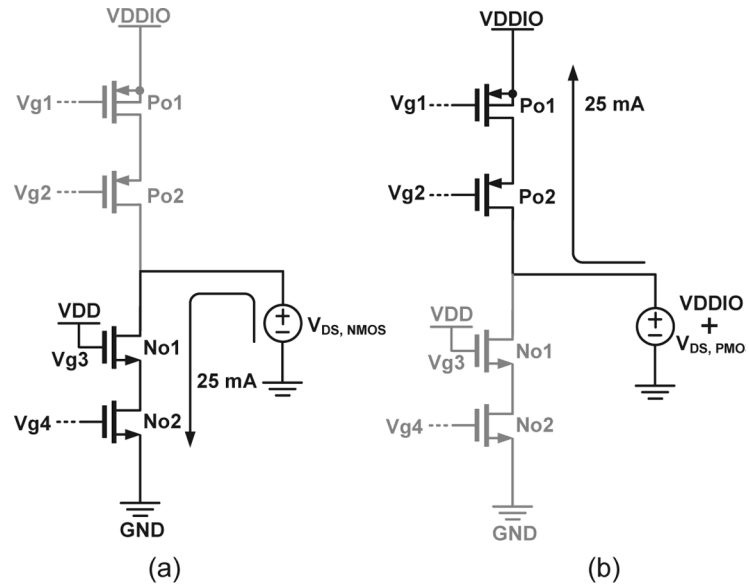

Fig. 10. The simplified circuit of output stage with ESD protection. (a) Discharging path. (b) Charging path.

the undesired leakage current path through the parasitic diode of Po2 in Output stage of Fig. 4.

F. Input Stage

As shown in Fig. 9, Vpad is clamped around 0.8 V by MN301 to prevent MP301 and MN302 from gate-oxide overstress in Rx mode, while MP303 acting as a weak feedback latch is used to charge the gate voltages of MP301 and MN302 to VDD. In Tx mode, MP305 is turned on and MP304 is turned off to reduce static power dissipation. Therefore, DIN is pulled low to logic 0.

G. ESD Protection Consideration

From the measurement results of previous works [1]–[4], the ESD strength of the stacked output stage with their current driving ability higher than 25 mA can be equalized up to 2 kV for HBM (human body model) and 200 V for MM (machine model) [18]. Fig. 10 shows the simplified circuit with ESD consideration through discharging path and charging path. $\mathrm{V_{DS,NMOS}}$ and $\mathrm{V_{DS,PMOS}}$ can be derived as

$$\mathrm{V_{DS,PMOS}} = \frac{\mathrm{V_{IL}} - \mathrm{GND}}{2} \tag{1}$$

$$\mathrm{V_{DS,NMOS}} = \frac{\mathrm{V_{IH}} - \mathrm{GND}}{2} \tag{2}$$

where $\mathrm{V_{IL}}$ and $\mathrm{V_{IH}}$ are set to $0.3 \times \mathrm{VDD}$ and $0.7 \times \mathrm{VDD}$, respectively [18]. Moreover, Output stage are operated in triode region. Thus, by taking above conditions and the characteristic of transistors in triode region into consideration, the size of Output stage can be estimated.

III. Dual-Path Gate-Tracking Circuit

One of the major reasons why the speed of prior mixed-voltage buffers can not run up to several hundred MHz is that the gate drives of the transistors close to the output pad can not be determined until all of the voltages are detected [13]–[16]. For instance, Vg2 of Po2 in Fig. 4 can not be defined until all of the other voltages are settled, including Vpad, Vnwell, VD25 from VDDIO detector, etc. What even worse

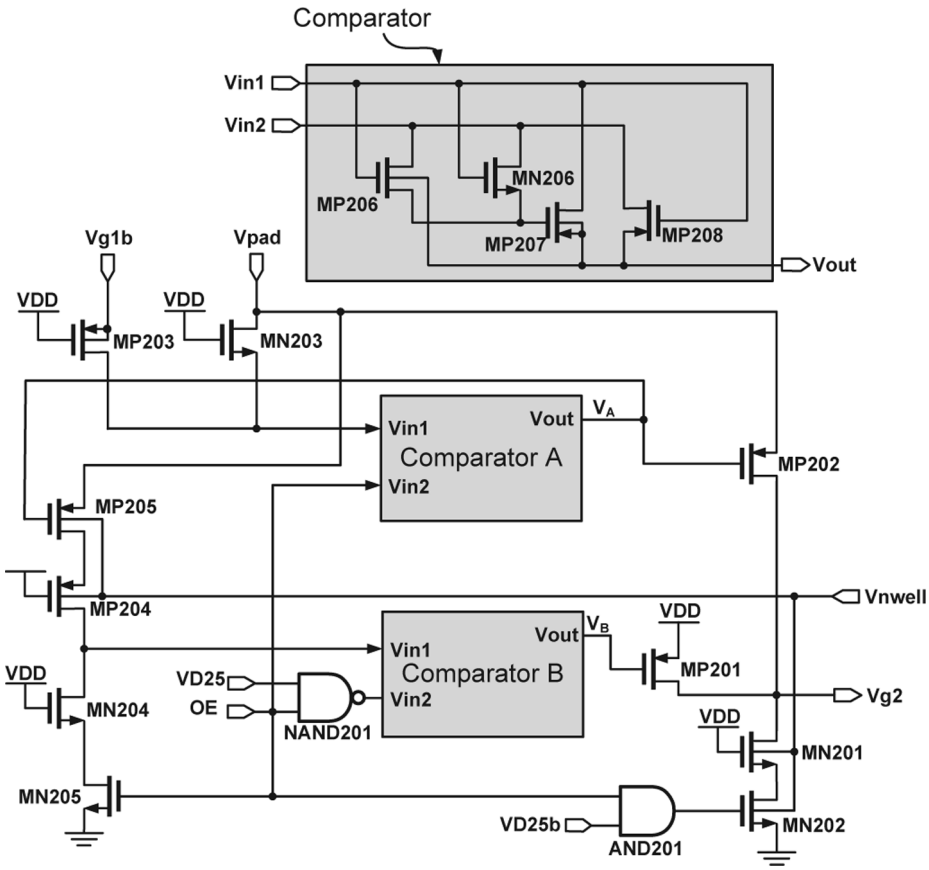

Fig. 11. Dual-path gate-tracking circuit.

is that only one signal path and certain complicated logical circuits based on a large look-up table were used in these prior works for the sake of area cost. Therefore, we propose a dual-path voltage comparison approach in this work to fasten the generation of Vg2.

Referring to Fig. 11, the schematic of Dual-path gate-tracking circuit, namely Vg2 generator, in Fig. 4 is revealed, including two Comparators, Comparator A and Comparator B. These comparators are utilized to compare two voltages, which are Vin1 and Vin2, and deliver the higher one as Vout (i.e., if Vin1 is larger than Vin2, Vout is equal to Vin1). Then, there are a total of 5 operation scenarios in Dual-path gate-tracking circuit described as follows.

A. Tx Mode and $\mathrm{VDDIO} = 2 \times \mathrm{VDD}$

When I/O buffer is in Tx mode, VDDIO is at $2 \times$ VDD, and DOUT is at logic 1. Vg1b, biased at $2 \times$ VDD generated by Vg1 generator, is fed into Vin1 of Comparator A through MP203. Besides, OE is logic 1 $(=\mathrm{VDD})$ to be fed into Vin2 of Comparator A. After comparing two voltages by Comparator A, VDD and Vg1b $(=2 \times \mathrm{VDD})$, the higher one is presented at node $\mathrm{V_A}(= 2 \times \mathrm{VDD})$ to turn off MP202. Because the $\mathrm{V_A}$ is $2 \times$ VDD, MP205 is turned off. Meanwhile, since OE is VDD, MN205 is turned on. Thus, the Vin1 of Comparator B is pulled low to 0 V. Because the VD25 is logic 1 generated by VDDIO detector, and OE is logic 1, Vin2 of Comparator B is pulled down to 0 V. After comparing two input voltages by Comparator B, $\mathrm{V_B}$ is 0 V to turn on MP201. MN202 is turned off by output of AND201 because VD25b is logic 0. Therefore, Vg2 is pulled high to VDD through MP201.

When DOUT is at logic 0 and Vpad is 0 V, MP202 is also turned off. $\mathrm{V_B}$ is 0 V to turn on MP201. Thus, Vg2 is still kept as VDD through MP201.

B. Tx Mode and $\mathrm{VDDIO} = \mathrm{VDD}$

When I/O buffer is in Tx mode, VDDIO is at VDD, and DOUT is at logic 1. Then, Vin1 of Comparator A is discharged to VDD. Besides, OE $(=\mathrm{VDD})$ is fed into Vin2 of Comparator A. That means $\mathrm{V_A}$ must be VDD to turned off MP202. At the same time, MP205 is turned off. Besides, since OE is VDD, MN205 is turned on. Thus, Vin1 of Comparator B is pulled low to 0 V. Simultaneously, since VD25 is logic 0, Vin2 of Comparator B is pulled high to VDD. Then, $\mathrm{V_B}$ must be VDD to turn off MP201. MN202 is then turned on by AND201. Therefore, Vg2 is pulled low to 0 V through MN201 and MN202.

When DOUT is at logic 0 and Vpad is 0 V, MP202 is also turned off. $\mathrm{V_B}$ is VDD to turn off MP201. Therefore, Vg2 is still 0 V.

C. Rx Mode and $\mathrm{Vpad} = 2 \times \mathrm{VDD}$

When I/O buffer is in Rx mode and Vpad is $2 \times$ VDD, Vin1 of Comparator A is discharged to '$\mathrm{VDD\text{-}Vth_{MN203}}$' through MN203. Besides, OE $(= 0\ \mathrm{V})$ is fed into Vin2 of Comparator A. Therefore, $\mathrm{V_A}$ of Comparator A becomes '$\mathrm{VDD\text{-}Vth_{MN203}}$' to turned on MP202. By AND201, MN202 must be turned off. Therefore, Vg2 is pulled high to $2 \times$ VDD through MP202.

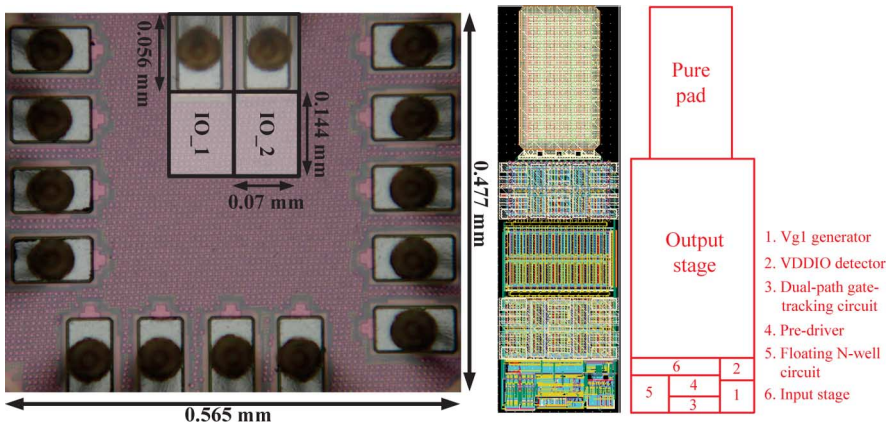

Fig. 12. Die photo of the proposed mixed-voltage I/O buffer.

D. Rx Mode and $\mathrm{Vpad} = \mathrm{VDD}$

When I/O buffer is in Rx mode and Vpad is VDD, Vin1 of Comparator A is charged to 'VDD-$\mathrm{Vth_{MN203}}$' through MN203. Besides, OE $(= 0\ \mathrm{V})$ is fed into Vin2 of Comparator A. Thus, $\mathrm{V_A}$ is 'VDD-$\mathrm{Vth_{MN203}}$' to turned on MP202. By AND201, the MN202 must be turned off. Therefore, Vg2 is pulled high to VDD through MP202.

E. Rx Mode and $\mathrm{Vpad} = 0\ \mathrm{V}$

When Vpad is 0 V, Vin1 of Comparator A is discharged to 0 V. Then, $\mathrm{V_A}$ must be pulled down to 0 V. Vin1 of Comparator B is discharged to '$\mathrm{Vthp_{MP205} + Vds_{MP204}}$' through MP205 and MP204. Therefore, $\mathrm{V_B}$ is '$\mathrm{Vthp_{MP205} + Vds_{MP204}}$' to turned on MP201. Then, Vg2 is also pulled high to VDD through MP201.

In short, not only the separation of voltage comparison using the dual-path methodology shortens the path to generate appropriate gate drives of MP202, MN202, and MP201, the look-up table required by the prior works [13]–[16] is also drastically reduced.

IV. Implementation and Measurement Results

The proposed design is implemented using a typical 90 nm CMOS process to justify the performance. Fig. 12 shows the die photo of the proposed mixed-voltage I/O buffer. The mixed-voltage I/O buffer's area is $0.07 \times 0.144\ \mathrm{mm^2}$, and a mixed-voltage I/O buffer with bounding pad's area is $0.07 \times 0.2\ \mathrm{mm^2}$. The eye diagrams of Vpad given different VDDIO are measured in Tx mode, as shown in Figs. 13 and 14. The performance of the proposed design in Tx mode is summarized in the Table III. The maximum data rate in $\mathrm{VDDIO} = 1.2\ (\mathrm{VDD})$ and $\mathrm{VDDIO} = 2.5\ \mathrm{V}$ (over $2 \times \mathrm{VDD}$) are 800 Mbps and 704 Mbps, respectively. Fig. 15 depicts the waveform of Vpad in the Rx mode. The maximum data rate of the proposed design in Rx mode is 660 Mbps. Table IV shows the comparison with several prior works. In terms of voltage modes, our design attains the same $2 \times \mathrm{VDD}$ functionality as [1], [2], and [14]. Although [15] and [16] reported sub-$3 \times \mathrm{VDD}$ tolerant capability, their data rate are relatively slow. Our design consumes only 0.09 μW and 0.78 mW in static and dynamic power, respectively, to provide 800 Mbps performance. Although this work attains the edge of speed at the expense of power consumption, the PDP (power-delay product) outperforms the second fastest work [1] very significantly.

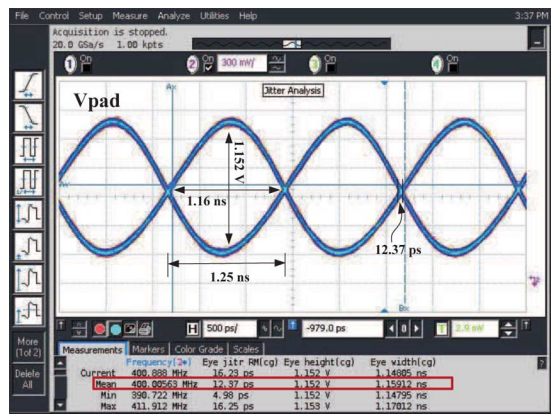

Fig. 13. The eye diagram of Vpad with $\mathrm{VDDIO} = 1.2\ \mathrm{V}$ in Tx mode.

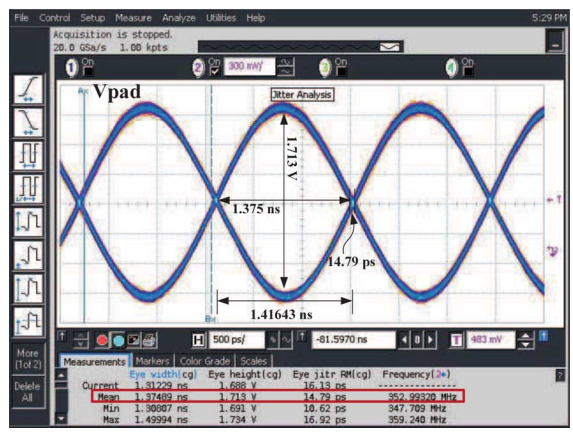

Fig. 14. The eye diagram of Vpad with $\mathrm{VDDIO} = 2.5\ \mathrm{V}$ in Tx mode.

V. Conclusion

A high speed VDD to $2 \times \mathrm{VDD}$ bidirectional mixed-voltage tolerant I/O buffer is proposed in this paper. The signal with a VDD to $2 \times \mathrm{VDD}$ swing can be transmitted and received over 660 Mbps data rate. Besides, the effects of gate-oxide overstress and the leakage current are both eliminated. A novel Dual-path

TABLE IV
PERFORMANCE CAPARISON OF MIXED-VOLTAGE I/O BUFFER WITH PRIOR WORKS

	Year	Voltage modes (V)	Maximum data rate (Mbps)	Process (μm)	Area (mm^2)	Power consumption Static/Dynamic(mW)	Power-delay product (PDP) (pJ)
This work	2011	1.2/2.5	800	0.09	0.01008	0.00009/0.78	0.975
[1]	2008	1.5/3.3	532	0.18	N/A	17.556 (Dynamic)	33
[2]	2009	1.5/3.3	266	0.13	0.0997	N/A	N/A
[14]	2010	0.9/1.2/1.8/2.5/3.3/5.0	158.4	0.35	0.0497	0.00033 (Static)	N/A
[15]	2010	0.9/1.2/1.8/3.3/5.0	100	0.18	0.04082	0.0039 (Static)	N/A
[16]	2011	0.9/1.2/1.8/3.3/5.0	250	0.18	0.044	0.017 (Static)	N/A

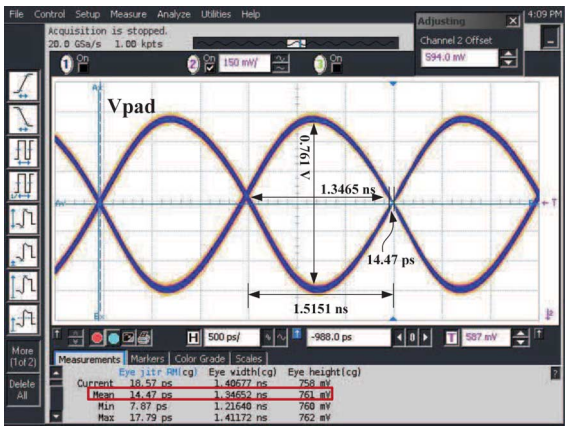

Fig. 15. The eyes diagram of the proposed design in Rx mode.

TABLE III
PERFORMANCE OF MIXED-VOLTAGE I/O BUFFER WITH DIFFERENT VDDIO IN TX MODE

VDDIO	Maximun data rate	Eye jitter	Eye height	Eye width
1.2 V	800 Mbps	12.37 ps	1.152 V	1.1591 ns
2.5 V	704 Mbps	14.79 ps	1.713 V	1.3749 ns

gate-tracking circuit is proposed to adjust gate drive of Po2 depending in different modes. All of the functions are verified through the on-silicon measurement. The maximum data rate reaches 800 Mbps, which is high enough to meet the specification of PCI-express.

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