Analysis of Calibrated On-Chip Temperature Sensor With Process Compensation for HV Chips

Chua-Chin Wang, *Senior Member, IEEE*, Wen-Je Lu, and Tsung-Yi Tsai

***Abstract*—This brief presents a wide-range temperature sensor with process compensation and nonlinear calibration for HV chip thermal monitoring. Due to a high supply voltage and a large current, HV chips are prone to overheating; thus, they require on-chip temperature sensors to monitor thermal variation. The voltage difference between the drain and source voltages of a metal–oxide–semiconductor, i.e., $V_{\rm DS}$, of HV devices is enlarged by high supply voltages, causing a severe channel length modulation effect to jeopardize the linearity of the saturation current. The proposed calibrated temperature sensors in this brief provide a nonlinear calibration function to resolve this problem. Moreover, our design reveals a process compensation capability by the proposed process variation canceler. The maximal deviation in the range of $(-40\ ^\circ\mathrm{C}, +150)\ ^\circ\mathrm{C}$ is measured to be $-2.05\ ^\circ\mathrm{C}$–$+2.06\ ^\circ\mathrm{C}$.**

***Index Terms*—Calibrated temperature sensor, channel length modulation effect, nonlinear calibration, process compensation.**

I. Introduction

HV CHIPS have been widely used in many power-related systems such as battery modules [1], motor drivers, and solar panel storage. HV chips usually encounter overheating problems caused by HVs and large currents, which may become a safety issue; therefore, they require on-chip temperature sensors to prevent thermal runaway. However, the voltage difference between the drain and source voltages of a MOS, i.e., $V_{\rm DS}$, of HV devices is larger than that of low-voltage devices such that the channel length modulation effect of MOSs will strongly affect the linearity of the saturation current. An additional critical issue is the demand of the wide-range operation temperature of certain applications. Electric vehicles, for example, require the harshest temperature range of $-40\ ^\circ$C–$+125\ ^\circ$C [1]. Temperature sensors are required to monitor the temperature of chips in applications with such a wide temperature range to prevent hazards caused by overheating problems [2]–[4].

Threshold voltage detection is a major temperature sensing theory [5]–[7]; however, the accuracy in this type of sensor is challenged in very wide ranges. Vaz *et al.* [6] proposed a temperature sensor for human body temperature monitoring, in which a large resistor is used to cancel the temperature nonlinearity components of the saturation current. However, this design was meant for low temperature ranges. Several logic-based design temperature sensors have been also proposed. Although Chung and Yang [2] proposed an all-digital temperature sensor, severe processing and nonlinear effects remained because it is difficult to detect and thus calibrate the process variation and second-order effects of MOSs in all digital circuits. A few time-domain temperature sensors have been reported [8]–[10]; however, the successive approximation algorithm requires a large area overhead. A frequency-to-digital-domain temperature sensor has been also reported [11] in which the ring oscillator is adjusted to generate a linear frequency versus temperature function, which is used to improve the linearity of the temperature sensor and to compensate for process variations. Moreover, several other high-linearity and second-order calibration methods have been reported [12]–[14]. Jeong and Ayazi [14] disclosed a process offset cancelation method by adding an identical circuit; however, nonlinear effects such as the channel length modulation effect, the body effect, and mobility remained [14]. Although many highly linear temperature sensors and nonlinear calibration methods were proposed, the channel length modulation effect of MOSs remains a challenge [2]–[17].

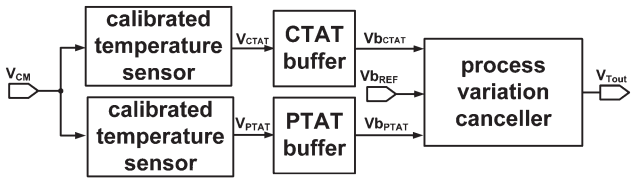

Fig. 1. Block diagram of the proposed temperature sensor.

In this brief, we propose calibrated temperature sensors with nonlinear calibration to resolve the channel length modulation effect and process variation problems. Notably, our design also considered the cancelation of the temperature variation of on-chip resistors.

II. Temperature Sensor

Fig. 1 shows the block diagram of the proposed temperature sensor composed of five major blocks including two calibrated temperature sensors, a complementary to absolute temperature (CTAT) buffer, a proportional to absolute temperature (PTAT) buffer, and a process variation canceler. The proposed calibrated temperature sensor is able to attain positive and negative temperature coefficients by adjusting the MOS ratios [14]. If the

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The authors are with the Department of Electrical Engineering, College of Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan (e-mail: ccwang@ee.nsysu.edu.tw; wen@vlsi.ee.nsysu.edu.tw; zack@vlsi.ee.nsysu.edu.tw).

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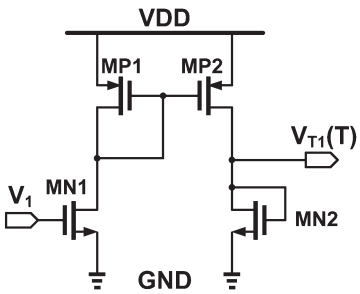

Fig. 2. Schematics of the noncalibrated temperature sensor.

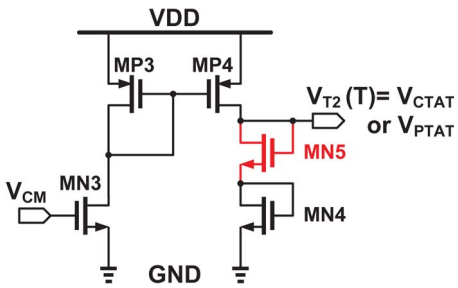

Fig. 3. Schematics of the calibrated temperature sensor.

conventional Vth detection approach is directly used, the output voltage range of the proposed calibrated temperature sensors will be limited, which in turn results in poor temperature sensitivity. The CTAT and PTAT buffers shown in Fig. 1 are used to enlarge the output range of the calibrated temperature sensors linearly. The process variation canceler is used to subtract the output voltages of calibrated temperature sensors to eliminate the common process variation. The details of these function blocks are given in the following sections.

A. Calibrated Temperature Sensor

Fig. 2 shows a schematic diagram of a previously introduced temperature sensor including two pMOSs and two nMOSs [14], i.e., the noncalibrated temperature sensor. It has a positive or negative temperature-to-voltage transfer curve attained by adjusting the lengths and widths of the MOSs. Because this method is based on threshold voltage detection, the linearity is affected by the threshold voltage, the channel length modulation effect, and the mobility variations. The channel length modulation effect of HV MOSs will significantly affect the linearity of the saturation current because $V_{\rm DS}$ is enlarged due to the HV supply. Therefore, we utilize a calibrated temperature sensor that utilizes an nMOS and a bias voltage control method, i.e., $V_{\rm CM}$, to reduce the channel length modulation effect, as shown in Fig. 3.

We recall the noncalibrated temperature sensor shown in Fig. 2, in which its output voltage is expressed as

$$V_{\rm T1}(T) = V_{\rm GS,\,MN2}(T) \tag{1}$$

where T is the absolute temperature expressed in kelvins and $V_{\rm GS,\,MN2}(T)$ is the voltage difference between the gate and source of MN2. $I_{\rm sat}(T)$ is expressed as [9], [14]

$$I_{\rm sat}(T) = \frac{1}{2}u(T)C_{\rm ox}\frac{W}{L}\left[V_{\rm GS}(T) - {\rm Vth}(T)\right]^2\left[1+\lambda V_{\rm DS}(T)\right] \tag{2}$$

where $I_{\rm sat}(T)$ is the saturation current, W is the channel width, L is the channel length, $C_{\rm ox}$ is the oxide capacitance, $u(T)$ is the mobility, $V_{\rm DS}(T)$ is the voltage difference between the drain and source of the MOS, λ is the channel length modulation coefficient, and ${\rm Vth}(T)$ is the threshold voltage. ${\rm Vth}(T)$ is defined as [9], [14]

$${\rm Vth}(T) = {\rm Vth0} - \alpha(T - T_0) \tag{3}$$

where T_0 is roughly equal to 298 K or 25 °C, Vth0 is the threshold voltage at T_0, and α is in the range of 0.5–3.0 mV/°C [12]. According to the aforementioned equations and the current mirror characteristic, $V_{\rm GS,\,MN2}(T)$ can be written as

$$V_{\rm GS,\,MN2}(T) = \omega'\lambda' \times V_{\rm GS,\,MN1}(T) - (\omega'\lambda' + 1) \times {\rm Vth0} + (\omega'\lambda' - 1) \times \alpha(T - T_0) \tag{4}$$

where ω' and λ' are equal to $\sqrt{\frac{\frac{W_{\rm MP2}}{L_{\rm MP2}}}{\frac{W_{\rm MP1}}{L_{\rm MP1}}} \times \frac{\frac{W_{\rm MN1}}{L_{\rm MN1}}}{\frac{W_{\rm MN2}}{L_{\rm MN2}}}}$ and $\sqrt{\frac{[1+\lambda V_{\rm DS,\,MP2}(T)]}{[1+\lambda V_{\rm DS,\,MP1}(T)]} \times \frac{[1+\lambda V_{\rm DS,\,MN1}(T)]}{[1+\lambda V_{\rm DS,\,MN2}(T)]}}$, respectively. λ' is the channel length modulation effect coefficient of the noncalibrated temperature sensor. Apparently, the temperature variation terms always exist in the right-hand side of the equation.

Referring to Fig. 3, although the temperature sensor was proposed previously [12], it was used to improve the linearity of the drain current by adding an extra nMOS. The design approach of this sensor for overcoming the temperature variation has never been investigated. In this brief, we rederive the functions of the temperature sensor to determine the design approach to attain the CTAT and PTAT characteristics and the channel length modulation calibration.

Again, referring to Fig. 3, $V_{\rm CM}$ is given externally, which presumes that the $V_{\rm GS}$ of MN3 is not affected by the on-chip temperature variation. The output voltage of the calibrated temperature sensor is expressed as

$$V_{\rm T2}(T) = V_{\rm GS,\,MN5}(T) + V_{\rm GS,\,MN4}(T) \tag{5}$$

where $V_{\rm GS,\,MN5}(T)$ and $V_{\rm GS,\,MN4}(T)$ are the voltage difference between the gate and source of MN5 and MN4, respectively. Similar to (4), $V_{\rm GS,\,MN5}(T)$ can be written as

$$V_{\rm GS,\,MN5}(T) = \left[V_{\rm GS,\,MN3}(T) - {\rm Vth}(T)\right] \times \omega''\lambda'' + {\rm Vth}(T) \tag{6}$$

where ω'' and λ'' can be written as $\sqrt{\frac{\frac{W_{\rm MP4}}{L_{\rm MP4}}}{\frac{W_{\rm MP3}}{L_{\rm MP3}}} \times \frac{\frac{W_{\rm MN3}}{L_{\rm MN3}}}{\frac{W_{\rm MN5}}{L_{\rm MN5}}}}$ and $\sqrt{\frac{[1+\lambda V_{\rm DS,\,MP4}(T)]}{[1+\lambda V_{\rm DS,\,MP3}(T)]} \times \frac{[1+\lambda V_{\rm DS,\,MN3}(T)]}{[1+\lambda V_{\rm DS,\,MN5}(T)]}}$, respectively.

Assume that the mobility of the nMOS is twice that of the pMOS and $V_{\rm CM} = (1/2){\rm VDD}$. If $W_{\rm MP3}/L_{\rm MP3} : W_{\rm MN3}/L_{\rm MN3} = 2:1$, then $V_{\rm GS,\,MN3}(T) \approx V_{\rm GS,\,MP3}(T)$ based on (2). Thus, ω'' is written as $\sqrt{\frac{W_{\rm MP4} \times L_{\rm MN5})}{(2W_{\rm MN5} \times L_{\rm MP4}}}$.

$V_{\mathrm{DS,\,MN3}}(T)$ is equal to $\mathrm{VDD}-[-V_{\mathrm{DS,\,MP3}}(T)]$. Thus, $V_{\mathrm{DS,\,MN3}}(T)$ and $V_{\mathrm{DS,\,MP3}}(T)$ are both equal to $\mathrm{VDD}/2$. Therefore, λ'' is simplified as $\sqrt{\frac{[1+\lambda V_{\mathrm{DS,\,MP4}}(T)]}{[1+\lambda V_{\mathrm{DS,\,MN5}}(T)]}}$, where $V_{\mathrm{DS,\,MP4}}(T)$ is equal to $V_{\mathrm{DS,\,MN5}}(T)+\Delta V_{\mathrm{DS}}(T)$, and $\Delta V_{\mathrm{DS}}(T)$ is the voltage difference between $V_{\mathrm{DS,\,MP4}}(T)$ and $V_{\mathrm{DS,\,MN5}}(T)$. λ'' is derived as $\sqrt{\frac{[1+\lambda V_{\mathrm{DS,\,MN5}}(T)]+\lambda\Delta V_{\mathrm{DS}}(T)}{[1+\lambda V_{\mathrm{DS,\,MN5}}(T)]}}$.

As a result of the inserted MN5, the supply voltage (the VDD headroom) is more evenly distributed over $V_{\mathrm{DS,\,MP4}}(T)$, $V_{\mathrm{DS,\,MN5}}(T)$, and $V_{\mathrm{DS,\,MN4}}(T)$.

- When $V_{\mathrm{CM}}=(\mathrm{VDD}/2)$ and $2(W_{\mathrm{MN3}}/L_{\mathrm{MN3}})=(W_{\mathrm{MP3}}/L_{\mathrm{MP3}})$, $V_{\mathrm{SG,MP3}}(T)\approx(\mathrm{VDD}/2)$ ($\because$ the gate and drain of MP3 is shorted).
- Since $V_{\mathrm{CM}}=\mathrm{VDD}/2$ and $V_{\mathrm{SG,MP3}}(T)\approx(\mathrm{VDD}/2)$, the gate of MP4 is driven by a reference voltage $(\mathrm{VDD}/2)$.
- MP4, MN4, and MN5 are affected by the channel length modulation effect. ($\because$ the gate and drain of the MP4 is not shorted). Thus, the respective $V_{\mathrm{DS}}(T)$ of MP4, MN5, and MN4 must be clamped to alleviate the channel length modulation effect. The parameters of our design are summarized in the following points.
- MN3, MP3, MN4, MN5, and MP4 are forced into the saturation region by tuning their individual sizes.
- Because all the MOSs of the calibrated temperature sensor are in the saturation region, $V_{\mathrm{DS,\,MN5}}(T)$ and $V_{\mathrm{DS,\,MN4}}(T)$ must be larger than $\mathrm{Vthn}(T)$. Moreover, $V_{\mathrm{DS,\,MN5}}(T)$, $V_{\mathrm{DS,\,MN4}}(T)$, and $V_{\mathrm{DS,\,MP4}}(T)$ must be larger than $V_{\mathrm{GS}}(T)-\mathrm{Vth}(T)$. ($V_{\mathrm{DS,\,MN5}}(T)+V_{\mathrm{DS,\,MN4}}(T)$ is equal to $V_{\mathrm{GS,\,MN5}}(T)+V_{\mathrm{GS,\,MN4}}(T)$, as shown in Fig. 3).
- Thus, the range of $V_{T2}(T)$ is limited in $[\mathrm{VDD}-2\mathrm{Vthn}(T)]-2\mathrm{Vthn}(T)$.
- By contrast, if the same conditions are applied to the noncalibrated temperature sensor, $V_{T1}(T)$ is limited in $[\mathrm{VDD}-\mathrm{Vthn}(T)]-\mathrm{Vthn}(T)$.
- $V_{\mathrm{T1}}(T)$ is the drain of MP2 and MN2, where the range of $V_{\mathrm{T1}}(T)$ determines the range of the $V_{\mathrm{DS}}(T)$ of MP2 and MN2. $V_{\mathrm{T2}}(T)$ is the drain of MP4 and MN5, where the range of $V_{\mathrm{T2}}(T)$ also determines the range of the $V_{\mathrm{DS}}(T)$ of MP4, MN4, and MN5.
- Thus, the voltage difference among $V_{\mathrm{DS,MP4}}(T)$, $V_{\mathrm{DS,\,MN5}}(T)$, and $V_{\mathrm{DS,\,MN4}}(T)$ is lower than that between $V_{\mathrm{DS,MP2}}(T)$ and $V_{\mathrm{DS,\,MN2}}(T)$. The proposed calibrated temperature sensor, therefore, can reduce the channel length modulation effect.

Because $\lambda\times\Delta V_{\mathrm{DS}}(T)$ is considerably smaller than $1+\lambda V_{\mathrm{DS,\,MN5}}(T)$, λ'' is close to 1. According to (6), $V_{\mathrm{GS,\,MN4}}(T)$ then becomes

$$V_{\mathrm{GS,\,MN4}}(T)=[V_{\mathrm{GS,\,MN3}}(T)-\mathrm{Vth}(T)]\omega'''\lambda'''+\mathrm{Vth}(T) \quad (7)$$

where ω''' and λ''' are equal to $\sqrt{\frac{W_{\mathrm{MP4}}\times L_{\mathrm{MN4}}}{2W_{\mathrm{MN4}}\times L_{\mathrm{MP4}}}}$ and 1, respectively. Then, $V_{T2}(T)$ is expanded into

$$V_{T2}(T)=\zeta\times V_{\mathrm{GS,\,MN3}}(T)-(\zeta-2)\times\mathrm{Vth0}+\triangle V(T) \quad (8)$$

where $\zeta=\omega''+\omega'''$. That is, the channel length modulation effect of the calibrated temperature sensor, i.e., $V_{T2}(T)$, will be canceled by using V_{CM} and MN5. $\triangle V(T)$ in (8) is quoted as

$$\triangle V(T)=(\zeta-2)\times\alpha\times(T-T_0) \quad (9)$$

where $(\zeta-2)$ and α are an adjustable coefficient term and a temperature variation term, respectively. If $(\zeta-2)>0$, the output of the temperature sensor attains a positive temperature characteristic, and vice versa. In short, the calibrated temperature sensor can be designed to possess either a negative or positive temperature coefficient by adjusting ζ. Thus, V_{CTAT} and V_{PTAT} can be written as

$$\begin{aligned}V_{\mathrm{CTAT}}=&\zeta_1\times V_{\mathrm{GS,\,MN3}}(T)-(\zeta_1-2)\times\mathrm{Vth0}\\&+(\zeta_1-2)\times\alpha\times(T-T_0)+\Delta p_{\mathrm{CTAT}} \quad (10)\\V_{\mathrm{PTAT}}=&\zeta_2\times V_{\mathrm{GS,\,MN3}}(T)-(\zeta_2-2)\times\mathrm{Vth0}\\&+(\zeta_2-2)\times\alpha\times(T-T_0)+\Delta p_{\mathrm{PTAT}} \quad (11)\end{aligned}$$

where ζ_1 and ζ_2 are the adjustable coefficients of V_{CTAT} and V_{PTAT}, respectively. ζ_1 and ζ_2 are smaller and larger than 2, respectively. Δp_{CTAT} and Δp_{PTAT} are the process variations of the V_{CTAT} and the V_{PTAT}, respectively. Δp_{CTAT} is equal to $-\Delta p_{\mathrm{PTAT}}$ [14].

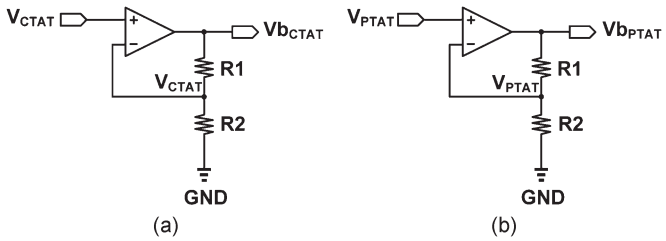

Fig. 4. Schematics of (a) CTAT buffer and (b) PTAT buffer.

B. CTAT and PTAT Buffers

Although the sensors are calibrated by the additional MN5 in Fig. 3, the output voltages of the sensors are estimated to be 10–100 mV, which cannot be directly coupled to the process variation canceler. The CTAT and PTAT buffers are needed to enlarge the outputs of the calibrated temperature sensors. Fig. 4(a) and (b) shows the schematics of the proposed CTAT and PTAT buffers, respectively. The buffers are based on the same circuitry, which is basically composed of an operational amplifier (OPA) and two polysilicon resistors. However, the temperature variation of the resistors is hostile to the accuracy of the sensors.

The temperature variation of several on-chip polysilicon resistors is simulated in the range of $[-50\,^{\circ}\mathrm{C},+160\,^{\circ}\mathrm{C}]$, as shown in Table I. The temperature variation curve of the polysilicon resistors is approximated by a field solver as

$$R(T)_{\mathrm{R_T}}\approx R_{\mathrm{T_0}}\left[1+\upsilon(T-T_0)+\upsilon'(T-T_0)^2\right] \quad (12)$$

where $R(T)_{\mathrm{R_T}}$ is the resistance of the resistor in the range from $-50\,^{\circ}\mathrm{C}$ to $+160\,^{\circ}\mathrm{C}$. Notably, υ and υ' are averagely -1.9×10^{-4} and 2.0×10^{-6}, respectively.

TABLE I
SIMULATIONS OF POLYSILICON RESISTOR CHARACTERISTICS

	R_{T_0}	υ	υ'
$R(T)_{5K}$	5K	-1.792×10^{-4}	1.991×10^{-6}
$R(T)_{25K}$	25K	-1.913×10^{-4}	1.993×10^{-6}
$R(T)_{125K}$	125K	-1.905×10^{-4}	2.053×10^{-6}
$R(T)_{625K}$	625K	-1.909×10^{-4}	2.073×10^{-6}

Note: R_{T_0} is the resistance of the resistor at T_0.

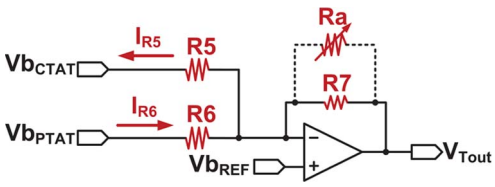

Fig. 5. Schematic of the process variation canceler.

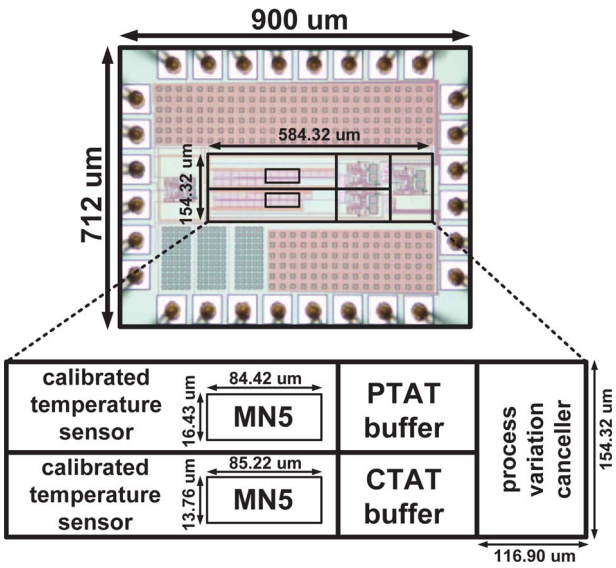

Fig. 6. Die photo of the proposed design.

$\mathrm{Vb_{CTAT}}$ in Fig. 4(a) can be written as the following equation if the process variation is taken into consideration:

$$\mathrm{Vb_{CTAT}} = \left(1 + \frac{\mathrm{R1_{T_0}}}{\mathrm{R2_{T_0}}}\right) \times V_{\mathrm{CTAT}}. \tag{13}$$

All of the resistors in this brief are polysilicon such that they have the same temperature coefficient.

C. Process Variation Canceler

Since the proposed calibrated temperature sensors are realized by the same circuit architecture, their process variation will be the same amount with opposite signs at each corner. Thus, the proposed process compensation method is to subtract the output voltages of the calibrated temperature sensors from each other to cancel the process variations. A process variation canceler with a subtraction function is carried out by a bias voltage ($\mathrm{Vb_{REF}}$) coupled to the plus input of an OPA, whereas $\mathrm{Vb_{CTAT}}$ and $\mathrm{Vb_{PTAT}}$ are both coupled to the minus input, as

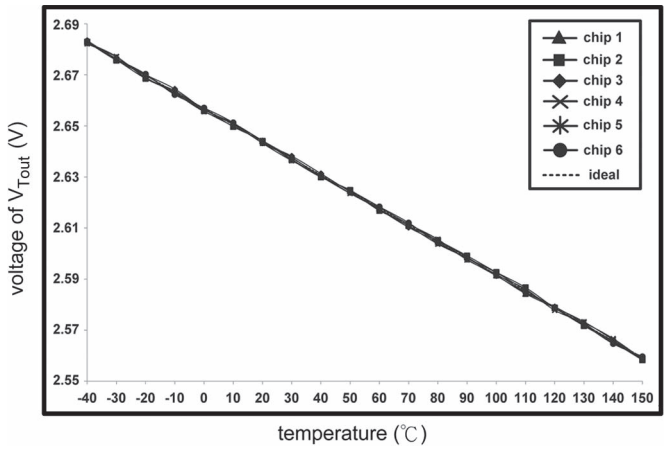

Fig. 7. Measurement results of the six chips.

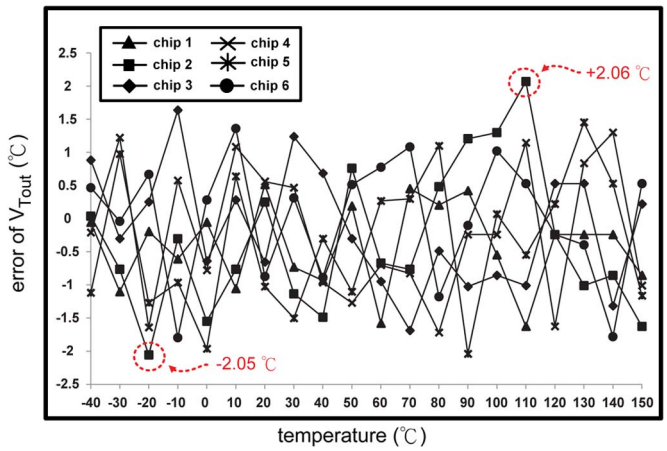

Fig. 8. Error distribution of the six chips.

shown in Fig. 5, where all the resistors are polysilicon. The currents flowing through the summing node are

$$I_{\mathrm{R5}} = \frac{\mathrm{Vb_{REF}} - \mathrm{Vb_{CTAT}}}{\mathrm{R5_{T_0}}\left[1 + \upsilon(T - T_0) + \upsilon'(T - T_0)^2\right]} \tag{14}$$

$$I_{\mathrm{R6}} = \frac{\mathrm{Vb_{PTAT}} - \mathrm{Vb_{REF}}}{\mathrm{R6_{T_0}}\left[1 + \upsilon(T - T_0) + \upsilon'(T - T_0)^2\right]} \tag{15}$$

where $\mathrm{R5_{T_0}}$ and $\mathrm{R6_{T_0}}$ are the resistances of R5 and R6 at T_0, respectively, and $\mathrm{Vb_{PTAT}} > \mathrm{Vb_{REF}} > \mathrm{Vb_{CTAT}}$ such that the current directions of I_{R5} and I_{R6} are opposite. V_{Tout} in Fig. 5 becomes

$$\begin{aligned} V_{\mathrm{Tout}} &= \kappa 1 \times (V_{\mathrm{PTAT}} + V_{\mathrm{CTAT}}) + \kappa 2 \times \mathrm{Vb_{REF}} \\ &= \kappa 1 \times [(\zeta_2 + \zeta_1) \times V_{\mathrm{GS,MN3}}(T) - (\zeta_2 + \zeta_1 - 4) \\ &\quad \times \mathrm{Vth0} + (\zeta_2 + \zeta_1 - 4) \times \alpha \times (T - T_0)] \\ &\quad + \kappa 2 \times \mathrm{Vb_{REF}} \end{aligned} \tag{16}$$

where $\kappa 1$ and $\kappa 2$ are $(-1 + (\mathrm{R1_{T_0}}/\mathrm{R2_{T_0}}))(\mathrm{R7_{T_0}}/(\mathrm{R5_{T_0}} + \mathrm{R6_{T_0}}))$ and $(1 + (\mathrm{R7_{T_0}}/\mathrm{R5_{T_0}} \parallel \mathrm{R6_{T_0}}))$, respectively, and $\mathrm{R7_{T_0}}$ is the resistance of R7 at T_0. Therefore, the process variation and the channel length modulation effect are theoretically canceled based on (16). In addition, the process variation of the canceler is dominated by the resistors. Thus, the canceler utilizes the resistors with the same characteristic to reduce the process variation. Moreover, we use an external variable resistor (Ra) to adjust the offset of the OPAs and the resistance variation of the resistors.

TABLE II
PERFORMANCE COMPARISON OF THE TEMPERATURE SENSORS

	Process (μm)	Supply Voltage (V)	Temperature Range (^{o}C)	Max. Deviation (^{o}C)	Power (mW)	Core Area (mm^2)	Normalized Temperature Deviation¶	Normalized Core Area$^\rho$
[9]	0.35	3.3	0 $\sim$ 90	-0.4/+0.6	0.0367	0.6	0.01111	4.898
[6]	0.35	3.3	35 $\sim$ 45	-0.1/+0.1	0.00011	0.084	0.02000	0.686
[7]	0.35	3.3	5 $\sim$ 80	-1.3/+1.3	15.5	0.049	0.03466	0.400
[2]	0.065	1	0 $\sim$ 60	-5.1/+3.4	0.15	0.01	0.14166	2.367
[10]	0.13	1.65	0 $\sim$ 100	-4/+4	0.1	0.12	0.08000	7.100
[13]	0.032	1	5 $\sim$ 100	-1.95/+1.95	N/A	0.01	0.04105	9.766
[5]	AMI 0.5	3	-40 $\sim$ 100	-2.5/+2.5	0.318	0.63	0.03571	2.520
[11]	0.065	1	0 $\sim$ 110	-1.5/+1.5	0.5	0.008	0.02727	1.893
[3]	0.7	5.5	-70 $\sim$ 130	-0.25/+0.25	0.1375	4.5	0.00250	9.183
[4]	0.7	5.5	-55 $\sim$ 125	-0.1/+0.1	0.4125	4.5	0.00111	9.183
[15]	0.16	1.8	-55 $\sim$ 200	-0.4/+0.4	0.04	0.1	0.00313	3.906
[16]	0.16	1.2	-40 $\sim$ 125	-0.4/+0.4	0.6	0.085	0.00484	3.320
This work	0.25*	5	-40 $\sim$ 150	-2.05/+2.06	0.384	0.09	0.02163	1.440

Note: ¶: Normalized Temperature Deviation = $\frac{\text{Max. Deviation}}{\text{Temperature Range}}$; $^\rho$: Normalized Core Area = $\frac{\text{Core Area}}{\text{Process}^2}$; *: HV process

III. IMPLEMENTATION AND MEASUREMENT RESULTS

Fig. 6 shows the die photo of this brief, where the core area of the proposed temperature sensor is 0.09 mm^2. The area of the process variation canceler is 116.90×154.32 μm^2. The area overheads of the nonlinear calibration and the process compensation are only 2.8% and 20%, respectively. Six different chips are measured to justify the linearity of voltage versus temperature, as shown in Fig. 7. Fig. 8 summarizes the deviation distribution of the six chips. In the range from -40 °C to 150 °C, the worst deviation is -2.05 °C–$+2.06$ °C. The performance comparison of the proposed design and several prior works is tabulated in Table II. Among those sensors for wide temperature range sensing, i.e., in [3]–[5], [15], [16], and in this brief in Table II, our design has the smallest normalized core area, and it is the only sensor fabricated by an HV CMOS process. Although the performance of our design will be slightly affected by voltage variation, this problem can be resolved by using accurate supply voltages with regulators.

IV. CONCLUSION

In this brief, the calibrated temperature sensor has attained process compensation by using a process variation canceler. In addition, the channel length modulation effect is also significantly reduced by using MN5 and $V_{\rm CM}$. The calibrated temperature sensor can be tuned to possess either a negative or positive temperature coefficient by adjusting ζ. The worst case deviation of the proposed three temperature sensors is only 1.08% with the penalty of acceptable area overheads. Notably, this brief has been the only solution realized on an HV process so far.

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