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# Wide-range CTAT and PTAT sensors with second-order calibration for on-chip thermal monitoring



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## ABSTRACT

This paper presents wide-range complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) sensors with second-order calibration for on-chip thermal monitoring. Particularly, a current mirror and an n-well resistor are used in these sensors to eliminate the second-order term of the temperature coefficient to linearize the transfer function between the output voltage and the temperature. The proposed CTAT and PTAT sensors are implemented on silicon using a typical 0.18  $\mu\text{m}$  CMOS process. The core area of the CTAT and PTAT sensors is 0.0125 mm<sup>2</sup> and 0.0074 mm<sup>2</sup>, respectively. In the range from  $-55\text{ }^{\circ}\text{C}$  to  $155\text{ }^{\circ}\text{C}$ , the worst deviation of the CTAT and PTAT temperature sensors is measured to be  $-3.75\text{ }^{\circ}\text{C}$  to  $+3.34\text{ }^{\circ}\text{C}$  and  $-3.73\text{ }^{\circ}\text{C}$  to  $+3.85\text{ }^{\circ}\text{C}$ , respectively. The maximum non-linearity reduction of the CTAT and PTAT sensors is 59.84% and 87.48%, respectively, by the proposed second-order calibration. Notably, the overhead area of the CTAT and PTAT sensors is only 0.64% and 1.08%, respectively.

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## 1. Introduction

It is well known that more transistors have been integrated in a chip by using advanced CMOS technologies. When many transistors are integrated and realized on a single die, the power density as well as the temperature will rise inevitably. Moreover, the chip with high switching activities will generate massive heat (namely hot spot) [1]. Another critical issue is the range of the temperature. The harshest temperature range is demanded by electrical vehicles (EV) and military equipments, which are  $-40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$  and  $-55\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , respectively [2–4]. Temperature sensors are then required to monitor the temperature of those chips in these applications in such a wide temperature range to ensure that no hazards would be caused by over heat problems.

Many prior temperature sensors relied on threshold voltage detection to estimate the temperature [5–8]. The accuracy in a very wide range is still a challenge regarding on-chip temperature sensing. Vaz et al. proposed a temperature sensor for human body temperature monitoring, where a large resistor is used to cancel temperature non-linearity components of the saturation current [7]. However, this design was meant for low temperature range. Several logic-based design temperature sensors have also been proposed [1,9]. Chung and Yang proposed an all-digital temperature sensor, where serious

process and non-linear effects still exist [1]. The reason is that the process variation and second-order effects of MOSs in all digital circuits are hard to be detected and then calibrated. A few time-domain temperature sensors were also reported [10–13]. Chen et al. proposed a time-domain temperature sensor based on a successive approximation algorithm [10]. The successive approximation algorithm, however, costs a large area overhead. Meanwhile, the high linearity and second-order effects calibration methods were reported [14–18]. Lin et al. proposed a non-linear calibration method by isolating body effect. This design, however, did not consider the process variation [14]. Jeong and Ayazi disclosed a process offset cancellation method by applying an identical circuit to realize temperature sensors [17]. The reported process compensation and second-order effects calibrated methods usually need a large area to realize compensation and calibration circuits [10–18]. Many low-cost calibration methods were also proposed [19–21]. Fisk and Hasan showed a method using the correlation between pinch-based resistance and substrate bipolar temperature gradient to carry out process-compensation [20]. Besides, Souri et al. also proposed high accuracy and low-power temperature sensors [22,23], where silicon on insulator (SOI) process was used to attain a much wider temperature range and low power consumption [22]. Another prior design used dynamic threshold MOSTs (DTMOSTs) and an inverter-based second-order zoom analog-to-digital converter (ADC) to achieve high accuracy and low power [23]. However, the SOI process, DTMOSTs, and the other prior calibration technologies must pay high die area and cost [14–26].

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In this study, we propose complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) sensors with low-cost second-order calibration to resolve all the mentioned problems. By using the proposed second-order calibrated CTAT and PTAT sensors consisting of a current mirror and an n-well resistor, the linearity can be enhanced.

## 2. Wide-range temperature sensor

Fig. 1(a) shows the schematic of the non-calibrated temperature sensor composed of 2 PMOSs and 2 NMOSs [15]. The non-calibrated temperature sensor will attain a positive or negative T-to-V (temperature-to-voltage) transfer curve by adjusting length and width of MOSs. Since this method is based on threshold voltage detection, the linearity of temperature sensors is affected by threshold voltage and mobility variations. Particularly, a significant second-order effect has been well known to exist between the saturation current of MOSs and the temperature. A simple thought is that the linearity of the transfer curve can be more linearized if this second-order effect is reduced or even cancelled. Therefore, we propose a second-order calibrated

temperature sensor, which utilizes an n-well resistor to calibrate the second-order effect.

### 2.1. Theory of second-order temperature calibration

Fig. 1(b) shows the second-order calibrated temperature sensor, which is composed of 2 PMOSs, 2 NMOSs, and an n-well resistor. The output voltage of the proposed temperature sensor is expressed as

$$V_{out}(T) = V_{GS4}(T) + I_{sat}(T)R(T) \tag{1}$$

where  $T$  is the absolute temperature in degrees of Kelvin,  $V_{GS4}(T)$  is the voltage difference between gate and source voltage of M4 with

**Table 1**  
Simulations of n-well resistor characteristic.

	$R_0$	$\gamma$	$\gamma'$
$R(T)_{5\text{ K}}$	5 K	$2.905 \times 10^{-3}$	$1.321 \times 10^{-5}$
$R(T)_{25\text{ K}}$	25 K	$2.905 \times 10^{-3}$	$1.421 \times 10^{-5}$
$R(T)_{125\text{ K}}$	125 K	$2.906 \times 10^{-3}$	$1.327 \times 10^{-5}$
$R(T)_{625\text{ K}}$	625 K	$2.911 \times 10^{-3}$	$1.320 \times 10^{-5}$

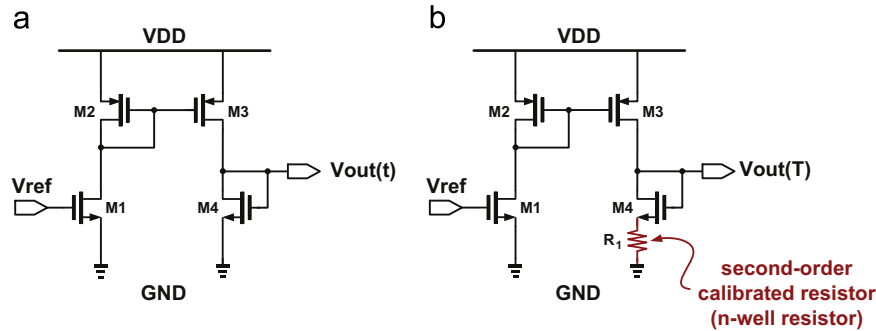


Fig. 1. Schematics of (a) non-calibrated temperature sensor, and (b) second-order effects calibrated temperature sensor.

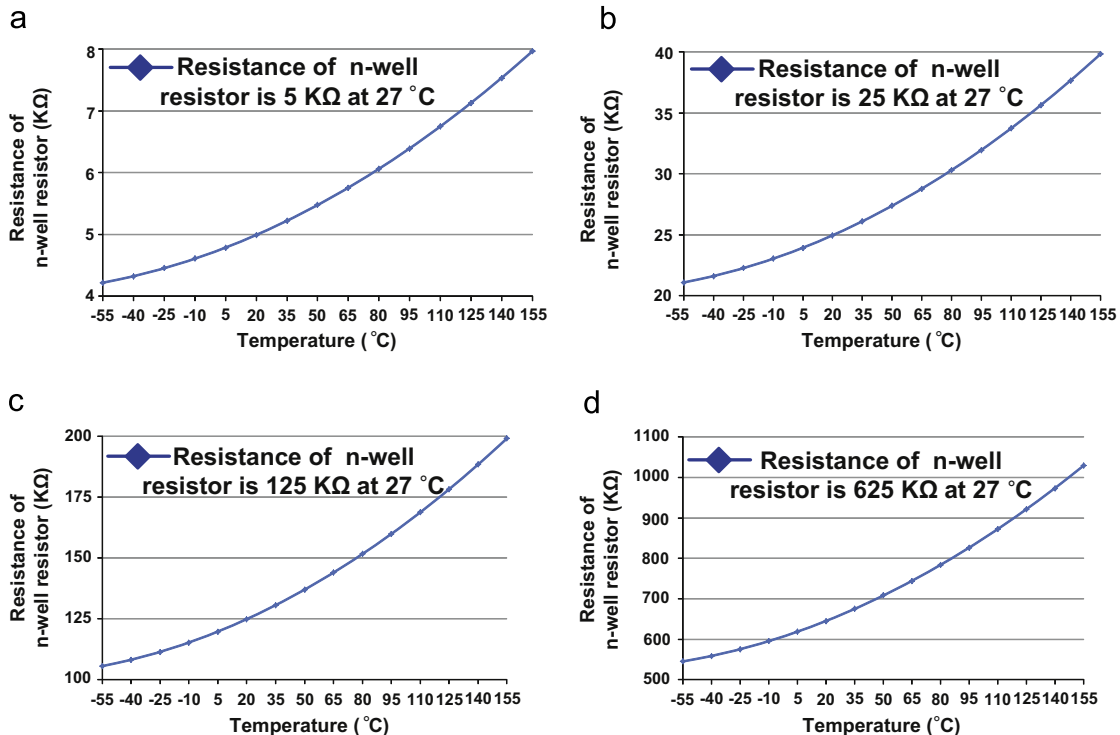


Fig. 2. Simulations of an n-well resistor characteristic curve (a) resistance=5 K Ω, (b) resistance=25 K Ω, (c) resistance=125 K Ω, and (d) resistance=625 K Ω.

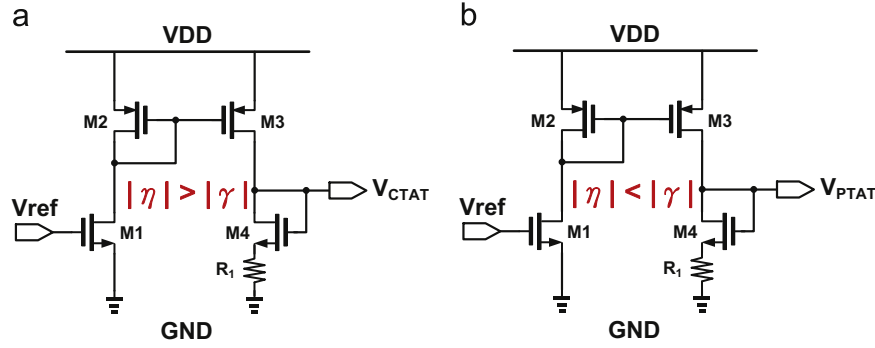


Fig. 3. Schematics of (a) second-order calibrated CTAT sensor, and (b) second-order effects calibrated PTAT sensor.

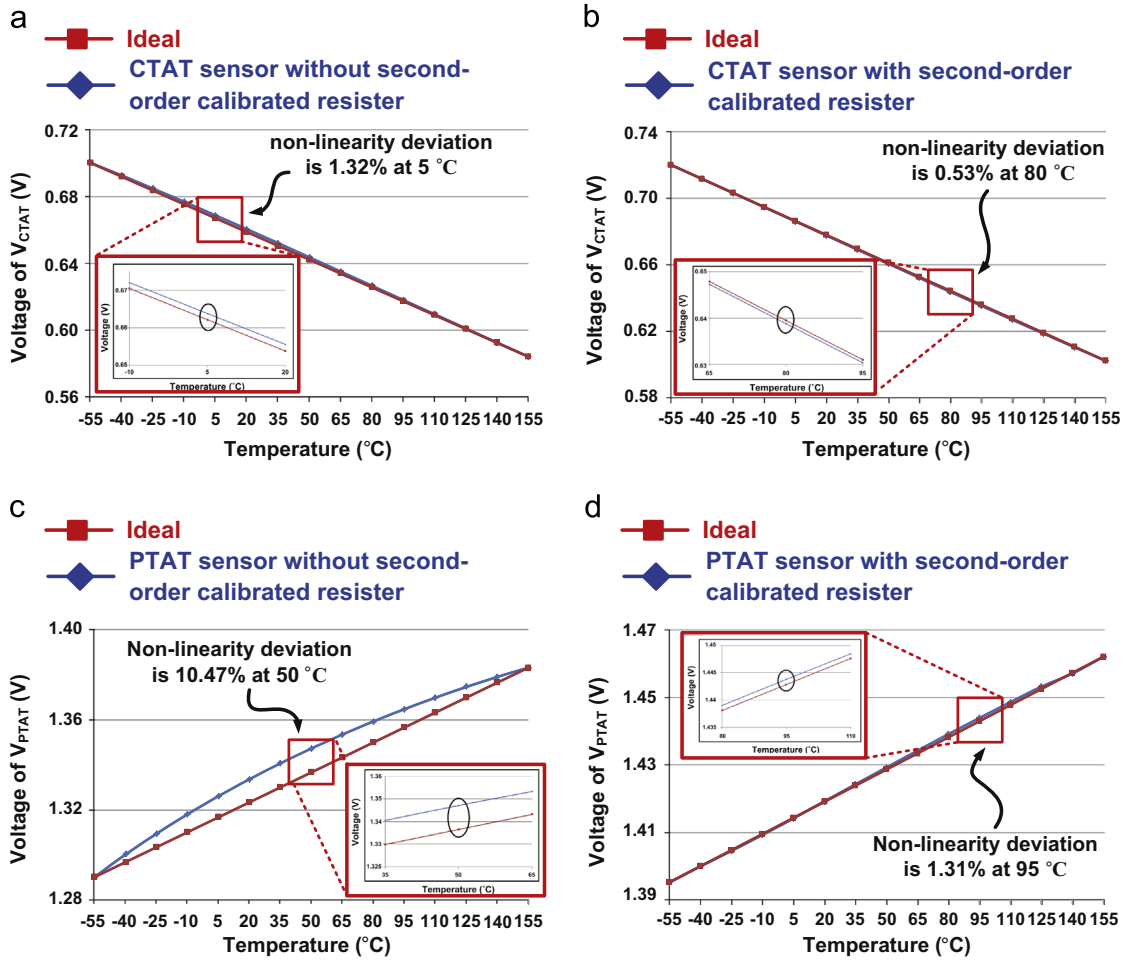


Fig. 4. Simulations of (a) non-calibrated CTAT sensor, (b) second-order calibrated CTAT sensor, (c) non-calibrated PTAT sensor, and (d) second-order calibrated PTAT sensor.

temperature variation,  $I_{\text{sat}}(T)$  is the saturation current in M4,  $R(T)$  is the resistance of the n-well resistor.  $I_{\text{sat}}(T)$  is expressed as follows [6].

$$I_{\text{sat}}(T) = \frac{1}{2} u(T) C_{\text{ox}} \frac{W}{L} [V_{\text{GS4}}(T) - V_{\text{th}}(T)]^2 \quad (2)$$

where  $W$  is the channel width of M4,  $L$  is the channel length,  $C_{\text{ox}}$  is the oxide capacitance,  $u(T)$  is the mobility, and  $V_{\text{th}}(T)$  is the threshold voltage.  $u(T)$  and  $V_{\text{th}}(T)$  are defined as follows [6]:

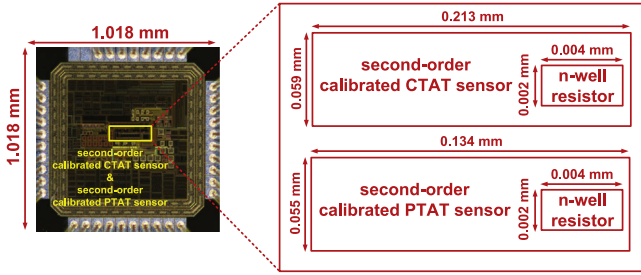
$$u(T) = u_0 \left( \frac{T}{T_0} \right)^{\text{UTE}} \quad (3)$$

$$V_{\text{th}}(T) = V_{\text{th}0} - \alpha(T - T_0) \quad (4)$$

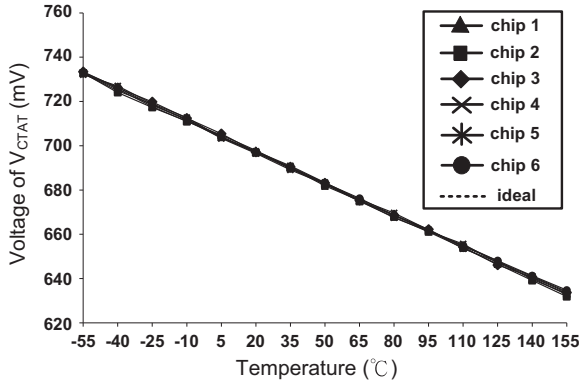
where  $\alpha$  can be written as  $\frac{1}{T_0}(KT1 + \frac{KT1L}{L_{\text{eff}}} + KT2 \times V_{\text{BS}})$ ,  $T_0$  is roughly equal to 298°K or 25 °C, UTE is a negative temperature coefficient of the mobility,  $V_{\text{th}0}$  is the threshold voltage at  $T_0$ ,  $u_0$  is the mobility at  $T_0$ ,  $KT1$  is the temperature coefficient of the threshold voltage,  $KT1L$  is the temperature coefficient of channel length,  $KT2$  is a body-bias coefficient of the threshold voltage with temperature variation,  $V_{\text{BS}}$  is the voltage difference between bulk and source voltage of M4. Notably, UTE is between  $-1.2$  and  $-2.0$ , and  $\alpha$  is in the range of  $0.5 - -3.0$  mV/°C [10]. According to the above equations and the current mirror characteristic, when all MOSs are saturated,  $I_{D1}$  and  $I_{D4}$

**Table 2**  
Calibration results at CTAT and PTAT sensors.

	Non-calibrated results	Calibrated results	Linearity improvement	Overhead area
CTAT	sensor	1.32%	0.53%	59.84%
0.64%				
PTAT	sensor	10.47%	1.31%	87.48%
1.08%				



**Fig. 5.** Die photo of the proposed CTAT and PTAT sensors.



**Fig. 6.** Measurement results of the proposed CTAT sensor.

can be written as

$$\frac{I_{D1}}{I_{D4}} = \frac{W_2}{L_2} \times \frac{W_1}{L_1} \times \frac{W_3}{L_3} \times \frac{W_4}{L_4} \times \frac{V_{GS1} - V_{th}(T)}{V_{GS4}(T) - V_{th}(T)} \quad (5)$$

$$\frac{\frac{1}{2}u(T)C_{ox}\frac{W_1}{L_1}[V_{GS1} - V_{th}(T)]^2}{\frac{1}{2}u(T)C_{ox}\frac{W_4}{L_4}[V_{GS4}(T) - V_{th}(T)]^2} = \frac{W_2}{L_2} \times \frac{W_3}{L_3} \times \frac{W_4}{L_4} \quad (6)$$

Based on Eqs. (5) and (6),  $V_{GS4}(T)$  can be written as

$$V_{GS4}(T) = \omega \times (V_{GS1} - V_{th0}) + V_{th0} + \Delta V_{GS4}(T) \quad (7)$$

where  $\omega$  is  $\sqrt{\frac{W_3}{L_3} \times \frac{W_1}{L_1} \times \frac{W_2}{L_2} \times \frac{L_4}{W_4}}$  and  $\Delta V_{GS4}(T)$  is  $(\omega - 1) \times \alpha(T - T_0)$ . If  $V_{GS1}$  is a constant value and  $\omega \approx 1$ ,  $\Delta V_{GS4}(T)$  is almost equal to 0.  $V_{GS4}(T)$  then almost becomes a constant as follows:

$$V_{GS4}(T) \cong \omega \times (V_{GS1} - V_{th0}) + V_{th0} \quad (8)$$

By Eqs. (2)–(4),  $I_{sat}(T)$  is derived as

$$I_{sat}(T) = \frac{1}{2}\beta_0[V_C + \alpha(T - T_0)]^2 \left(\frac{T}{T_0}\right)^{UTE} \quad (9)$$

where  $\beta_0$  is  $u_0 \times C_{ox} \frac{W}{L}$  and  $V_C$  is  $V_{GS4}(T) - V_{th0}$ . Then, we use Taylor series to approximate  $I_{sat}(T)$

$$I_{sat}(T) \cong I_0[1 + \eta(T - T_0) + \eta'(T - T_0)^2] \quad (10)$$

where  $I_0$  is  $\frac{1}{2}\beta_0 V_C^2$ ,  $\eta$  equals to  $\left(\frac{2\alpha}{V_C} + \frac{2UTE}{596}\right)$ , and  $\eta'$  becomes  $\left(\frac{\alpha^2}{V_C^2} + \frac{2\alpha UTE}{298V_C} + \frac{2UTE(UTE-1)}{4 \times 298^2}\right)$ . Notably,  $\eta$  and  $\eta'$  are negative coefficients. The best strategy to linearize Eq. (10) is to find a way to cancel the right-most term. Meanwhile, cost (area) is always a concern for the sensors to be physically used. Therefore, we utilize on-chip resistors, which also have a similar second-order effect vs. temperature, to carry out the cancellation of the right-most term in Eq. (10). The resistance vs. temperature variation of several n-well resistors is simulated in range of  $[-55^\circ\text{C}; +155^\circ\text{C}]$ , as shown in Fig. 2 and Table 1. The resistance characteristic of the n-well resistors, based on these simulations, can be approximated as

$$R(T) = R_0[1 + \gamma(T - T_0) + \gamma'(T - T_0)^2] \quad (11)$$

where  $R_0$  is the resistance of the n-well resistor at  $T_0$ , and  $\gamma$  and  $\gamma'$  are the first-order and the second-order temperature coefficients thereof, respectively. Thus,  $I_{sat}(T) \times R(T)$  is simplified as the following equation owing to the fact that  $\gamma$ ,  $\gamma'$ ,  $\eta$ , and  $\eta'$  are always very small

$$I_{sat}(T) \times R(T) \cong I_0 R_0[1 + \eta(T - T_0) + \eta'(T - T_0)^2 + \gamma(T - T_0) + \gamma'(T - T_0)^2] \quad (12)$$

$\gamma$  and  $\gamma'$  of the 0.18  $\mu\text{m}$  CMOS process are  $2.90 \times 10^{-3}$  and  $1.32 \times 10^{-5}$ , respectively, as shown in Table 1. According to Eqs. (8) and (9), if  $\omega$  is 1.2,  $V_{ref}$  is 1.2 V, and  $V_{th0}$  is 0.6 V,  $\eta$  and  $\eta'$  are derived as  $-4.02 \times 10^{-3}$  and  $-1.34 \times 10^{-5}$ , respectively. Thus,  $\gamma'$  is almost equal to  $-\eta'$  such that the second-order terms are canceled to linearized  $V_{out}(T)$ . Thus, Eq. (12) is derived based on this assumption

$$I_{sat}(T) \times R(T) \cong I_0 R_0[1 + \eta(T - T_0) + \gamma(T - T_0)] \quad (13)$$

$$V_{out}(T) = V_{GS4}(T) + I_0 R_0[1 + \eta(T - T_0) + \gamma(T - T_0)] \quad (14)$$

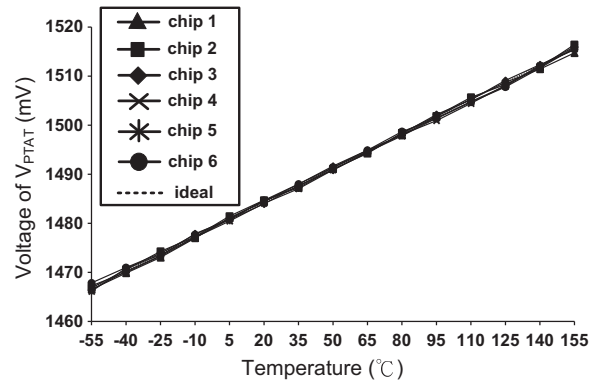
The temperature coefficient of  $V_{out}(T)$  becomes as follows:

$$\frac{\partial}{\partial T}(V_{out}(T)) = I_0 R_0(\eta + \gamma) \quad (15)$$

Therefore, the output of the second-order calibrated temperature sensor,  $V_{out}(T)$ , will become a first-order (linear) function vs. temperature.

In other words, by adjusting the resistance of the n-well resistor, an appropriate second-order positive temperature coefficient ( $\gamma'$ ) of the n-well resistor will be attained to cancel the second-order effects ( $\eta'$ ) of M4.

Besides, other major non-ideal effects of the second-order calibrated temperature sensor are channel length modulation and body effect. The channel length modulation affects the mismatch of the current mirror. Notably, adding the n-well resistor reduces the individual drain-source voltage drops of M3 and M4 such that the channel length modulation of M3 and M4 is suppressed. Besides, the substrates of all MOSs are connected to their individual own sources in the second-order calibrated temperature



**Fig. 7.** Measurement results of the proposed PTAT sensor.

sensor. Thus, the body effect of the second-order calibrated temperature sensor will not be a problem. Besides, another serious problem is process variation, which causes various output offsets of those Vth-based temperature sensors given different processes [5–7,14,15,17,21]. Thanks to the linearity feature calibrated by the second order effect cancellation, we can apply the one-point calibration method to calibrate the output offsets of the proposed design at different process corners [17].

2.2. Second-order calibrated CTAT and PTAT sensors

Based on the previous second-order calibration method, the schematics of the second-order calibrated CTAT and PTAT sensors are shown in Fig. 3(a) and (b), respectively. According to Eq. (14),  $\eta$  and  $\gamma$  are negative and positive temperature coefficients, respectively. If  $|\eta| > |\gamma|$ , the output of the temperature sensor attains

negative temperature characteristic and vice versa. The temperature characteristic of the second-order calibrated temperature sensor is given as follows.

If  $|\eta| > |\gamma|$ , it is the same as follows:

$$-\left(\frac{2\alpha}{(V_{GS4}(T) - V_{th0})} + \frac{2UTE}{596}\right) > \gamma \tag{16}$$

Eq. (16) is derived as follows based on Eq. (8).

$$\frac{1}{\omega} < \left(-\gamma - \frac{2UTE}{596}\right) \left(\frac{V_{GS1} - V_{th0}}{2\alpha}\right) \tag{17}$$

Therefore, the output of the second-order calibrated temperature sensor shows a negative temperature characteristic. By contrast, if  $|\eta| < |\gamma|$ , the equation becomes as follows:

$$\frac{1}{\omega} > \left(-\gamma - \frac{2UTE}{596}\right) \left(\frac{V_{GS1} - V_{th0}}{2\alpha}\right) \tag{18}$$

Thus, the output of the second-order calibrated temperature sensor attains a positive temperature coefficient. In summary, the second-order calibrated temperature sensor can be designed to possess either a negative or a positive temperature coefficient by adjusting  $\omega$ . Notably, the  $\left(-\gamma - \frac{2UTE}{596}\right) \left(\frac{V_{GS1} - V_{th0}}{2\alpha}\right)$  equals to 1.07. According to Eqs. (17) and (18), the valid  $\omega$  will be in the range between 0.9 and 1.2.

3. Implementation and measurement results

In this work, the proposed CTAT and PTAT sensors are implemented using a typical 0.18  $\mu\text{m}$  CMOS process. Fig. 4(a) and (b) shows the non-calibration and calibration simulation results of the proposed CTAT sensor, respectively, while Fig. 4(c) and (d) is those of the proposed PTAT sensor. Table 2 compares the non-calibrated and calibrated simulation results, where the maximum non-linearity reduction of the CTAT and PTAT sensors are 59.84% and 87.48%, respectively. Fig. 5 shows the die photo, where the core areas of the proposed CTAT and PTAT sensors is only 0.0125  $\text{mm}^2$  and 0.0074  $\text{mm}^2$ , respectively. The overhead area of the proposed CTAT and PTAT sensors are only 0.64% and 1.08%, respectively. Six different dies of the proposed CTAT and PTAT sensors are measured, as shown in Figs. 6 and 7, respectively. Figs. 8 and 9 summarize the deviation distributions of the proposed CTAT and PTAT sensors, respectively. In the range from  $-55^\circ\text{C}$  to  $155^\circ\text{C}$ , the worst deviations of our CTAT and PTAT sensors are  $-3.75^\circ\text{C}$  to  $+3.34^\circ\text{C}$  and  $-3.73^\circ\text{C}$  to  $+3.85^\circ\text{C}$ , respectively. The performance comparison of the proposed design and several prior works is tabulated in Table 3. Among those designs to cover  $100^\circ\text{C}$  temperature sensing range, i.e., [13,6,21], and our works, our CTAT sensor and PTAT sensor attain the second smallest normalized temperature deviation and the fourth.

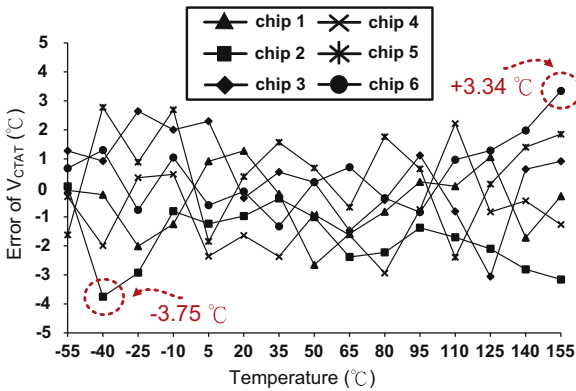


Fig. 8. Error distribution of the proposed CTAT sensor.

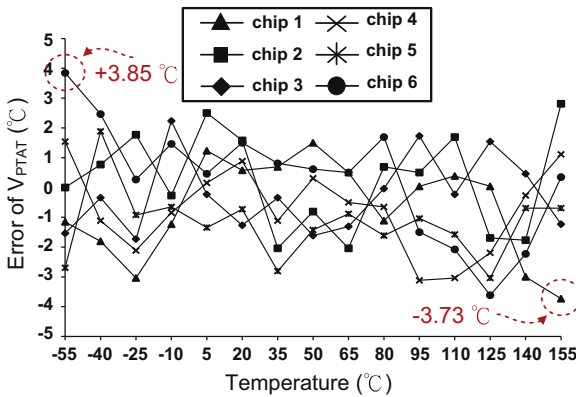


Fig. 9. Error distribution of the proposed PTAT sensor.

Table 3 Performance comparison of temperature sensors.

	[13]	[16]	[6]	[21]	[22]	The proposed CTAT sensor	The proposed PTAT sensor
Year	2012	2012	2013	2013	2013	2014	2014
Process ( $\mu\text{m}$ )	0.13	0.032	AMI 0.5	0.09	SOI 0.16	0.18	0.18
Supply voltage (V)	1.65	1	3	1.5	1.8	1.8	1.8
Temperature range ( $^\circ\text{C}$ )	0–100	5–100	–40 to 100	–55 to 105	–55 to 200	–55 to 155	–55 to 155
Inaccuracy ( $^\circ\text{C}$ )	–4/+4	–1.95/+1.95	–2.5/+2.5	–3.5/+3.5	–0.4/+0.4	–3.73/+3.34 <sup>a</sup>	–3.73/+3.85 <sup>a</sup>
Core area ( $\text{mm}^2$ )	0.12	0.01	0.63	1.058	0.1	0.0125 <sup>b</sup>	0.0074 <sup>b</sup>
Normalized temperature deviation <sup>c</sup>	0.08000	0.04105	0.03571	0.04375	0.00314	0.03376	0.03609

<sup>a</sup> No any extra calibration points.

<sup>b</sup> Only temperature sensor.

<sup>c</sup> Normalized temperature deviation =  $\frac{\text{Inaccuracy}}{\text{temperature range}}$

#### 4. Conclusion

The proposed CTAT and PTAT sensors are calibrated by using a current mirror and an n-well resistor to eliminate the second-order term of the temperature coefficient. Thus, the proposed CTAT and PTAT sensors can be used in a wide temperature range ( $-55^{\circ}\text{C}$  to  $155^{\circ}\text{C}$ ). The overhead area of the proposed CTAT and PTAT sensors, however, is only 0.64% and 1.08%, respectively. Besides, the same circuit architecture is used to carry out the CTAT and PTAT sensors to attain positive or negative temperature characteristics depending on the demand. Notably, the temperature range of proposed CTAT and PTAT sensors is currently known to be the widest to date.

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