0.7 % error rate 3A bidirectional current sensor using high voltage CMOS process

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A R T I C L E   I N F O

Keywords:
High-voltage (HV)
Bidirectional sensing
Input voltage range
Current sensor
Sensing error

A B S T R A C T

This investigation demonstrates a high-accuracy bidirectional high-voltage (HV) current sensor fabricated using CMOS technology. Besides Noise filter, Sense stage, and Controller, the proposed sensor is featured with a Switching Network composed of transmission gates, which is able to steer the direction of the current for bidirectional sensing. A digital feedback loop comprises Controller generating a pair of digital signals to Switching Network such that the direction of the current is detected real-time. The area of the proposed sensor on silicon is 1173 × 664 μm² fabricated by 0.5 μm high-voltage CMOS process. The sensing voltage error is 0.7% by physical measurements, where the input voltage range is 8–14 V, and the current sensing range is -3 – 3 A.

1. Introduction

In any power system, the bidirectional current detection is very important for safety [1]. Traditional current sensors are found very hard to detect the bidirectional current in real-time operations such that detecting the bidirectional large current with high accuracy attracts strong attention [2–5]. Many researchers have reported several current sensor designs to resolve this issue, e.g. Refs. [6–8], basically using a low-resistance resistor as a sensing resistor in series with the load and then detecting the voltage drop thereof. Although the low-resistance resistors means to improve efficiency and accuracy, the intrinsic resistance variation results in large input offset to amplifiers [9]. Besides, to the best of our survey, all of the existing current sensors are focused on the detection of only one current direction. That is, they are not able to detect the discharge and charge currents of a battery system in run time, unless two sensors are used simultaneously. To resolve all the mentioned problems, a bidirectional current sensor using the fully-differential amplifier (FDA) with digital auxiliary circuits is proposed in this investigation. More specifically, the proposed sensor is featured with a digital feedback loop, where the sensed output voltage is sampled and converted into digital codes to drive Switching Network composed of transmission gates such that the correct current direction can be detected. The Switching Network not only correctly selects the direction of the current, but also elevates the accuracy higher than our previous work in Ref. [10]. With the assistance of external micro-controller, a simple FSM (finite state machine) is realized to automatically proceed the current sensing for charge-discharge-charge cyclic operations. The design was realized on silicon prototype and justified by physical measurements to sense the voltage from 8 to 14 V, and current range from −3 A to 3 A. Most important of all is that only 0.7% error is found to prove the accuracy of the proposed design.

2. High-voltage bidirectional current sensor

The block diagram of the proposed HV bidirectional current sensor is shown in Fig. 1, including a current sensing resistor (Rcs), a Noise filter, a Switching Network, a Sense Stage, Rout, an external micro-controller (MC), and a Controller. Fig. 2 shows the schematic of the proposed HV bidirectional current sensor, where all the details will be given in following text.

2.1. Operation of the proposed HV bidirectional current sensing

A very small sensing voltage (Vcs) is generated by Ics via Rcs, where Rcs is a small resistor, as shown in Fig. 1. Noise filter comprising 4 Rnf, and a Cnf rejects unwanted high-frequency noise. I acts like a low-pass filter with a 3-dB bandwidth defined in Eqn. (1).

\[ f_{-3db} = \frac{1}{2\pi \cdot Rnf \cdot Cnf} \] (1)
FDA in Sense Stage of Fig. 2 attains a virtual short across the input terminals (namely, $V_{ip} = V_{in}$) [10]. The drain currents of the M301 and M302 are then proportional to $(V_{csp} - V_{ip})/2R_{NF}$ and $(V_{csn} - V_{ip})/2R_{NF}$, respectively, assuming the transmission gates are ideal. Current mirror carries out the current subtraction to generate $\Delta I = I_1 - I_2$, whereupon $\Delta I$ is converted into an output voltage, $V_{cso}$, by $R_{out}$. The proposed sensing system’s operations are classified into two modes:

- **Discharge mode**: When $V_{csp} > V_{csn}$ makes $I_1 > I_2$, the controller turns on $S_0$, and then $V_{BIAS}$ is kept higher than $V_{cso}$ to inject current into the current mirror.
- **Charge mode**: When $V_{csp} < V_{csn}$ makes $I_1 < I_2$, the controller turns on $S_1$, and then $V_{BIAS}$ is lower than $V_{cso}$. The current would be steered away from $V_{cso}$ to $V_{BIAS}$.

Assume the gain of the entire system is $A_V$. $V_{cso}$ can be formulated as follows.

$$V_{cso} = V_{cs} \cdot A_V + V_{BIAS}$$  \hspace{1cm} (2)

$A_V$ can be written as follows:

$$A_V = \frac{R_{out}}{2 \cdot R_{NF}}$$  \hspace{1cm} (3)

Based on Eqs. (2) and (3), $V_{cso}$ can be organized as follows:

$$V_{cso} = \frac{V_{cs} \cdot R_{out}}{2 \cdot R_{NF}} + V_{BIAS}$$  \hspace{1cm} (4)

Therefore, $I_{cs}$ can be estimated indirectly using $V_{cso}$, as follows:

$$I_{cs} = \frac{V_{gs}}{R_{cs}} = \frac{(V_{cso} - V_{BIAS}) \cdot 2 \cdot R_{NF}}{R_{out} \cdot R_{cs}}$$  \hspace{1cm} (5)

### 2.2. FDA design

FDA in Fig. 2 is basically a two-stage fully-differential amplifier including a common-mode feedback, as shown in Fig. 3 [11]. Apparently, the common-mode voltage affects the output swing. Since the proposed sensor is meant to detect high voltage and current, which will easily generate significant common-mode offset. Thus, common-mode feedback circuit is needed, which regulates its common-mode voltage to a pre-defined value.

FDA shown in Fig. 3 is used to create virtual shorts and generate stable $V_{op}$ and $V_{on}$ to drive M301 and M302 into saturation, respectively. The saturation condition of PMOS is governed by Eqs. (6) and (7).

$$|V_{gs} - V_{th}| > 0$$  \hspace{1cm} (6)

$$|V_{ds}| = |V_{gs} - V_{th}|$$  \hspace{1cm} (7)

where $V_{th}$ is the PMOS threshold voltage. The common mode output voltage of FDA, namely $V_{oc}$, can be written as follows:

$$V_{oc} = \frac{V_{gs} + V_{on}}{2}$$  \hspace{1cm} (8)
Moreover, the differential mode output voltage of the FDA, namely $V_{od}$, is as follows [10]:

$$V_{od} = (V_{ip} - V_{in}) \times A_{FDA} \quad (9)$$

where $A_{FDA}$ is the FDA gain. Thus, $A_{FDA}$ can be summarized as follows:

$$A_{FDA} = \frac{g_{m,M309}(r_{o,M309} \parallel r_{o,M311})}{r_{o,M313} \parallel r_{o,M314}} \quad (10)$$

where $g_{m,M313} = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})$, $r_{o,M313}$ is the output resistance of M313, $\mu$ is the carrier mobility, and $C_{ox}$ is the capacitance of the gate oxide. Based on Eqs. (8) and (9), the gate voltage of M301 ($V_{g,M301}$) and M302 ($V_{g,M302}$) can be derived as follows:

$$V_{g,M301} = V_{on} = V_{oc} + \frac{V_{od}}{2} \quad (11)$$

$$V_{g,M302} = V_{op} = V_{oc} - \frac{V_{od}}{2} \quad (12)$$

Thus, $V_{g,M301}$ and $V_{g,M302}$ can be re-organized as follows:

$$V_{g,M301} = \frac{V_{op} + V_{on}}{2} + \frac{(V_{ip} - V_{in}) \times A_{FDA}}{2} \quad (13)$$

$$V_{g,M302} = \frac{V_{op} + V_{on}}{2} - \frac{(V_{ip} - V_{in}) \times A_{FDA}}{2} \quad (14)$$

Thus, $A_{FDA}$ should be tuned not too large to keep M301 and M302 saturated.

### 2.3. Controller design

Referring to Fig. 2 again, Controller comprises a comparator (CMP), a T flip-flop, and an external micro-controller (MC). Fig. 4 is the schematic of the proposed comparator. The operation is listed as follows.

(1). T flip-flop is activated by Preset. When Preset = 1, $S0 = 1$. Preset = 1 at power on and $T = 1$ in the initial state.

(2). CMP compares $V_{cso}$ with $V_{BIAS}$ to trigger T flip-flop. When $V_{BIAS}$ is higher than $V_{cso}$, namely Discharge mode, $S0$ and $S1$ are kept unchanged. On the contrary, it will be in the Charge mode, and then T flip-flop pulls high $S1$, and $S0$ is pulled low.

(3). MC will generate $T$ based on the previous state and the current state of the circuit as follows.

- The previous and the current states = Charge mode $\Rightarrow T = 0$.
- The previous state = Charge mode and the current state = Discharge mode $\Rightarrow T = 1$.
- The previous and the current states = Discharge mode $\Rightarrow T = 0$.
- The previous state = Discharge mode and the current state = Charge mode $\Rightarrow T = 1$.

(4). CMP compares $V_{cso}$ with $V_{BIAS}$ again to determine the states of $S0$ and $S1$.

This controller is in charge of the automatic bidirectional current sensing for the battery system no matter what the state is, either changed from discharge to charge, or vice versa. Fig. 5 is the flow chart of the controller. Preset is basically an enable signal to activate $S0$ and
S1. When Preset becomes 1, So is high. Then, the Preset, S1, and S0 will change depending on the magnitudes of VBIAS and Vcaso(I). Thus, controller can work correctly when the current direction changes at will.

3. Implementation and measurement

The proposed current sensor was fabricated using TSMC 0.5 μm CMOS high-voltage mixed-signal based LDMOS USG AL 2P3M polycide (T50UHV).
3.1. Post-layout simulations

To reject the high-frequency noise higher than 1.5 MHz, $R_{NF} = 10$ kΩ, and $C_{NF} = 20$ pF are used in the Noise filter (referring to Eqn. (1)). To enlarge the range of the sensor current, the smallest $R_{CS}$ is selected to be 0.067 Ω in our design. Referring to Eqn. (2), a linear function is expected between $V_{CS}$ and $V_{CE}$. Fig. 6 (a) shows post-layout simulations between $V_{CS}$ and $V_{CE}$ to verify this feature, when the sensed voltage ($V_{CS}$) range is -200 – 200 mV, and $V_{BIAS}$ is 5 V. Moreover, Fig. 6 (b) is the all-PVT-corner (process, voltage, temperature) post-layout simulations of the proposed current sensor to validate Eqn. (5). It shows that when the sensing current range is -3 – 3 A, the output voltage range $V_{CS}$ is 3–5 V. The proposed HV current sensor shows the worst-case sensing error of 0.85% when $I_{CS}$ equals to ±3 A, as shown in Fig. 7. Besides, the average error is 0.48%.

3.2. Chip implementation and measurement setup

Fig. 8 shows the die photo of the proposed HV current sensor, where the chip area is 1744 × 1303 μm², and the core area is 1173 × 664 μm². The measurement setup with the battery module is shown in Fig. 9. The ANR26650 battery module is the real battery device to be tested [12], where the current magnitude is adjusted via an electronic load (PRODIGT 32131D Electronic Load). The power supply (Chroma 3201P-600-B) is in charge of supplying the required bias voltages ($V_{BIAS}$). An oscilloscope (Teledyne LeCroy - WaveRunner 610Zii) is used to monitor $V_{CE}$. Battery test equipment (LANHE CT2001D) is also used to assess the performance of the proposed HV current sensor.

3.3. Field measurement

To prove the performance of the proposed sensor working in the range of 8–14 V, the power supply generates 7 voltages (8, 9, 10, 11, 12, 13, 14 V). Meanwhile, the electronic load consumes 13 different currents in the range of 0–3 A, as shown in Fig. 10. Fig. 11 summarizes the error distribution at the 7 sensed voltages given the same current. The worst measured error is less than 1.22%.

Beside the experiment using equipments as the above, we use a real battery module consisting of 4S3R ANRANR26650 cells of which specification is given in Table 1. A battery testing system (LANHE CT2001D) was used to charge/discharge the battery module. Three chips fabricated with the proposed HV current sensor were used to carry out a total of 225 times measurements as summarized in Fig. 12. The standard deviation in the measurement results is smaller than ±3σ, as shown in Fig. 13. Table 2 tabulates a performance comparison of the proposed design and several recent works. Notably, our design is the only one to work in the range of 8–14 V and 0–3 A with maximum error of only ≤0.7%. Assume the FOM (figure of merit) is defined in Eqn. (15). Our design attains the best FOM of all the works.

\[
\text{FOM} = \frac{\text{Voltage Range} \times \text{Sensing Current Range}}{\text{Core area} \times \text{Max. Error}} \tag{15}
\]
Fig. 9. Measurement setup of the proposed HV current sensor.

Fig. 10. Measurement results attained using the proposed HV current sensor.

Fig. 11. $V_{CSO}$ error measurement attained using the proposed HV current sensor.

Fig. 12. $V_{CSO}$ error measurement in charge/discharge mode obtained using the proposed HV current sensor in real battery module testing.

Table 1

Cell specifications of the lithium-ion rechargeable battery (MODEL: ANR26650) [12].

<table>
<thead>
<tr>
<th></th>
<th>ANR26650</th>
</tr>
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<tbody>
<tr>
<td>Nominal Voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Charge Voltage</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Discharge Cutoff Voltage</td>
<td>2 V</td>
</tr>
<tr>
<td>Nominal Charge current</td>
<td>2.5 A</td>
</tr>
<tr>
<td>Maximum Charge current</td>
<td>10 A</td>
</tr>
<tr>
<td>Maximum Discharge current</td>
<td>50 A</td>
</tr>
<tr>
<td>Typical Capacity</td>
<td>2500 mAh</td>
</tr>
<tr>
<td>Minimum Capacity</td>
<td>2400 mAh</td>
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Table 2
Comparison to state-of-the-art.

<table>
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<tr>
<th>Year</th>
<th>TPE</th>
<th>TENCON</th>
<th>INTELEC</th>
<th>ICECS</th>
<th>ISCAS</th>
<th>LEM</th>
<th>This work</th>
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<tbody>
<tr>
<td>2014</td>
<td>2015</td>
<td>2016</td>
<td>2016</td>
<td>2018</td>
<td>N/A</td>
<td>2020</td>
<td></td>
</tr>
<tr>
<td>Process</td>
<td>0.5 μm CMOS</td>
<td>0.25 μm BCD</td>
<td>PCB</td>
<td>0.18 μm HVC</td>
<td>0.5 μm CMOS</td>
<td>Hall sensor</td>
<td>750UHV CMOS</td>
</tr>
<tr>
<td>Implementation</td>
<td>Measurement</td>
<td>Measurement</td>
<td>Measurement</td>
<td>Simulation</td>
<td>Simulation</td>
<td>Measurement</td>
<td>Measurement</td>
</tr>
<tr>
<td>Bidirectional</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>5.5</td>
<td>5</td>
<td>12</td>
<td>1.8 &amp; 5</td>
<td>5</td>
<td>±15</td>
<td>5–20</td>
</tr>
<tr>
<td>Voltage Range (V)</td>
<td>2.7–4.5</td>
<td>36–55</td>
<td>1–12</td>
<td>36</td>
<td>5</td>
<td>±15</td>
<td>8–14</td>
</tr>
<tr>
<td>Sensing Current Range (A)</td>
<td>0.05–0.6</td>
<td>0.44–2.2</td>
<td>1–20</td>
<td>0.5–1.5</td>
<td>0–5</td>
<td>±3–3</td>
<td>±3–3</td>
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<tr>
<td>Max. Error (%)</td>
<td>4</td>
<td>2.5</td>
<td>3.3</td>
<td>1.2</td>
<td>3</td>
<td>±1.5</td>
<td>0.7(≤±3σ)</td>
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<tr>
<td>Core Area (mm²)</td>
<td>0.05</td>
<td>1.58</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0.78</td>
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<tr>
<td>FOM</td>
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<td>8.17</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>76.923</td>
</tr>
</tbody>
</table>

Note: σ: Standard deviation.

Fig. 13. Standard deviation of measurement results (225 times).

4. Conclusion

This investigation presents a high-accuracy CMOS HV bidirectional current sensor. Our design works in the input voltage range from 8 to 14 V. Moreover, it attains the very small sensing voltage error <0.7%. The design is featured with the digital feedback control to make bidirectional sensing feasible, and achieve the high accuracy at the same time.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

This work was partially supported by Ministry of Science and Technology (MOST), Taiwan, under grant MOST 110-2218-E-110-008-, MOST 109-2241-E-110-001- and MOST 109-2218-E-110-007-. Moreover, this work was also partially supported by Ministry of Economic Affairs, Taiwan, under grant 107-EC-17-A-17-S3-050. The authors would like to express their deepest gratefulness to TSRI (Taiwan Semiconductor Research Institute), Taiwan, for their thoughtful chip fabrication service.