Microelectronics Journal 118 (2021) 105295

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

# An adaptive constant current and voltage mode P&O-based Maximum Power Point Tracking controller IC using 0.5-μm HV CMOS

Chua-Chin Wang [a,b,*], Oliver Lexter July A. Jose [a], Po-Kai Su [a], Lean Karlo S. Tolentino [a,c], Ralph Gerard B. Sangalang [a,d], Jessica S. Velasco [c], Tzung-Je Lee [a]

[a] Department of Electrical Engineering, National Sun Yat-Sen University, No. 70 Lian-Hai Road, Gushan District, Kaohsiung, 80424, Taiwan
[b] Institute of Undersea Technology, National Sun Yat-Sen University, No. 70 Lian-Hai Road, Gushan District, Kaohsiung, 80424, Taiwan
[c] Department of Electronics Engineering, Technological University of the Philippines, Ayala Boulevard, Ermita, Manila, 1000, Philippines
[d] Department of Electronics Engineering, Batangas State University, Alangilan, Batangas City, 4200, Philippines

ARTICLE INFO

*Keywords:*
Energy harvesting
Maximum Power Point Tracking (MPPT)
Perturb and observe (P&O)
Photovoltaic (PV)
HV CMOS

ABSTRACT

Photovoltaic (PV) energy harvesting has been widely used in the application of energy storage for battery charging. The more solar energy effectively harvested by the harvesting circuit, the more efficient charging will take place. Many papers used different MPPT methods that enhance PV harvesting that require ADC and MCU which is costly and also requires a long period of tracking. A high-voltage energy harvesting circuit with adaptive constant current (ACC), constant voltage (CV), and maximum power tracking (MPPT) control for 20V/5 W solar panels is proposed to carry out the constant current charging (CC) and constant voltage (CV) charging modes of lithium-ion batteries when the solar panel's maximum power point changes. Pulse width modulation (PWM) and pulse frequency modulation (PFM) are implemented under different light intensity conditions to improve the efficiency. The ACC mode controlled by perturb-and-observe (PBO) MPPT algorithm improved the efficiency during insufficient light source or low battery power. When the battery is fully charged, the over-charging damage is prevented to the lithium-ion battery when CV mode is activated. TSMC 0.5-μm UHV process is used to fabricate the energy harvesting circuit. For the photocurrent range of 0.1 A to 0.3 A, this design achieved a peak efficiency of 98%.

## 1. Introduction

Green energy is the major trend and will be the world focuses on technology development. Many countries regard the increase in the proportion of green energy usage as a national policy direction. The countries have also signed a treaty to reduce carbon emissions, hoping to achieve a green homeland in the future. Among the many natural energy resources, solar energy is the natural energy with the highest available energy density and has the characteristics of generating added value. If the solar energy source can be accessed efficiently, the ratio of natural energy usage will be greatly increased, and the core concept of sustainable development will be achieved.

In recent years, photovoltaic (PV) energy harvesting has focused on low-power applications in vehicles [1,2], wireless sensors [3], modern mobile devices [4], Internet of Things (IoT) [5], wireless sensor networks (WSN) [6], roof-integrated PV (photovoltaic) systems [1], and the application of energy storage for battery charging [3,7–9]. It is a popular trend nowadays because the highest power density is exhibited by solar energy [7]. Among the devices that can store energy, the lithium battery is featured with high energy density which is why it is widely used in many portable devices. If solar energy can be harvested more effectively through the energy harvesting circuit, then the utilization of solar energy for more efficient charging will not only make life more convenient, but also increase the usage of renewable energy.

The general lithium battery charging curve is shown in Fig. 1. A charging cycle can be roughly divided into constant current mode (CC) and constant voltage mode (CV). In the constant current charging mode, a large current is used. Battery charging speeds up the charging time and efficiency; when the battery voltage reaches $V_{full}$, it will enter the constant voltage charging mode to prevent the battery from overcharging through the charging current.

Based on the characteristic curve of the PV cell, under certain conditions, the PV cell can output the maximum power. At this time, its voltage output by the solar cell is called Vmpp and the current is called Impp. The process of continuously controlling the solar panel

* Corresponding author.
*E-mail address:* ccwang@ee.nsysu.edu.tw (C.-C. Wang).

https://doi.org/10.1016/j.mejo.2021.105295
Received 9 June 2021; Received in revised form 31 August 2021; Accepted 20 October 2021
Available online 11 November 2021

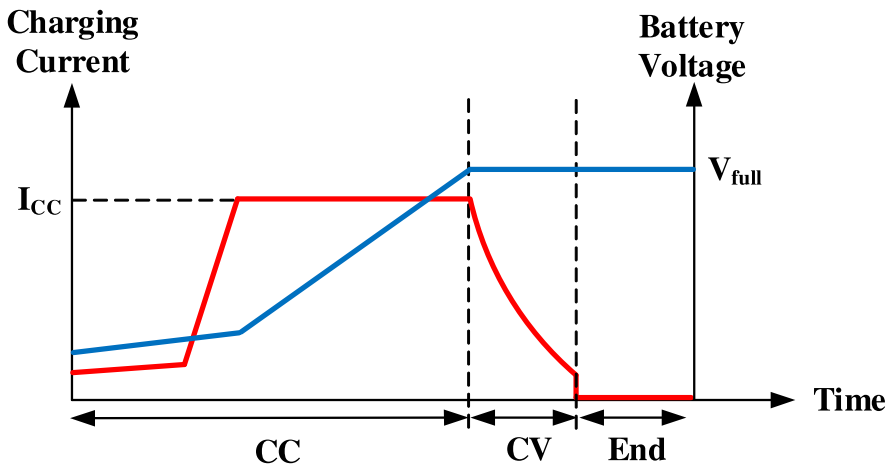



**Fig. 1.** Battery charging curve of lithium battery.[10].

**Table 1**
Comparison of the MPPT methods.

| MPPT method | PV panel dependent | True MPPT | Implementation complexity |
|---|---|---|---|
| P&O/Hill Climbing [12] | No | Yes | Medium |
| Sectored Hill Climbing [12] | Yes | Yes | Medium |
| FOCV [5,6] | No | No | Low |
| Incremental Conductance [12] | No | Yes | High |
| Ripple correlation control [9] | No | Yes | Medium |
| Neural Network [13] | Yes | Yes | High |
| Fuzzy Logic [13] | Yes | Yes | High |

at the Maximum Power Point (MPP) is called Maximum Power Point Tracking (MPPT).

Many prior small works already presented different MPPT methods which can enhance PV energy harvesting' s efficiency [1–8,11–13]. The incremental conductance method [12], the neural network, and the fuzzy logic control method [13] use digital logic circuits to determine the power and then track the MPP. These digital logic circuits require analog-to-digital converters (ADC) and microcontrollers (MCU) which are costly and requires long period of tracking. On the other hand, tracking of the MPP will be faster and the system cost will be lower through analog power calculation method [8], the perturb and observe (P&O), or hill-climbing method [1,2,7]. These methods sense the output current since the output current is proportional to the output power. With this, the maximum power can therefore be determined. To further enhance the tracking speed, sectored hill-climbing method [3] was used. It uses an embedded resistor array for the analysis and storage of the PV's features ($V_{mpp}$, $I_{mpp}$, etc.) to track the MPP, but complex control circuits are needed for its implementation. The ripples in the voltage and current are considered in ripple correlation control (RCC) method. Analog circuits can be easily implemented using RCC method as shown in certain previous works [9,14]. However, RCC does not perform well at varying transients and irradiances [15]. On the other hand, simple control circuits are used in the fractional open circuit voltage (FOCV) method in sensing the open-circuit voltage and detecting the MPP [5,6]. Nevertheless, its tracking efficiency is lower than that in other stated techniques.

Among the MPPT methods mentioned above, the implementation of P&O and sectored hill-climbing methods in integrated circuits is relatively simple, while incremental conductance [12] requires an analog to digital converter and a digital to analog converter, which will make the MPPT controller consume more power. A circuit [13] which used a different method, i.e., neural network and fuzzy logic control method, needs to be realized through a microprocessor. Finally, Table 1 summarizes the comparison of these MPPT methods.

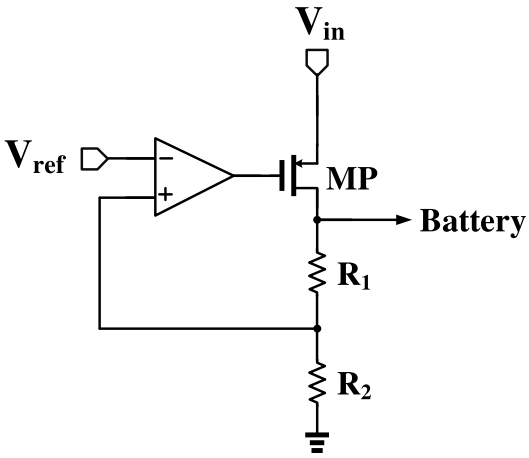



**Fig. 2.** Typical low dropout (LDO) architecture.

In this paper, a 5-W, 10–20 V PV and a 3.6 to 4.2-V Li-ion battery are used as energy source and storage device, respectively. This solar panel is commonly used in medical equipment and air monitoring systems applications [11]. The purpose of this paper is to present a single-die MPPT Energy Harvesting IC.

The proposed P&O-based MPPT energy harvesting circuit utilized adaptive constant current (ACC) mode with PWM control based on the PV's output current. In addition, it executes the constant voltage (CV) mode to protect the battery from overcharging . TSMC 0.5-μm UHV CMOS process was used to fabricate the chip. Measurement results show a 98% peak MPPT tracking efficiency and a 5-W power throughput of 5 W at a 1-MHz switching frequency.

## 2. Energy harvesting system design principles and methods

Currently, most energy harvesting circuits are aimed at low-power applications in wireless sensor networks, and seldom are used for general solar panels. In low-power energy harvesting circuits, the voltage is usually not too high. The solar energy harvesting circuit for general power storage can be integrated into the circuit through higher voltage process CMOS technology.

Battery charger circuit can be divided into low dropout (LDO) architecture and switching architecture, as shown in Figs. 2 and 3, respectively. The advantages of the LDO architecture are small area and high accuracy, but the efficiency is low when the input and output voltage difference is large. The switching architecture can provide a

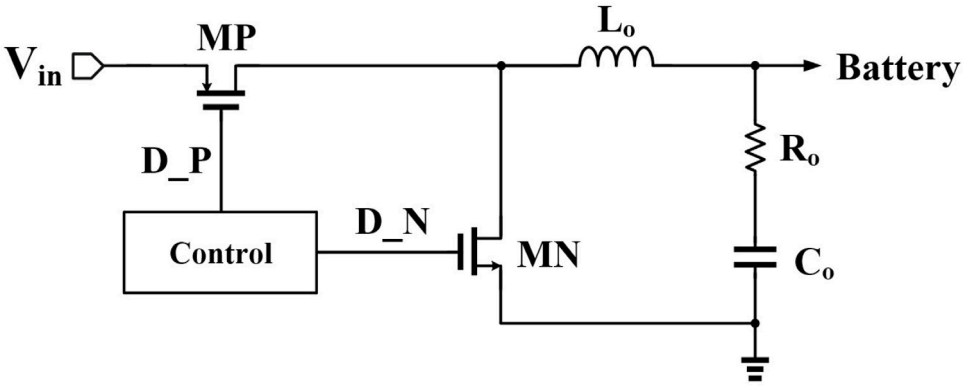



**Fig. 3.** Typical switching architecture.

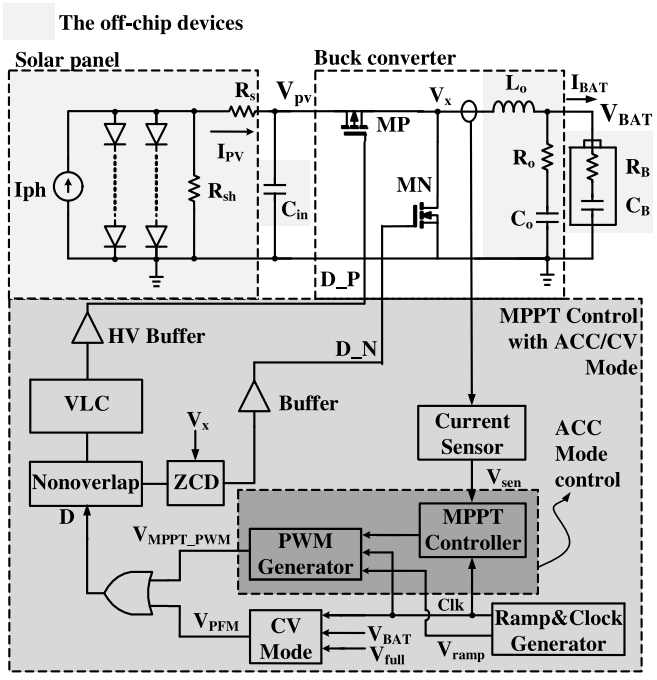



**Fig. 4.** Block diagram of the proposed design.

larger output current, and can maintain high efficiency when the input and output ranges are large, but the disadvantage is that the design is complex, large and ripples.

In order to receive the large current output from PV cells and achieve high efficiency, the design uses the switching architecture. More specifically, the proposed control method using the switching architecture is Pulse Width Modulation (PWM). In an environment with stable and sufficient sunlight, solar energy can produce an output of large currents that can be regarded as heavy load, and maximum power point tracking is performed through PWM so that the battery can be charged with high efficiency. When the battery voltage reaches 4.2 V, it enters the constant voltage charging mode, and needs to be charged with a small current, which is regarded as light load. Therefore, the constant voltage charging mode uses pulse frequency modulation (PFM) to reduce switching loss and improve the overall efficiency [11].

The operating modes of the system in this design depends on a current sensor to detect the inductor current, converting it into voltage parameter $V_{sen}$, and sending it to the MPPT control circuit. After sampling and holding, the magnitudes are compared to obtain change in current. Since the sampling period is much shorter than the change in battery charging voltage, the slow change in battery voltage can be ignored. The change in power is then attained by observing the change of the charging current.

## 3. System architecture

Fig. 4 shows the system block diagram of the overall architecture. It consists of a 10–20 V, 5-W solar panel, a 3.6 to 4.2-V Li-ion battery, a Buck Converter which serves as energy harvester and an MPPT Control Circuit with ACC/CV Modes. The equivalent circuit of the solar panel, which is generated by actually measuring its characteristics, uses a 2-D model. $I_{PH}$ represents the resulting photocurrent, that changes based on the solar irradiance or amount of light source. Series and shunt parasitic resistors are represented by $R_s$ and $R_{sh}$, respectively. The diodes connected in series and parallel represent the PV cells connected in series and parallel. $V_{PV}$ and $I_{PV}$ are the generated solar panel's voltage and current, respectively. The current–voltage (IV) characteristic curve of the solar cell is shown in Fig. 5, which is consistent with the solar panel used. In the said figure, the maximum power changes at different level photocurrents (which represents solar irradiances). To step down the solar panel's voltage, the buck converter is needed. It includes the 20-V HV CMOS transistors (MP and MN), the load capacitor ($C_o$), and the load inductor ($L_o$). The $C_o$'s effective resistance is denoted by $R_o$. The MPPT Control with ACC/CV Mode includes the Current Sensor, MPPT Controller, the PWM generator, the constant voltage mode control circuit (CV Mode control), (VLC), Zero-Current Detector (ZCD), Ramp & Clock Generator and Nonoverlap circuit.

### 3.1. Methodology

The perturb and observe (P&O) algorithm is shown in Fig. 6. The entire operation is listed as follows.

(1) Comparing the current photovoltaic power (P(t)) to previews photovoltaic power (P(t)) by current (I) and voltage (V) measurements at these two consecutive time steps.
(2) When the difference between P(t) and P(t−1) is not equal to zero, the maximum power point (MPPT) of the optimal point will be tracked or located whether to the left or right of the recent position in the power–voltage (P–V) characteristic curve.
(3) When P(t)−P(t−1) equals to 0, the maximum power is obtained. The P&O method is executed by altering the PWM duty cycle.
(4) If the power at the current step is greater than that at the previous step, the duty cycle will be increased until the MPP is determined.

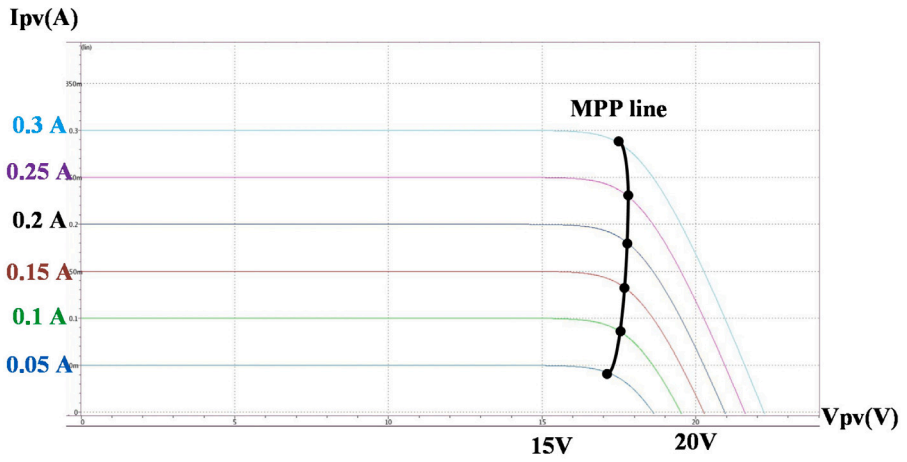



**Fig. 5.** Current–voltage (IV) characteristic curve of the solar cell.

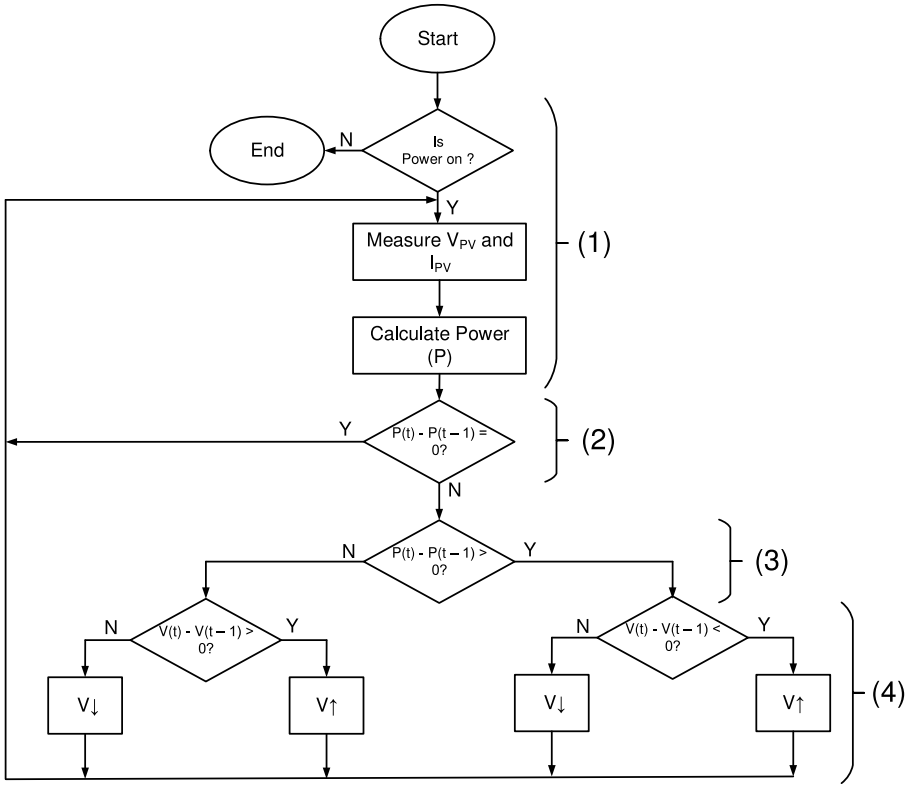



**Fig. 6.** Proposed method.

### 3.2. Current sensor

Since the battery current needs to be detected for comparison, the current sensor in Fig. 7 is used to monitor the inductor current ($I_L$). Referring to Fig. 7, M1, M2, M4 and MP, M3, M5 are current mirror, making $V_y$ equal to $V_x$. In this way, M1 can copy the MP's current ($I_L$ or $I_{BAT}$) which has a ratio of 1/K, reducing linearly the inductor current to be detected. Since the current along M1 is $\frac{I_{BAT}}{K}$ and the current along M2 is $I_{bias}$, the current along MR will be $\frac{I_{BAT}}{K} - I_{bias}$. Eq. (1) shows the expression for the output voltage, $V_{sen}$. $V_{sen}$ is linearly related to $I_{BAT}$, if $I_{BIAS} \ll \frac{I_{BAT}}{K}$ is satisfied.

$$V_{sen} = \left( \frac{I_{BAT}}{K} - I_{BIAS} \right) \times R_{sen} \quad (1)$$

### 3.3. MPPT controller

Fig. 8 shows the MPPT Controller and PWM Generator circuit [10]. After the current sensor detects the inductor current and converts it into $V_{sen}$ signal, the said signal sequentially enters the capacitor for sampling and holding. The two-phase comparison can detect and estimate the inductor's current indirectly through. This modulates the magnitude of voltage $V_{cc}$ and compares it with $V_{ramp}$ to generate a $V_{MPP\_PWM}$ which regulates and controls the duty cycle, thereby achieving impedance matching and maximum power point tracking.

### 3.4. ACC mode charging

Referring to Fig. 8, during ACC mode, transmission gates, TG1 and TG2 simultaneously samples the sensed signal, $V_{sen}$. Comparator, CMP1, compares the sampled signals to determine the operating

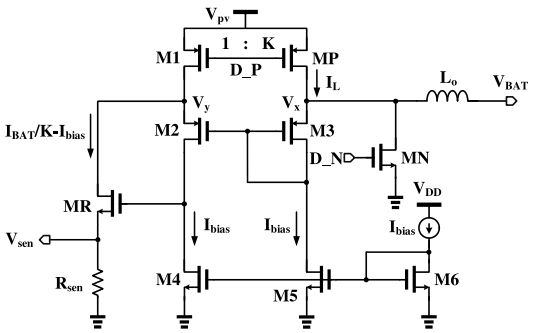
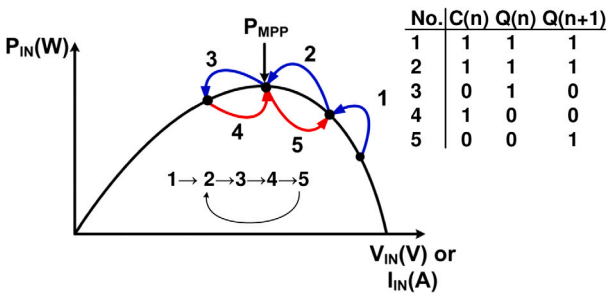



**Fig. 7.** Schematic of the Current Sensor.




| No. | C(n) | Q(n) | Q(n+1) |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 1 |
| 3 | 0 | 1 | 0 |
| 4 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 |

**Fig. 9.** The MPPT tracking process.

power point. Referring to Fig. 9 and Table 2, a typical MMPT tracking procedure is listed as follows;

Step 1 XNOR gate and the DFF generates C(n), Q(n), and Q(n+1) which adjust the power point, where C(n) denotes the change of induction current. A logic value of 1 for C(n) means an increase in current. The changing direction of $V_{cc}$ in the previous and present cycles are represented by Q(n) and Q(n+1), respectively.

Step 2 An increase in $V_{cc}$ in the final cycle means a Q(n) value of 1. Performing the process which consists of Steps 2, 3, 4, and 5 again as shown in Fig. 9 and Table 2 can track the MPP effectively. Since the current is directly related to the solar panel's power and a much smaller change in $I_{BAT}$ at every cycle is expected, tracking the MPP is attainable.

Step 3 Transistors in Fig. 8, sw1 and sw2, were controlled by Q(n) to see the status of $V_{cc}$ whether charged or discharged. Q(n) stores the Q(n+1) of the previous cycle which is high. The comparison result of C(n) is low (that is, the output power of the solar cell in this period is less than the output power of the previous period). The said condition indicates that the maximum power point (MPP) has achieved. At this time, $V_{cc}$ is adjusted to a lower value. Then, the direction of the power point will be reversed, and a low state of Q(n+1)=0 is expected.

Step 4 The MPPT controller generates $V_{MPPT\_PWM}$ for output current ($I_{BAT}$) adjustment with respect to $V_{cc}$ and $V_{ramp}$. Sampling signals comprises sclk1 and sclk2 while the D flip-flop generates a trigger signal (sclk3).

Step 5 Q(n) is low and C(n) is low. At this time, the direction of the power point will be reversed, and Q(n+1) is high. Then, the next step will be Step 2 and the process is repeated until the maximum power point at a certain irradiance (represented by a photocurrent) is reached.

Fig. 11 shows the corresponding waveforms of the aforementioned operations.

**Table 2**
Transitions of the maximum power point tracking logic.

| Step | Q(n) | C(n) | Q(n+1) |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 1 |
| 3 | 1 | 0 | 0 |
| 4 | 0 | 1 | 0. |
| 5 | 0 | 0 | 1 |
| 2 | 1 | 1 | 1 |
| 3 | 1 | 0 | 0 |
| . | . | . | . |
| . | . | . | . |
| . | . | . | . |

Fig. 10 shows the simulation results of the design layout. When the sunlight is sufficient, the output current is in the range of 0.3 and 0.1 A. Notice also that the charging current of the lithium battery is 0.1 A. The time for the output voltage to become stabilized or the setting time is 2 ms.

### 3.5. CV mode control with PFM

Before the battery voltage $V_{BAT}$ reaches the full voltage $V_{full}$, Comparator Comp3 in Fig. 12 will generate logic 0 to make the $V_{PFM}$ output the same as CLK. Since the CLK duty cycle generated by the clock generator is very small, the $V_{MPPT\_PWM}$ duty cycle in Fig. 8 is relatively large. After the OR gate, $V_{MPPT\_PWM}$ is still output and sent to the non-overlapping circuit.

When the battery voltage $V_{BAT}$ reaches 4.2 V, it is an indication that the Li-ion battery is already fully charged, Comp3 will output logic 1 to mask-out CLK. At this time, $V_{PFM}$ will output a longer logic 1 signal such that MP in Fig. 13 will be turned off to achieve constant voltage charging. Fig. 13 illustrates the waveforms in CV mode.

### 3.6. Zero-current detector (ZCD)

In order to prevent power NMOS MN from generating reverse current, causing higher power consumption and reducing efficiency,

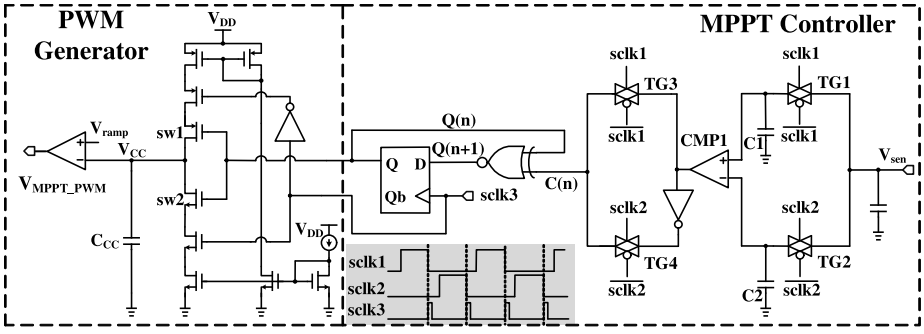



**Fig. 8.** MPPT Controller and the PWM Generator.

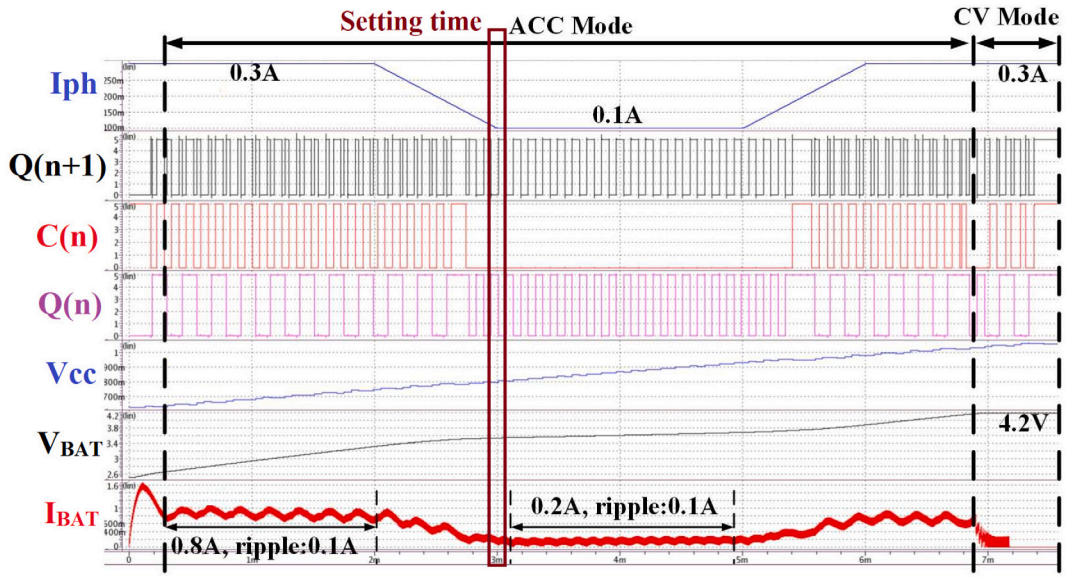



**Fig. 10.** Simulated Waveform in the Charging Process.

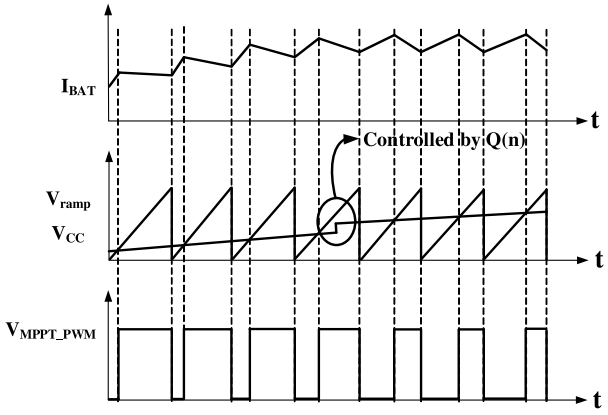



**Fig. 11.** The waveforms of $I_{BAT}$, $V_{ramp}$, $V_{CC}$ and $V_{MPPT\_PWM}$ during the MPPT process in ACC mode control.

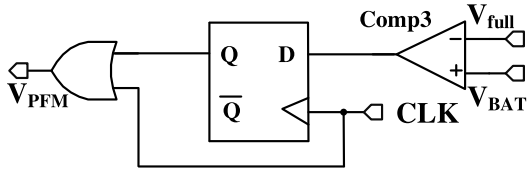



**Fig. 12.** CV Mode control circuit.

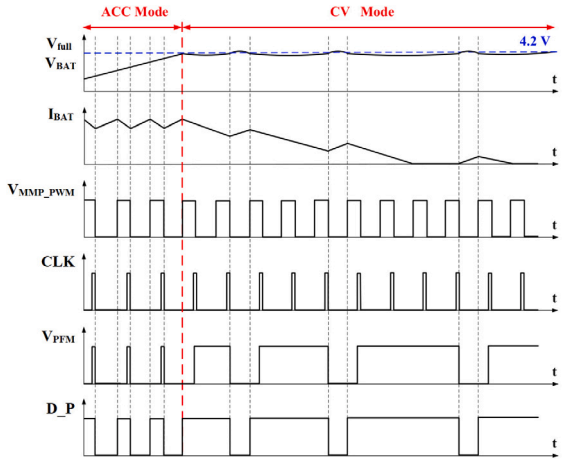



**Fig. 13.** Waveforms during ACC and CV modes.

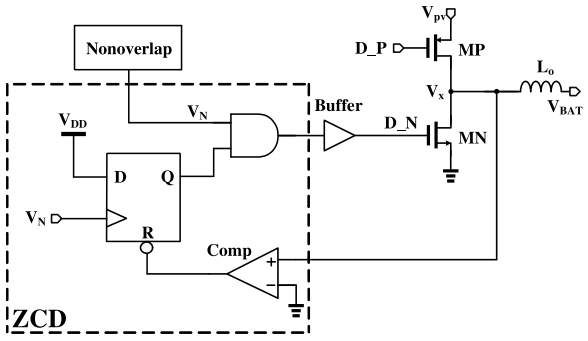



**Fig. 14.** Zero-current detector (ZCD).

a Zero-Current Detector (ZCD) as shown in Fig. 14 is needed to turn off MN immediately when the inductor discharges to zero current. Referring to Fig. 14, the D flip-flop is at reset condition when $V_x$ equals 0 V. Then, to switch off MN, D_N must be 0 V. If $V_x > 0$ V is satisfied, the Nonoverlap circuit's generated signal, $V_N$, is coupled to D_N for the system to operate normally.

### *3.7. Voltage level converter (VLC)*

Due to the need to raise the duty cycle signal to make the Power MOS completely turn off and on, a voltage level converter (VLC), as shown in Fig. 15, is needed to complete it. When the $V_{in}$ signal is logic 1, M1 will be turned on, and the logic 0 will be transmitted to the gate of M4 to turn on M4. When M4 is turned on, the $V_{DD}$ signal will be transmitted to $V_{out}$. Notably, $V_{DDH}$ in Fig. 15 is in the range of 40 ~ 60 V, and the $V_{DD}$ can be as low as 5 V in our design.

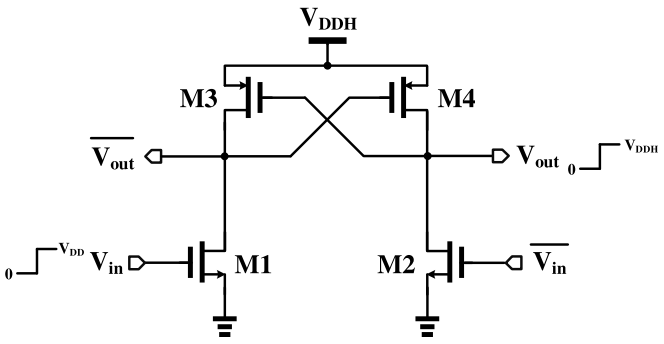



**Fig. 15.** Voltage level converter (VLC).

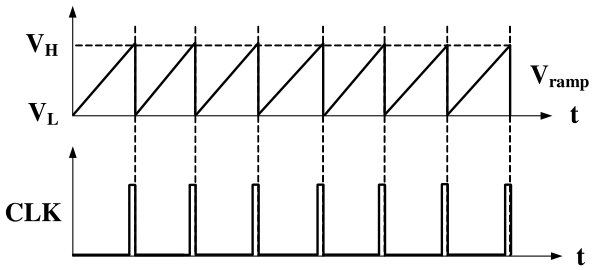



**Fig. 17.** Ramp and clock waveform.

**Table 3**
Solar panel specification sheet.

| Specification | Value |
|---|---|
| Maximum power | 5 W |
| Maximum power voltage | 18 V |
| Maximum power current | 0.28 A |
| Open circuit voltage | 21.6 |
| Short circuit current | 0.31 A |

### 3.8. Ramp & clock generator

In order to achieve PWM and PFM control, a ramp and clock generator is needed to provide the required signals. First, a bias current is generated to charge $C_{ramp}$. When the $V_{ramp}$ voltage reaches the upper limit voltage $V_H$, Comp1 will generate a logic 0 signal to make CLK output high. At this time, CLK will turn on M2 to quickly discharge $C_{ramp}$. When the $V_{ramp}$ voltage reaches the lower bound voltage $V_L$, Comp2 will generate a logic 0, making CLK output low, so that the above operations are repeated to generate the ramp and CLK signals (see Figs. 16–18).

### 3.9. Non-overlapping circuit

When the Power PMOS is turned on before the Power NMOS is completely turned off, a large current will flow from the supply to the ground, causing serious efficiency loss or even burning the circuit. To avoid this hazard, it is necessary to specially generate the two signals that control the Power MOS to make the Power PMOS turn on longer than the Power NMOS, so as to prevent the possible DC short-circuit scenario.

## 4. Measurement results

Fig. 19 illustrated layout and die photo of the chip which is fabricated using 0.5 μm HV CMOS, which is TSMC 0.5 μm CMOS HIGH VOLTAGE MIXED SIGNAL BASED LDMOS USG AL 2P3M POLICIDE 5/20/450/600/700/800 V. Core circuit used up 2073 × 2295 $\mu m^2$ from the 3600 × 3480 $\mu m^2$ chip total area. The location and size ratio of each sub-circuit inside the core is present.

The input of the measurement set-up consists of a 10 to 20-V polycrystalline solar panel, which the specification sheet is presented in Table 3, ITECH IT6333 A power supply to generate reference voltages and supply power to chip, and Agilent 33250 A to generate required clocks as shown in Fig. 20. The output waveform can be observed in LeCroy WaveRunner 610Zi and the current is monitored by Keysight.

Experiment 1: Insufficient sunlight results in a low input voltage of 3.3 V to the chip as shown in Fig. 21. With this, the PWM generator create pulses with different duty cycle to perform the ACC mode charging function.

Experiment2: An increase of input voltage to 4.26 V with varying and still insufficient sunlight drives the MPPT controller using the perturbation observation method generates a Q(n+1) signal as shown in Fig. 22. This signal then goes to the PWM generator for pulse wave modulation and the generated pulse waves will control power transistors.

Experiment 3: When the input voltage is boosted from 4.18 V to 4.1 V, (varying and insufficient sunlight), as shown in Figs. 23 and 24, respectively, the MPPT controller compares current from the inductor and input sample to generate the C(n) signal. Anti-mutual exclusion OR gate and D-type flip-flop circuit are responsible for maximum power tracking. They will generate Q(n) signal and send it to PWM generator to generate pulses.

Experiment 4: As battery approaches to full charge condition, illustrated in Fig. 25, it enters the constant voltage charging mode. Notice the pulse signals of different frequencies are modulated by PFM to achieve the effect of slowing down the charging current.

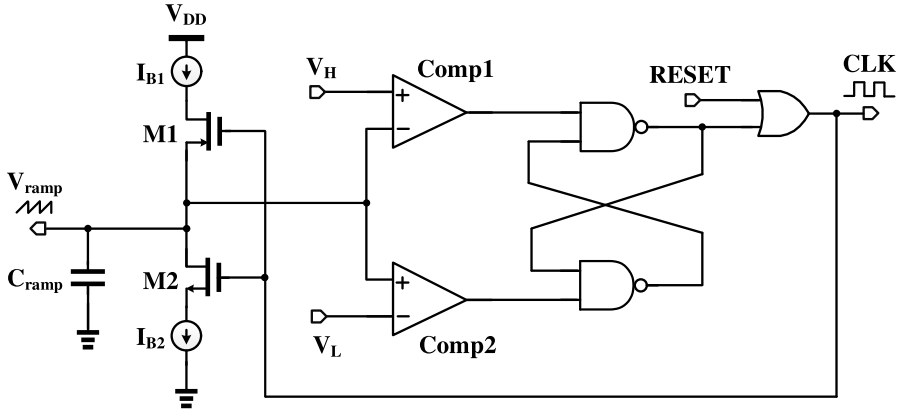



**Fig. 16.** Ramp and clock generator.

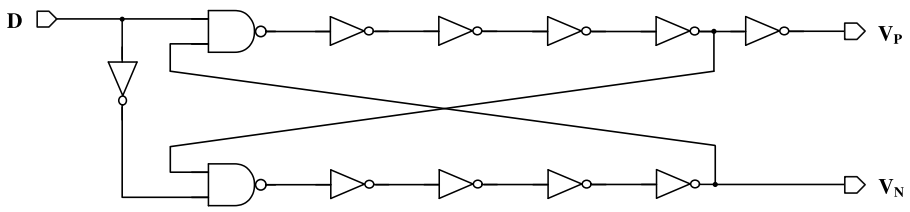



**Fig. 18.** Non-overlapping circuit.

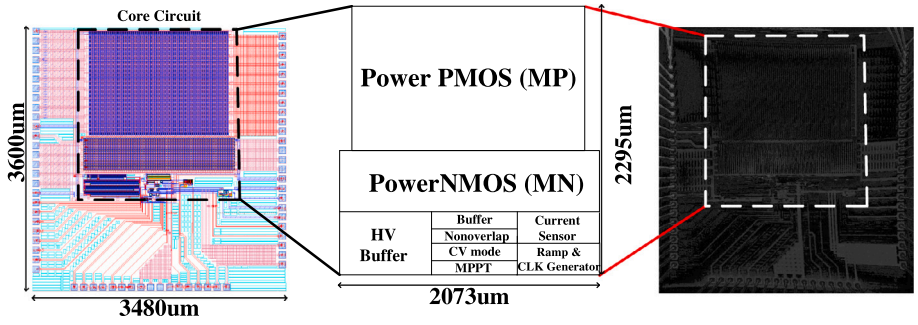



**Fig. 19.** 0.5 μm MMPT energy harvester layout and die photo.

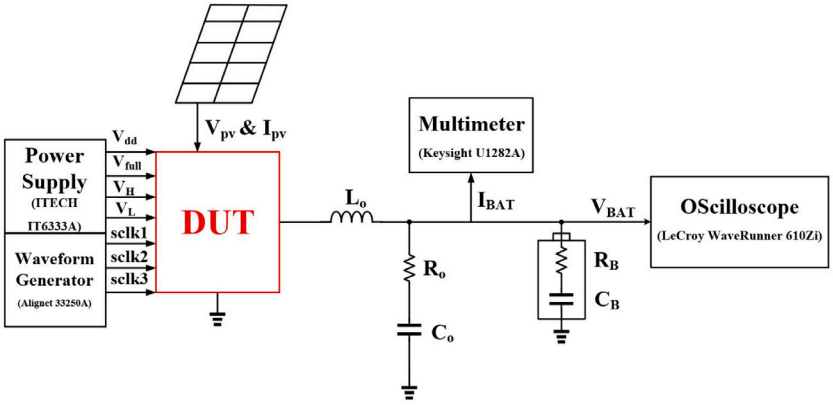



**Fig. 20.** Measurement setup.

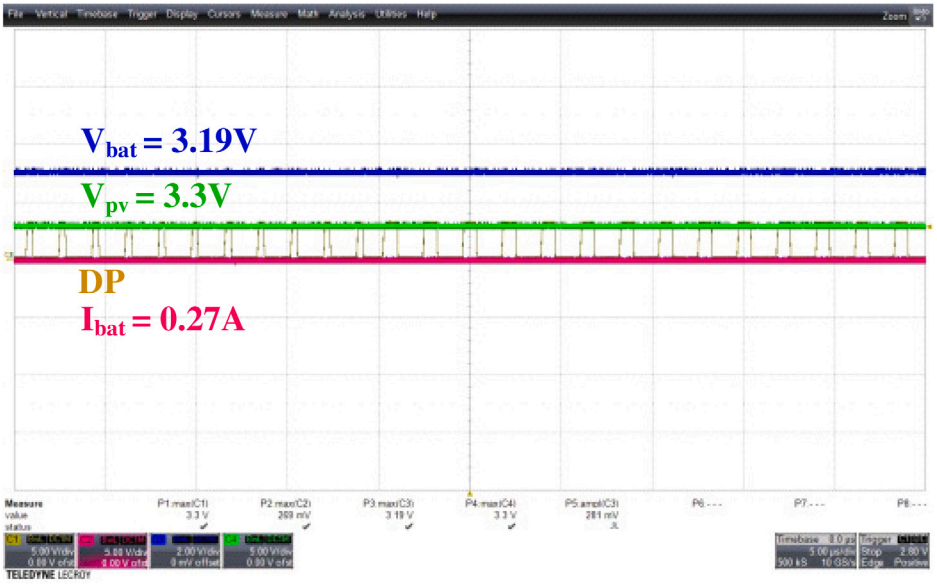



**Fig. 21.** Experiment 1: Pulses generated from 3.3 V low input voltage.

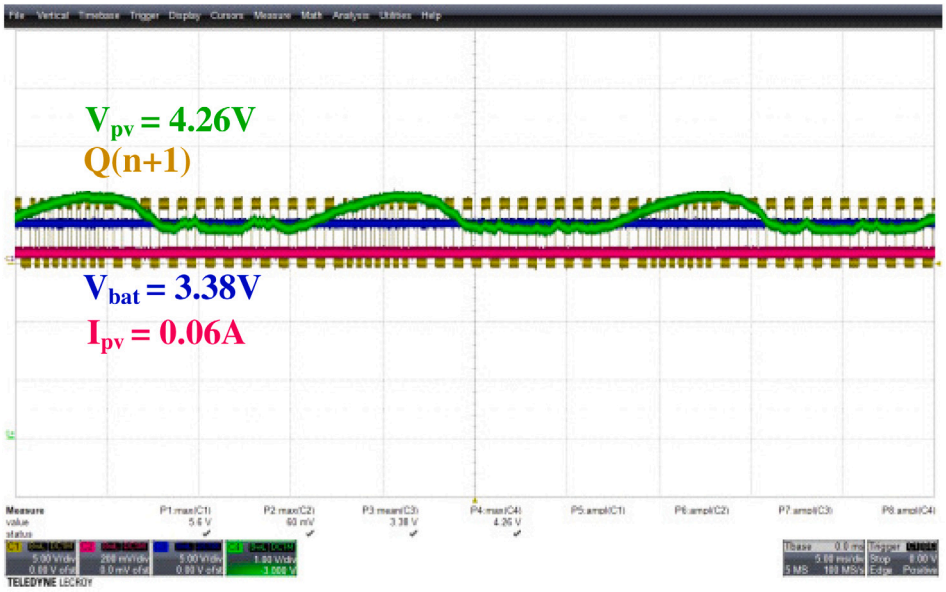



**Fig. 22.** Experiment 2: Pulses generated from 4.26 V low input voltage with maximum power tracking of Q(n+1).

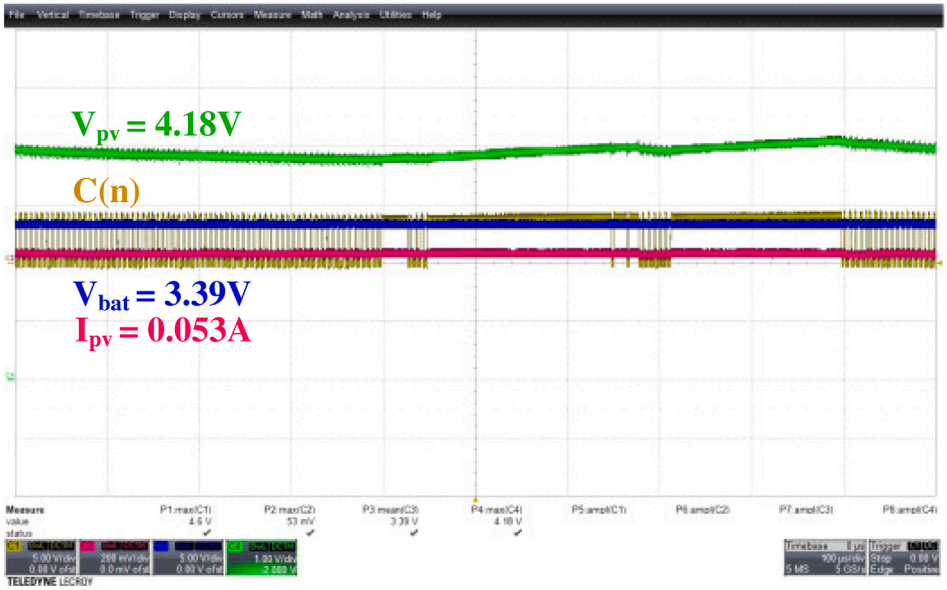



**Fig. 23.** Experiment 3: Pulses generated from 4.18 V low input voltage with controller sample and hold generates C(n).

Experiment 5: Given a sufficient sunlight of 15.9 V at the input, the output condition of the chip is shown in Fig. 26.

Table 4 presents the results of the voltage $V_{bat}$ and current $I_{bat}$ across the battery for the different values of $V_{pv}$. The value of $I_{pv}$ is based on the ACC mode charging. In experiment 1, it has the lowest voltage $V_{pv}$ with 3 V and provides a battery voltage of 3.19 V. As the value of the $V_{pv}$ increases, it still provides an output voltage across the battery. With the maximum input voltage in the PV cell of 15.9 V, it results in an output voltage of 3.31 V in the battery.

Table 5 shows the comparison with several recent research in PV Energy-Harvester. This work has generated highest operating voltage with 10 V and 20 V and power of 5 W. It also has the highest Figure of Merit (FOM) of 19.6, use 0.5-μm process technology and a high range of input voltage of 10 ∼ 20 V, which is the solar panel open-circuit voltage, $V_{oc}$.

**Table 4**
Summary of the input–output response from the experiment.

| | $V_{pv}$ | $I_{pv}$ | $V_{bat}$ | $I_{bat}$ |
|---|---|---|---|---|
| Experiment 1 | 3.3 V | – | 3.19 V | 0.27 A |
| Experiment 2 | 4.26 V | 0.06 A | 3.38 V | – |
| Experiment 3 | 4.18 V | 0.053 A | 3.39 V | - |
| | 4.1 V | 0.048 A | 3.42 V | |
| Experiment 4 | – | – | 4.11 V | – |
| Experiment 5 | 15.9 V | 0.118 A | 3.31 V | 0.324 A |

## 5. Conclusion

In this paper, we propose an MPPT controller IC which has ACC and CV modes for solar energy harvesting, During ACC mode, the ACC from the solar panel charges the Li-ion battery. The MPPT controller's peak tracking efficiency is 98% at a photocurrent ranging from 0.1–0.3 A

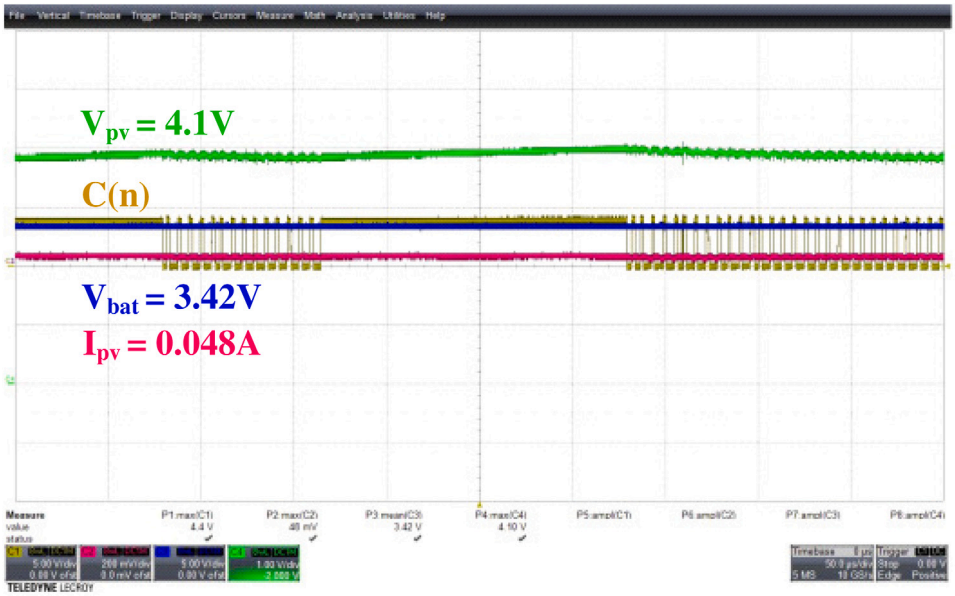



**Fig. 24.** Experiment 3: Pulses generated from 4.1 V low input voltage with controller sample and hold generates C(n).

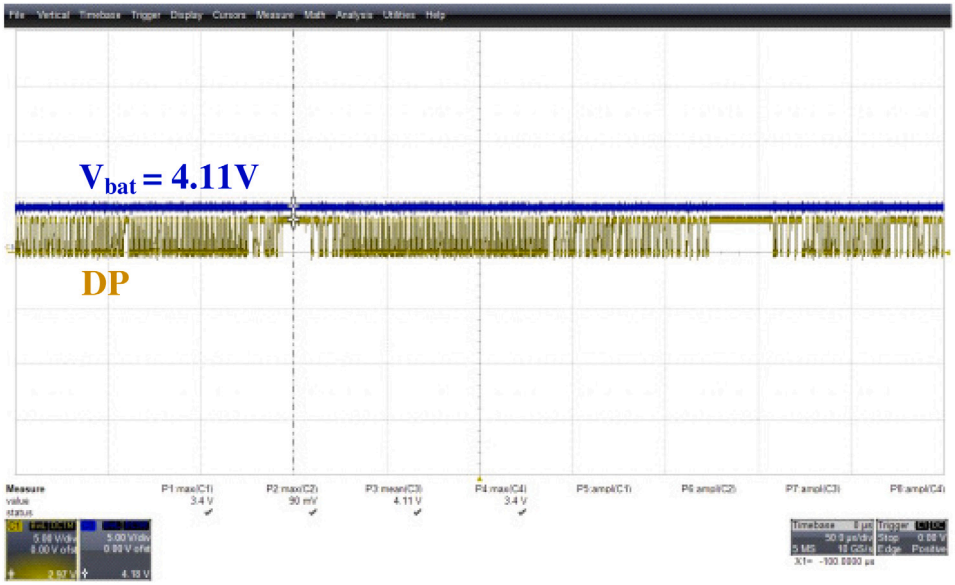



**Fig. 25.** Experiment 4: PFM pulse signal when the battery voltage reaches full charge.

based on measurement results. Moreover, when CV mode is activated by the energy harvesting circuit, it employs PFM making Li-ion battery voltage to fully charge at a limit of 4.2 V for overcharge protection of the battery. The CC and CV in the circuit provides an output voltage of 3.6 to 4.2 V for a high input voltage range of 10 to 20 V with maximum efficiency of 98%. The proposed circuit has the highest value of the FOM in comparison with the other recent researches.

## CRediT authorship contribution statement

**Chua-Chin Wang:** Conception and design of study, Analysis and/or interpretation of data, Writing – original draft. **Oliver Lexter July A. Jose:** Conception and design of study, Analysis and/or interpretation of data, Writing – original draft. **Po-Kai Su:** Acquisition of data, Analysis and/or interpretation of data. **Lean Karlo S. Tolentino:** Acquisition of data, Writing – review & editing. **Ralph Gerard B. Sangalang:** Acquisition of data, Writing – review & editing. **Jessica S. Velasco:** Analysis and/or interpretation of data, Writing – review & editing. **Tzung-Je Lee:** Analysis and/or interpretation of data, Writing – original draft.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Acknowledgment

We would like to thank the Ministry of Science and Technology, Taiwan, for partially supporting this study under grant MOST 109-2224-E-110-001-, MOST 109-2218-E-110-007-, MOST 110-2218-E-110-008-, and MOST 109-2221-E-110-079-. We would like to thank Taiwan Semiconductor Research Institute (TSRI) in National Applied Research Laboratories (NARLabs), Taiwan, for the fabrication of chip.

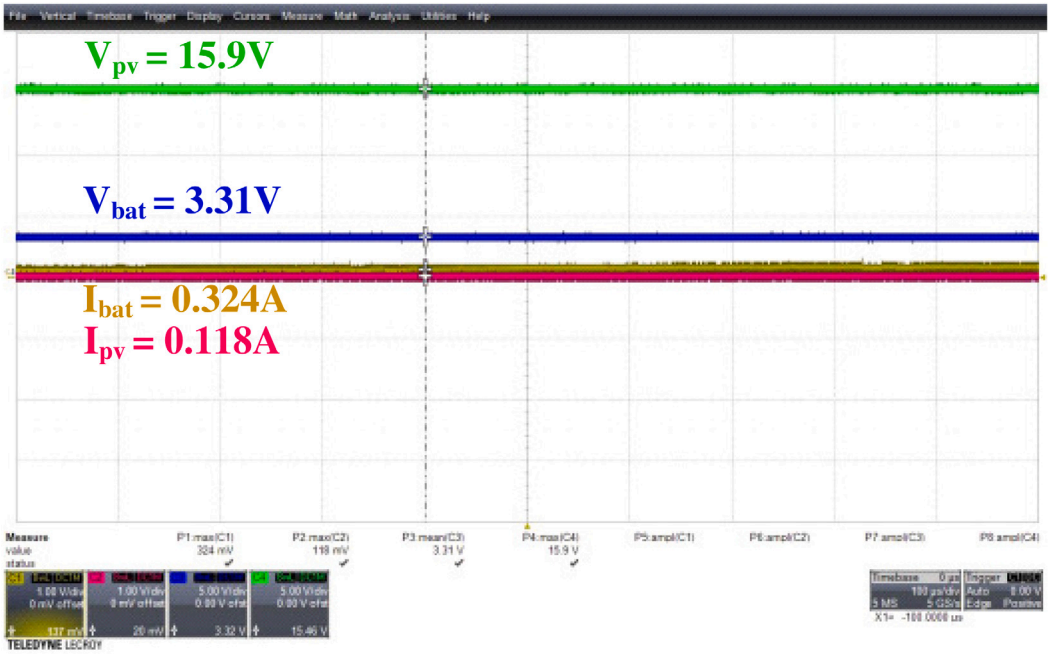



**Fig. 26.** Experiment 5: Input and output conditions at 15.9 V high input voltage.

**Table 5**
PV Energy-Harvester performance comparison.

| | ISSCC [3] | TPE [1] | VLSI-DAT [7] | ISVLSI [8] | HNICEM [9] | TCAS-II [16] | MEJ [17] | TPEL [18] | This work |
|---|---|---|---|---|---|---|---|---|---|
| Year | 2013 | 2013 | 2014 | 2015 | 2015 | 2020 | 2021 | 2021 | |
| Process | 0.35 μm | 0.35 μm | 0.18 μm | 0.18 μm | 0.35 μm | 0.18 μm | 0.18 μm | 0.18 μm | 0.5 μm |
| Method | Sectored Hill-Climbing | Quasi-P&O | P&O | P&O | RCC | P&O | D&AFOCV | P&O | P&O |
| Input voltage | 0.5 ~ 2 V | 3.5 ~ 5.4 V | 0.5 ~ 1.1 V | 0.3 ~ 0.7 V | 16 V | 2 ~ 7.2 V | 30 mV ~ 1 V | 0.6 ~ 1.15 V | 10 ~ 20 V |
| Output voltage | 4.2 V | N. A. | 1.2 ~ 1.8 V | N. A. | 5 V | 3.3 ~ 3.6 V | 1 V | 1.2 ~ 1.8 V | 3.6 ~ 4.2 V |
| Frequency (kHz) | 500 | 530 | N. A. | 1000 | 10 | N. A. | 0.94 | N. A. | 1000 |
| Throughput (W) | 0.5 | 27 | 0.045 | 0.15 | 30.64 | 0.0012 | – | 0.0001~0.003 | 5 |
| Efficiency | 99% | 95% | 90% | 95% | 97.42% | 98% | 91.15% | 94.7% | 57.16%(worst) ~98%(peak) |
| Power Consumption (mW) | 3.4 | 0.56 | N. A. | N. A. | N. A. | 0.009 | 0.03 (min.) | N. A. | 20 |
| Chip area ($mm^2$) | 1.625 | 0.45[a] | 1.43 | 2.373[b] | 0.21[b] | 0.882 | 0.16892 | 0.9486 | 12.53 |
| FOM[c] | 1.98 | 5.13 | 0.99 | 0.665 | 15.59 | 7.06 | 0.9115 | 1.089 | 19.6 |

[a]Control circuit area of [1] is only indicated.
[b]Only the core area is stated.
[c]FOM is the product of the peak MPPT efficiency and maximum input voltage.

## References


[1] R. Enne, M. Nikolic, H. Zimmermann, A Maximum Power-Point Tracker without Digital Signal Processing in 0.35$\mu$m CMOS for Automotive Applications, in: Proc. IEEE International Solid-State Circuits Conference Digest of Technical Papers, 2012, pp. 102–103.

[2] R. Enne, M. Nikolić, H. Zimmermann, Dynamic integrated MPP tracker in 0.35 μm CMOS, IEEE Trans. Power Electron. 28 (6) (2013) 2886–2894.

[3] T.-H. Tsai, K. Chen, A 3.4mW Photovoltaic Energy-Harvesting Charger with Integrated Maximum Power Point Tracking and Battery Management, in: Proc. IEEE International Solid-State Circuits Conference Digest of Technical Papers, 2013, pp. 72–73.

[4] W.-C. Liu, Y.-H. Wang, T.-H. Kuo, An adaptive load-line tuning IC for photovoltaic module integrated mobile device with 470μs transient time, over 99% steady-state accuracy and 94% power conversion efficiency, in: Proc. 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, 2013, pp. 70–71.

[5] T.-W. Hsu, H.-H. Wu, D.-L. Tsai, C.-L. Wei, Photovoltaic energy harvester with fractional open-circuit voltage based maximum power point tracking circuit, IEEE Trans. Circuits Syst. II: Express Briefs 66 (2) (2019) 257–261.

[6] D.-L. Tsai, H.-H. Wu, C.-L. Wei, A low-power-consumption boost converter with maximum power tracking algorithm for indoor photovoltaic energy harvesting, in: Proc. 2017 IEEE Wireless Power Transfer Conference (WPTC), 2017, pp. 1–3.

[7] S.-Y. Wang, H.-H. Wu, C.-L. Wei, An integrated boost converter with maximum power point tracking for solar photovoltaic energy harvesting, in: Technical Papers of 2014 International Symposium on VLSI Design, Automation and Test, 2014, pp. 1–4.

[8] Y. Sugimoto, The Solar Cells and the Battery Charger System Using the Fast and Precise Analog Maximum Power Point Tracking Circuits, in: Proc. 2015 IEEE Computer Society Annual Symposium on VLSI, 2015, pp. 597–602.

[9] L.K.S. Tolentino, F.R.G. Cruz, R.G. Garcia, W.-Y. Chung, Maximum power point tracking controller IC based on ripple correlation control algorithm, in: Proc. 2015 International Conference on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment and Management (HNICEM), 2015, pp. 1–6.

[10] C.-C. Wang, G.-X. Liu, A 1.5A 88.6% Li-ion Battery Charger Design using Pulse Swallow Technique in Light Load, in: Proc. IEEE International Symposium on Circuits and Systems (ISCAS), 2019, pp. 1–4.

[11] Datasheet: Poly-Crystalline Solar Panel, https://www.invensun.com/solar-panels/5w-solar-panel.

[12] K.J. George, Direct control method applied for improved incremental conductance MPPT using SEPIC converter, in: Proc. 2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE), 2014, pp. 1–6.

[13] V.V. Ramana, D. Jena, Maximum power point tracking of PV array under non-uniform irradiance using artificial neural network, in: Proc. 2015 IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES), 2015, pp. 1–5.

[14] A. Trivedi, A. Gupta, R.K. Pachauri, Y.K. Chauhan, Comparison of Perturb & Observe and Ripple correlation control MPPT algorithms for PV array, in: Proc. 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), 2016, pp. 1–5.

[15] M.G. Batarseh, M.E. Za'ter, Hybrid maximum power point tracking techniques: a comparative survey, suggested classification and uninvestigated combinations, Sol. Energy 169 (2018) 535–555.

[16] L. Liu, C. Huang, J. Mu, J. Cheng, Z. Zhu, A P& O MPPT with a novel analog power-detector for WSNS applications, IEEE Trans. Circuit. Syst. II: Express Briefs 67 (10) (2020) 1680–1684.

[17] G. Saini, M.S. Baghini, An energy harvesting system for time-varying energy transducers with FOCV based dynamic and adaptive MPPT for 30 nW to 4 mW of input power range, Microelectron. J. 114 (2021) 1–13.

[18] J.-Z. Yan, W.-H. Pan, H.-H. Wu, T. Hsu, C.-L. Wei, Photovoltaic energy harvesting chip with p & o maximum power point tracking circuit and novel pulse-based multiplier, IEEE Trans. Power Electr. 36 (11) (2021) 12867–12876.