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A 15.13 mW 3.2 GHz 8-bit carry look-ahead adder using single-phase all-N-transistor logic

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ABSTRACT

Adders are critical to the efficiency of arithmetic circuits in battery-powered electronic devices. This study demonstrates an 8-bit CLA (carry look-ahead adder) using single-phase ANT logic to increase the computation speed and reduce the power dissipation simultaneously. The single-phase ANT has no internal loop that optimizes the efficiency of the prior ANT. Utilizing a TSMC 40-nm technology, the proposed 8-bit CLA is fabricated. It attains the highest operating frequency of 3.2 GHz and the lowest normalized PDP (power delay product) by on-silicon measurement for 20 pF load.

1. Introduction

The increasing demand for battery-powered portable electronic systems, such as mobile phones, tablets, laptops, etc., raises concerns about speed and power usage [1]. Adders, as one of mentioned application essential building components, play a critical role in arithmetic circuit efficiency. Since addition is the most used operation in arithmetic circuits, research for effective adder architectures has always been a hot topic [2]. Static and dynamic logics are the two main techniques in adder circuit design. The integrated circuit architecture of a static adder is more complex and requires a significant amount of power and area. Dynamic CMOS gates are considered to be more effective due to the smaller parasitic capacitance and absence of output glitching [3]. The increase in power dissipation during higher switching activity is the primary issue of dynamic adders.

The overall power consumption of digital circuits is mainly divided into two types: dynamic and static. Dynamic power dissipation occurs when the device is in active mode, whereas leakage dominates static power consumption. All-N Transistors (ANT) logic is a dynamic circuit that consists of stacked series of NMOS (N-block) for logic operations [4]. The NMOS in the N-block requires lower V_{th} compared to PMOS devices, resulting in reduced power consumption and a smaller area. However, as the number of stacked NMOS devices in the N-block increases, prior ANT circuit's operation speed decrease with higher delay [5]. The charge and discharge in another ANL circuit are easily affected by the large value of gate capacitance, which leads to glitch problems [6].

This research presents a single-phase ANT logic architecture that obtains a low PDP (power delay product) solution. The topology does not have an internal loop that primarily affects prior ANT power consumption and delay. Its functionality is justified through a prototype fabricated using 40-nm CMOS technology.

The prior ANT logic design is briefly described in Section 2.1. The proposed Single-Phase ANT logic is addressed in Section 2.2. Single-phase ANT logic-based 8-bit CLA is thoroughly described in Section 2.3. The measurement results are demonstrated in Section 3 and conclusion is presented in Section 4.

2. Single-phase ANT logic

2.1. Prior ANT logic design

The prior ANT topology has an internal feedback loop, as illustrated in Fig. 1. Prior ANT logic enters the evaluation state when the clock input is "1", producing a logical output based on the N-block [4,7]. When the input clk = "0", ANT logic enters the precharge state, generating the same output as the previous state. The following issues that may affect the prior ANT logic functionality are listed.

1. During the logic evaluation, the loop formed by MN_{103} and MP_{103} may cause hysteresis and additional delay.
2. The big loading of the clk signal that drives three transistors in a single ANT may cause hold and setup time hazards.
3. Lastly, a total of 7 transistors in addition to the N-block consumes a large area.

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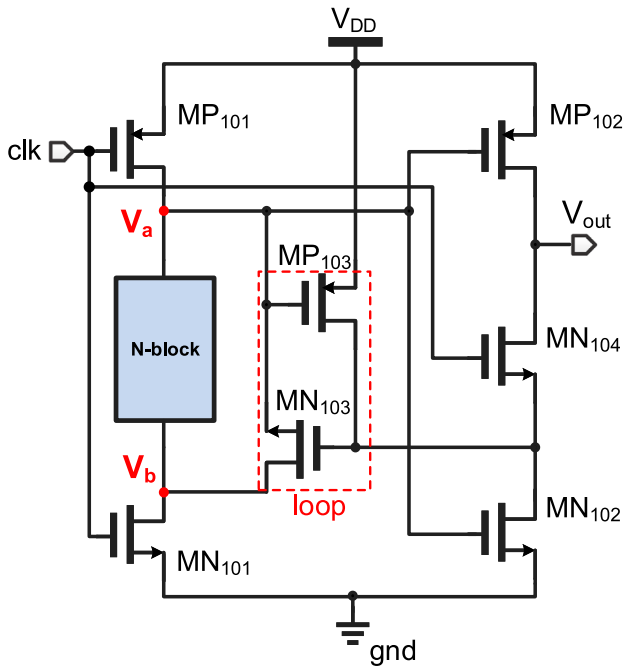

Fig. 1. Prior ANT Logic.

Table 1
Summary of single-phase ANT logic operations.

Stage	Transistor state		Output (V_Y)
Precharge(clk = 0)	MP_{201} on MN_{202} on MN_{203} off		Previous state
Evaluation(clk = 1)	Condition-1		V_{DD}
	N-block on MN_{202} off MP_{202} on MN_{203} on		
	Condition-2		0 to V_{DD}
	N-block off MN_{203} on MP_{202} off MN_{202} on	N-block on MN_{203} on MP_{202} on MN_{202} off	
	Condition-3		V_{DD} to 0
	N-block off MN_{203} on MP_{202} off MN_{202} on		
	Condition-4		0
	N-block off MN_{203} on MN_{202} on MP_{202} off		

To minimize hysteresis and improve the efficiency of this previous ANT design, the internal loop shall be removed. This will also improve circuit evaluation speed and reduce the total number of transistors in the auxiliary circuit. In addition, decreasing the voltage across V_A and switching off the output block of the ANT will reduce its power consumption even more.

2.2. Single-phase ANT logic

Fig. 2(a) shows the topology of the proposed single-phase ANT. Unlike the prior ANT, the absence of the internal loop will fasten the discharge and charge activity of the inverter formed by MP_{202} and MN_{202}. Furthermore, an RC delay produced by MN_{201} will reduce potential errors at the gate drives of MP_{202} and M_{202}. The voltage across node V_A achieves $V_{DD}-V_{th}$, which provides a small voltage swing to the inverter's input. It will lessen the power dissipation of the proposed ANT.

The output waveform for the proposed ANT's operation is shown in Fig. 2(b). The operation of the ANT is divided into two stages; precharge and evaluation.

1. **Precharge:** When clk = 0, the ANT goes to the precharge. In this stage, MP_{201} is on, MN_{203} is off, while MN_{201} will always be on due to its gate drive equal to V_{DD}. MN_{202} is on and MP_{202} is off, since the voltage across node V_A is $V_{DD}-V_{th}$. V_Y produced an output based on the previous state.
2. **Evaluation:** The ANT logic enters the evaluation stage when clk = 1. The evaluation stage has four conditions depending on the output V_Y's previous state and the "on" and "off" state of the N-block. All the conditions are explained as follows.
   - **Condition 1:** Node V_A is discharged via N-block to gnd, when N-block is on. In this condition, MN_{202} is off, and MP_{202} is on. V_Y is then charged to V_{DD}.
   - **Condition 2:** When N-block is off, and the voltage across node V_A is $V_{DD}-V_{th}$, MP_{202}, and MN_{202} are off and on, respectively, to pull V_Y to gnd. The voltage at node V_A is discharged to gnd through MN_{203} and N-block, once if the N-block is turned on. At this point, MN_{202} will be switched off, and MP_{202} will be on, pulling V_Y up to V_{DD}.
   - **Condition 3:** This condition occurs when the voltage at node V_A is $V_{DD}-V_{th}$ and N-block is off. Due to the state of MP_{202} and MN_{202}, which are off and on, respectively, output V_Y will be discharged from V_{DD} to gnd.
   - **Condition 4:** Node V_A turns on MN_{202} and turns off MP_{202} when N-block is off, pulling output V_Y to the gnd.

Table 1 summarizes the four conditions for single-phase ANT logic in the evaluation phase.

2.3. Single-phase ANT logic-based 8-bit CLA

Fig. 3 illustrates the 8-bit CLA block design based on the proposed single-phase ANT logic. Inputs A[0-7] and B[0-7] are coupled to 8-bit G/P generator. A 1-bit generation (G_i) and propagation (P_i) circuit are shown in Figs. 4 and 5, respectively. Eq. (1) defines the equation for G_i and P_i [8,9].

$$P_i = A_i \oplus B_i, \qquad G_i = A_i B_i \tag{1}$$

Fig. 6 shows the carry generation circuit using single-phase ANT logic in which input is coupled to the output of the generation circuit. Its output signal (C_i) is characterized by Eq. (2) [8,9].

$$C_i = G_i + P_i G_{i-1} + \cdots + P_i P_{i-1} \ldots P_0 C_{in} \tag{2}$$

Fig. 7 illustrates the sum generation circuit, whose output signal (S_i) is represented by Eq. (3) [8,9]. The generation and propagation circuits' output is connected to the sum generation's input. The output of the sum generation circuit is connected to 3 stages of tapered buffers, as shown in Fig. 3.

$$S_i = P_i \oplus C_{i-1} \tag{3}$$

The demand for an increasing number of devices in an IC for higher operating speeds and functionality leads to circuit optimization issue, such as propagation delay, power consumption, and area [10]. These factors are mainly affected by the transistor size. Increasing the size of the transistor improves the propagation delay but also results in additional power consumption due to the increase in the gate capacitance. The transistor sizes in the proposed single-phase ANT logic are properly

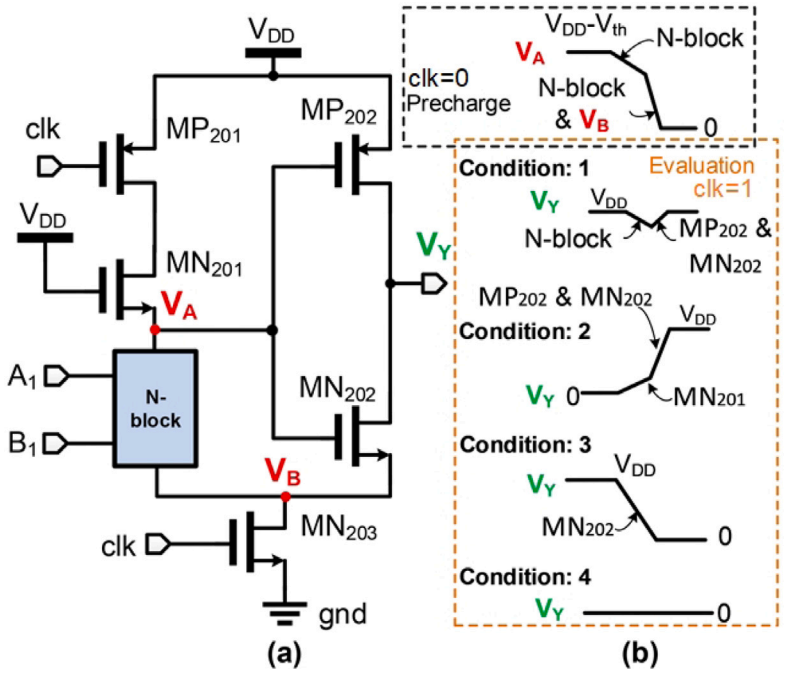

Fig. 2. Single-phase ANT logic (a) proposed schematic and; (b) output waveforms.

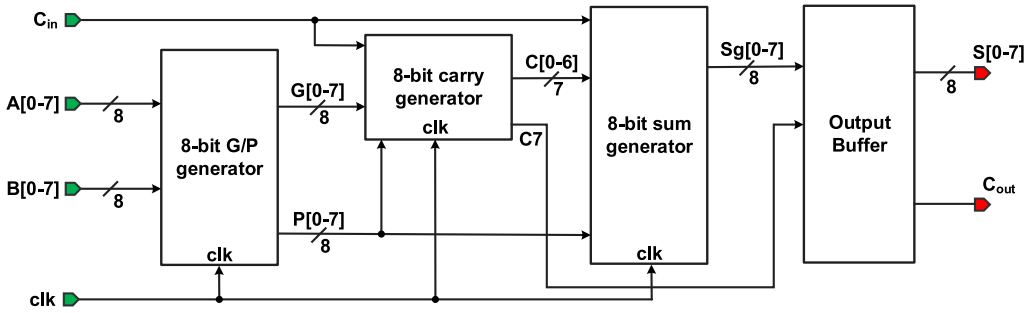

Fig. 3. 8-bit CLA block diagram.

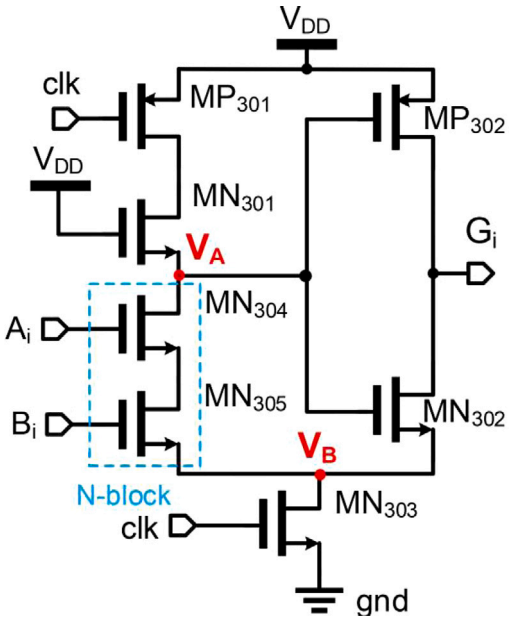

Fig. 4. 1-bit generation circuit.

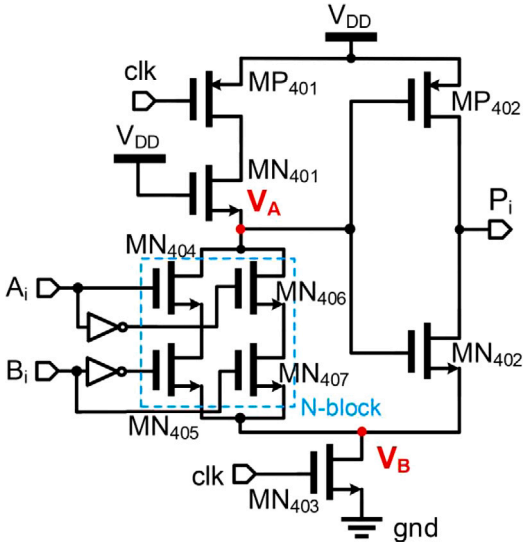

Fig. 5. 1-bit propagation circuit.

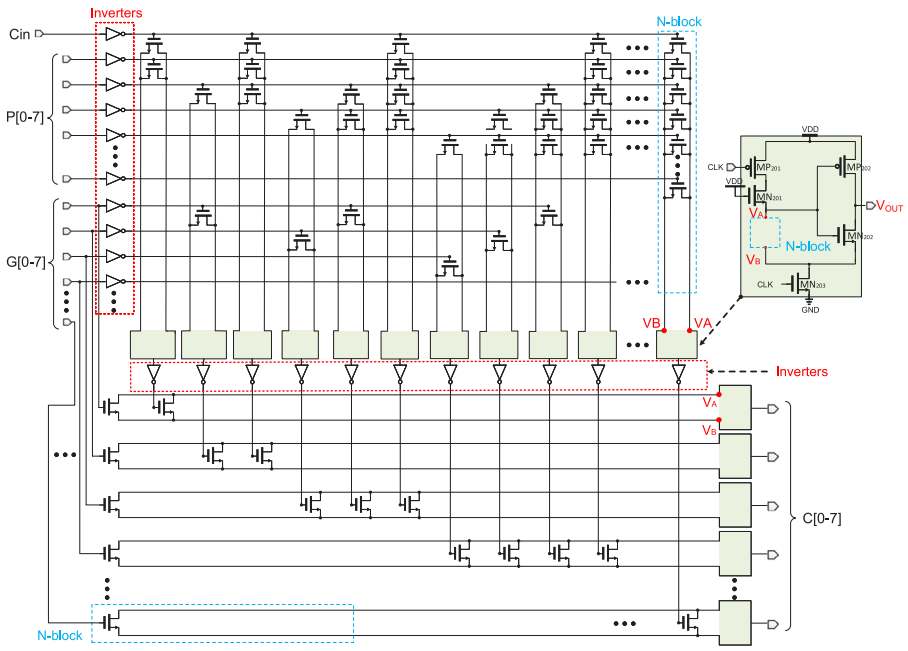

Fig. 6. 8-bit carry generation circuit.

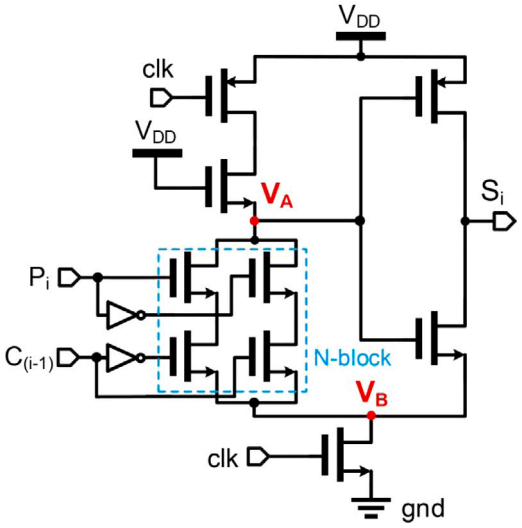

Fig. 7. 1-bit sum generation circuit.

Table 2
AND/XOR ANT Logic block sizing.

Fig. 4, Fig. 5 transistors	W/L ratio
MP_{301}, MP_{401}	75/2, 75/2
MP_{302}, MP_{402}	75/2, 75/2
MN_{301}, MN_{401}	25/1, 25/1
MN_{302}, MN_{402}	75/4, 75/4
MN_{303}, MN_{403}	75/2, 75/2
MN_{304}, MN_{305}	5/1, 10/1
MN_{404}, MN_{405}	5/1, 10/1
MN_{406}, MN_{407}	5/1, 10/1

Table 3
Test 1 Input pattern and equivalent output.

Input			Output	
C_{in}	A_7 - A_0	B_7 - B_0	C_{out}	S_7 - S_0
0	0000 1010	0000 0010	0	0000 1100
0	0000 0010	0000 1101	0	0000 1111
0	0000 1111	0000 0000	0	0000 1111
0	0000 0011	0000 0001	0	0000 0100
0	0000 1111	0000 1111	0	0000 1110
0	0000 1000	0000 1010	0	0000 0010
0	0000 0000	0000 0000	0	0000 0000
0	0000 0011	0000 0100	0	0000 0111

tuned by equalizing the rise time and the fall time of the output signals. Referring to Fig. 2, MP_{201} and MP_{202} must have a higher value of resistance to match with MN_{201} and MN_{202}, with a 2:1 aspect ratio to achieve an equal magnitude of currents [11].

Referring to Fig. 4, the transistors in the N-block are connected in series. The width of MN_{305} must be twice as large as MN_{304}. If the transistor in the N-block is connected in parallel, as shown in Fig. 5, the width of the transistors must be equal (namely, $MN_{404} = MN_{406}$, $MN_{405} = MN_{407}$). Table 2 summarizes the overall transistor sizes of the proposed ANT.

3. Realization and measurement

The 8-bit CLA based on the single-phase ANT logic is implemented using TSMC 40-nm CMOS process. Shown in Fig. 8 is the die photo of the 8-bit CLA with 797.565×804.395 μm^2 and 154.776×179.165 μm^2 chip area and core area, respectively.

Fig. 9 shows the measurement set-up for this research. The clk, A0 – A7, and B0 – B7 inputs of the CLA were generated by the Agilent 82 150 pattern generator. The 0.9 V supply is provided by Agilent N6761A power supply. Lastly, the output waveform of our chip is observed using high-frequency Keysight DSAV134 and MXR254A oscilloscopes.

Tables 3 (Test 1) and 4 (Test 2) tabulates the input pattern and equivalent outputs of the 8-bit CLA at clk = 3.2 GHz. Fig. 10(a) and (b) show the corresponding measurement waveforms for Test I, and Fig. 11(a) and (b) for Test II. Both measurement results produced a logic level the same as the equivalent output from Tables 3 and 4, which demonstrate the performance and functionality of the proposed single-phase ANT-based CLA.

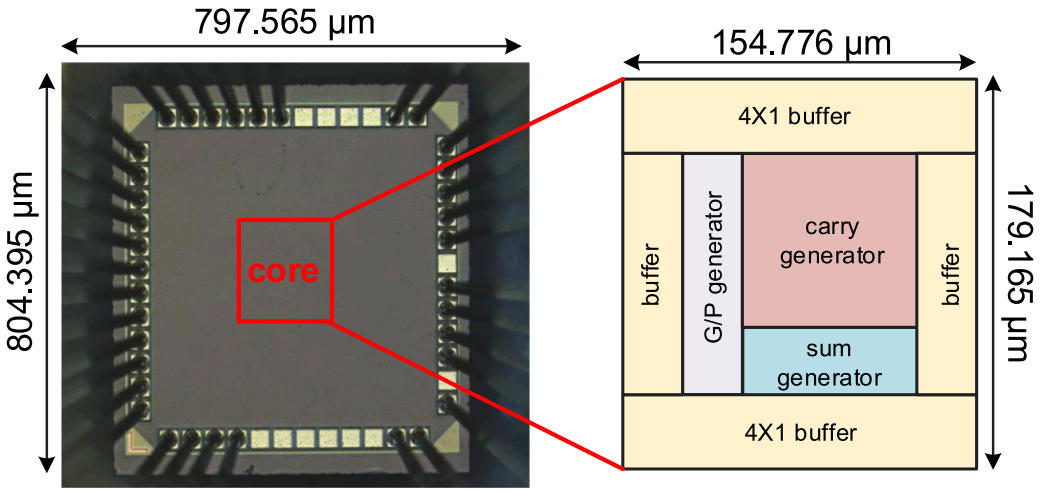

Fig. 8. Die photo and layout of the proposed single-phase ANT-based CLA.

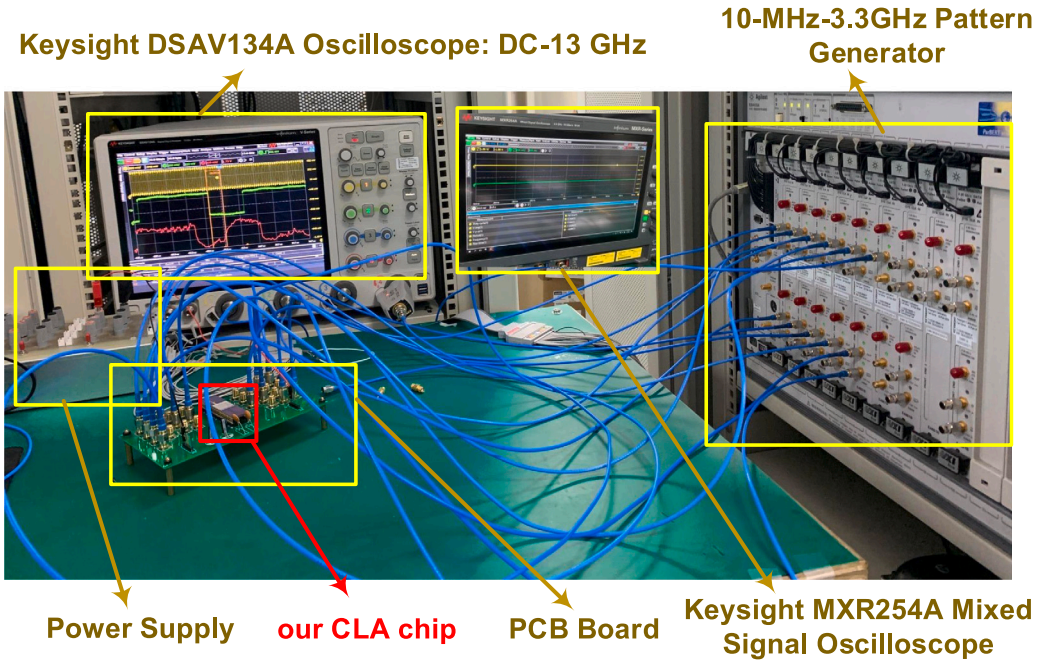

Fig. 9. Measurement set-up (TSRI Tainan Lab.).

Table 4
Test 2 Input pattern and equivalent output.

Input			Output	
C_{in}	A_7 - A_0	B_7 - B_0	C_{out}	S_7 - S_0
0	1010 0000	0010 0000	0	1100 0000
0	0010 0000	1101 0000	0	1111 0000
0	1111 0000	0000 0000	0	1111 0000
0	0011 0000	0001 0000	0	0100 0000
0	1111 0000	1111 0000	1	1110 0000
0	1000 0000	1010 0000	1	0010 0000
0	0000 0000	0000 0000	0	0000 0000
0	0011 0000	0100 0000	0	0111 0000

Fig. 12 shows the histogram and eye diagram measurement of the proposed single-phase ANT logic-based CLA. The eye diagram and histogram have a height and width of 213 mV and 8.76 ns, respectively.

Table 5 summarizes recent studies on CLA adders. Our 8- bit CLA operates at a clock frequency of 3.2 GHz (maximum) at the highest value of C_{load} = 20 pF. Notably, this study provides the lowest measured normalized PDP, indicating less energy lost per switching events than all the prior works as shown in Fig. 13.

4. Conclusion

This study is focused on single-phase ANT logic-based 8-bit CLA implemented in TSMC 40-nm CMOS technology. The single-phase ANT design does not have an internal loop reducing its power consumption

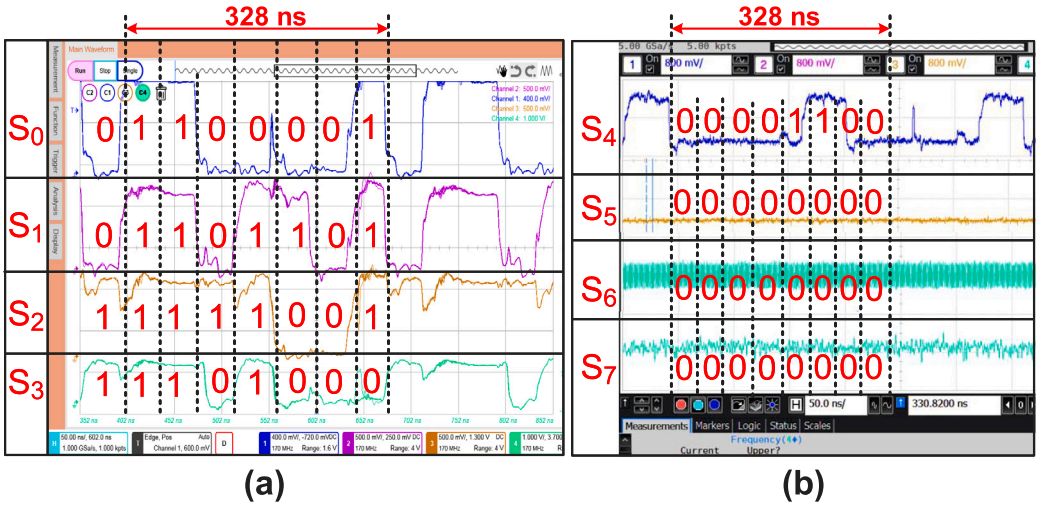

Fig. 10. Test 1 (a) S0 ~ S3 and (b) S4 ~ S7 at 3.2 GHz operating frequency.

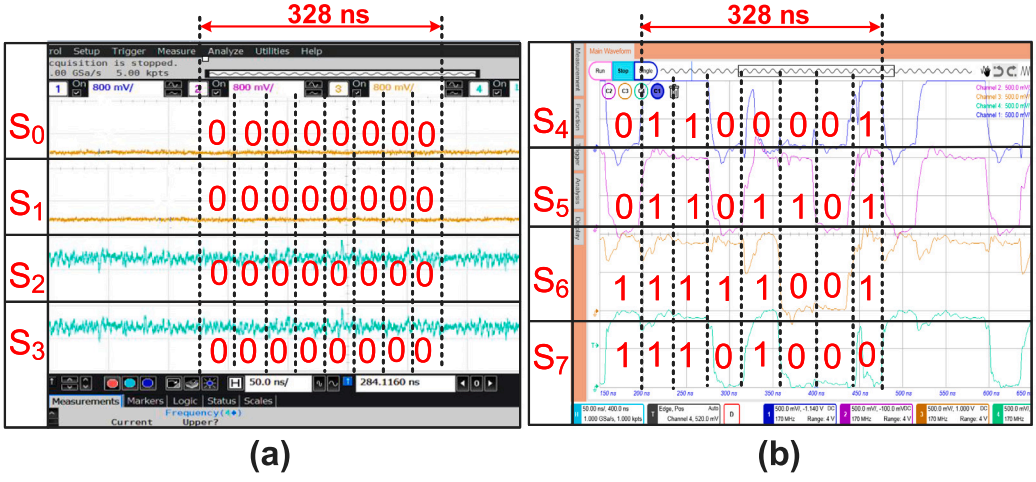

Fig. 11. Test 2 (a) S0 ~ S3 and (b) S4 ~ S7 at 3.2 GHz operating frequency.

Table 5
Performance comparison with several prior works.

Parameter	[1]	[12]	[13]	[14]	[15]	[7]	This work
Year	2017	2018	2019	2020	2021	2022	2023
Publication	RISE	TVLSI	SEC	TCAS	TN	CSSP	Integration
Verification	Simul.	Simul.	Simul.	Simul.	Simul.	Meas.	Meas.
Technology (nm)	45	65	28	45	45	16	40
Supply voltage (V_{dd})	1.2	1.2	0.9	0.8	1	0.8	0.9
Length (bits)	1	1	8	1	1	8	8
Max. clk freq (GHz)	0.5	1	0.5	0.1	0.1	0.8	3.2
Delay (ns)	0.215	0.0518	1.117	0.0657	0.027	8.79	8.57
Power consumption (mW)	0.00406	0.00444	0.008865	0.00048	0.0024	28.8	15.13
Loading capacitance (pF)	0.01	0.01	0.01	0.006	0.001	20	20
Core area (mm^2)	N/A	N/A	N/A	N/A	N/A	0.0313	0.027
Normalized area[a]	N/A	N/A	N/A	N/A	N/A	122.26	16.87
Nor. power[b] (mW)	0.564	0.3083	2.188	1.25	24	0.937	**0.2918**
Nor. power per bit (mW)	0.564	0.3083	0.273	1.25	24	0.117	**0.036**
Nor. area per bit	N/A	N/A	N/A	N/A	N/A	15.2825	**2.1087**
Nor. PDP (nJ)	12.124	1.597	244.4	13.687	648	0.1373	**0.125**

Note:

[a] $\text{Normalized area} = \frac{\text{Core Area } (mm^2)}{\text{Technology (nm)} \times \text{Technology (nm)} \times 10^6}$

[b] $\text{Nor. power} = \frac{\text{P (mW)}}{\text{Freq (MHz)} \times C_{load}\text{(pF)} \times V_{dd}^2(V)}$

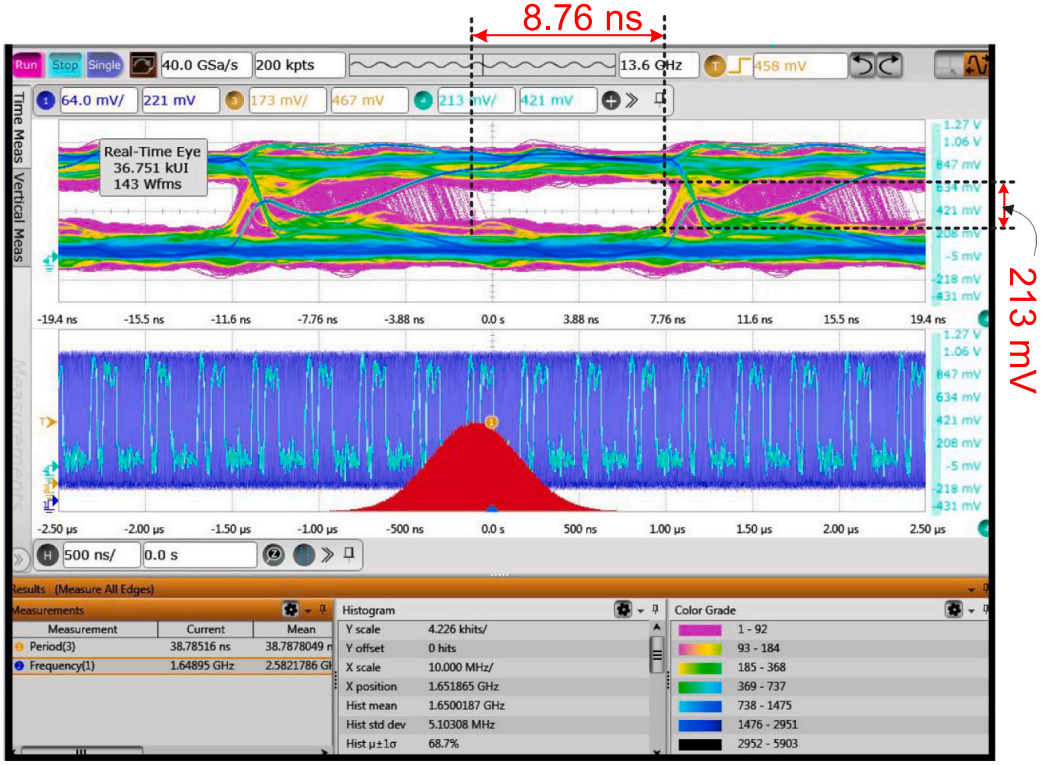

Fig. 12. 8-bit CLA jitter and histogram measurement.

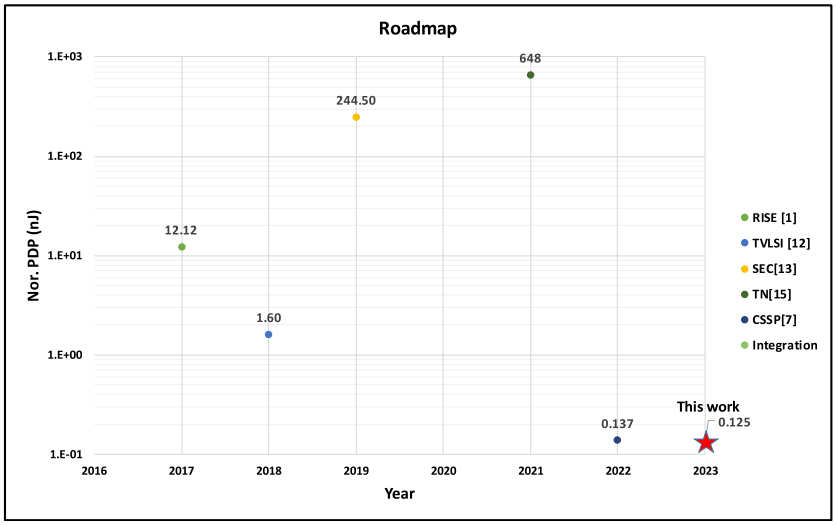

Fig. 13. CLA designs technology roadmap.

and improving the performance of the prior ANT. It is one of the two CLA designs that is physically fabricated at the highest C_{load} = 20 pF. It has a maximum operating frequency of 3.2 GHz. Notably, this work has the lowest PDP, which makes it very energy efficient.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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