A Practical Load-Optimized VCO Design for Low-Jitter 5V 500 MHz Digital Phase-Locked Loop*

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ABSTRACT

In high-speed digital systems and high-resolution display devices, the jitter effect of phase-locked loops (PLL) limits the system performance. Power supply noise coupling is one of the major causes of PLL jitter problems, especially with mixed-signal systems. The paper presents a targeted 5.0 V 500 MHz PLL which is implemented by a 0.6 um 1P3M digital CMOS technology. The features of the proposed design include a load-optimized 3-stage VCO, a frequency limiter RC circuit, and a ratioed VCO controlling current mirror. The jitter, thus, is reduced to 72.693 ps at 600 MHz at the presence of supply noise, while the sensitivity is limited to 286.6 ps/V. This high-noise immunity design allows that the PLL can be integrated with digital circuits.

1. INTRODUCTION

PLLs are often used in the I/O interfaces of digital ICs in order to hide clock distribution delays and improve the overall system timing [5] or high frequency clock generators [2], [3], [7]. However, the noisy environment in which the ICs operate might introduce unwanted jitter from the expected timing at the output of the PLL. With a demand on high frequency and high speed PLLs, the design of low jitter PLLs thus become very challenging. Though many PLL designs have been proposed [1], [4], [6], [7], several design factors have long been ignored. First, the lock time of the PLL should be as short as possible. Second, the lowest output frequency might not necessarily be zero. Third, the size ratio of the conventional ring oscillator type VCO (voltage controlled oscillator) should be tuned and might be the same at every stage of inverters. In this work, we present a PLL design including a load-optimized 3-stage VCO, a frequency limiter RC circuit, and a ratioed VCO controlling current mirror. The targeted frequency is 500MHz, while the output clock is ranged between 380 MHz and 600 MHz. The fast lock time is 95 us in the worst case. The entire design is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.6 um 1P3M CMOS technology and verified by HSPICE.

2. VCO Design for Low-Jitter PLL

As shown in Fig. 1, the entire PLL circuits consists of a PFD (phase-freq detector), a charge pump, a second order loop filter, a VCO and a digital divider. In our design, the reference input clock is given 20 MHz which can be easily produced by most of the commercial crystal oscillators.

2.1 Frequency limiter

Most of the PLLs are designed specifically for certain pre-determined operating frequency. Thus there is no need to sacrifice the lock time for the working frequency range from 0 MHz to a desired upper bound. Hence, we introduce a practical frequency limiter between the charge pump and the current mirror for ring oscillator in the VCO. The detailed frequency limiter is shown in Fig. 2. We tend to take advantage of the L/W ratio of NMOS M2 to clamp the output frequency range and the upper bound of this range such that the actually highest frequency of the PLL is not the same as that of the ring OSC. Besides, this highest output frequency of the output frequency range can be determined by adjusting the resistance of R1 in Fig. 2.

In contrast, M3 itself can be deemed as a nonlinear RC circuit which is able to control the lowest output operating frequency. The samller the L/W of M3, the lower the output frequency. However, the ring OSC will not function if the L/W of M3 is smaller than a certain value. The size of M3 is thus used as an adjustable mechanism to determine the range of the output frequency. Another major benefit of such a circuit is to reduce the noise coupling effect of power supply to the ring OSC besides the mentioned frequency limiting function.

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2.2 Load-Optimized Ring OSC

Conventionally the ring OSC of the VCO used in high frequency PLLs is composed of three cascaded inverters with equal size. The might lead to a problem if the output of the VCO is connected to a buffer. It indicates that the last stage of the OSC possesses two loads while the other stages have only one. If the buffer size is sufficiently large in order to drive large load, the output of the VCO will damp to a stable voltage value if Vin of the frequency limiter is small. Hence, we adopt a ratioed design for the cascaded inverters to optimize the loading at each stage. The sizes of the transistors used in the OSC are shown in Fig. 2.

2.3 Fast Lock Time Consideration and Compensation

The mentioned frequency limiter basically provides an almost pre-determined bias voltage at the input of the VCO. Referring to Fig. 3, the V-f diagram of the proposed VCO reveals that our design strictly focuses the targeted range, 500 MHz. The lock time will be drastically reduced owing to the none-zero output frequency given the lowest input voltage to the VCO. However, the drawback of the narrow band effect can be compensated by the digital frequency divider shown in Fig. 1.

3. Simulation Result and Chip Layout

To verify the correctness and functionality of the proposed design, we design the entire PLL circuit using TSMC 0.6 um 1P3M CMOS technology. The schematic and the layout are respectively shown in Fig. 4 and Fig. 5. The capacitors in the loop filter are composed of gate-to-bulk capacitors of 50 parallel NMOS transistors, respectively. That is, the source and drain of these transistors are all grounded. The gain-bandwidth diagram is given in Fig. 6. The measured sensitivity and the jitter performance is summarized in Table 1. The comparison of our design and prior works are also illustrated in the following Table 2 and Table 3. Basing on the results in the tables, the proposed design is superior to the prior works regarding the jitter and lock time.

4. Conclusion

A novel and practical VCO design for digital PLL is presented in this paper. Besides shortening the lock time, the jitter caused by noise of the power supply is also reduced. Meanwhile, the loading effect of the ring OSC is taken into consideration. Simulation results provided by HSPICE reveals the value of the entire design.

5. REFERENCES

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jitter without supply noise	±21.023ps
Jitter given noise of 0.5V 1MHz square wave	-70.6/+72.693ps
Sensitivity	286.6ps/V

Table 1 : cycle–to-cycle VCO jitter at 600Mhz @5V 0.6 um 1P3M CMOS

	Lock time	Jitter	Lock Freq.	Technology
[4]	N/A	80ps	250MHz	0.5um CMOS 3V
[5]	N/A	144ps	250MHz	0.5um CMOS 3.3V
[8]	N/A	81ps	130MHz	0.8um CMOS 5V
Ours	43u	160ps	480MHz	0.6um CMOS 5V

Table 2 : jitter comparison without noise presence

	Jitter p-p (ps)	**Std** (ps)	**Noise-Level** (v)	Sensitivity Ps/V	Freq. (MHz)	Technology
[1]	133	20.97	0.5	N/A	360	0.5um CMOS 3.3V
Ours	-70.6/+72.7	52.2	0.5	286.6	480	0.6um CMOS 5V

Table 3 : jitter comparison with noise presence

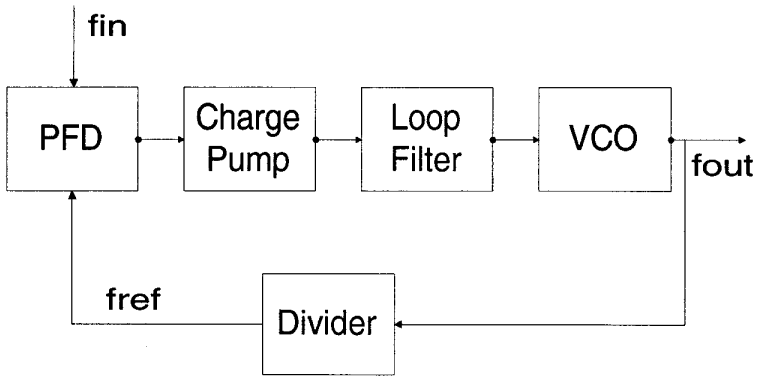

Fig. 1: Block diagram of PLLs

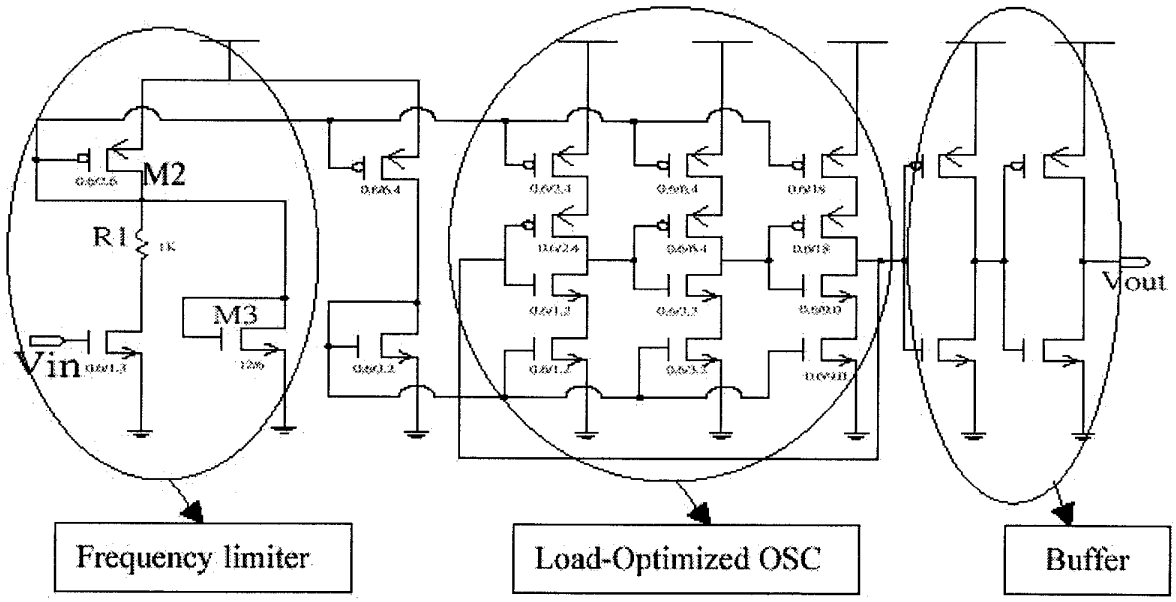

Fig. 2: Schematic of the propose VCO

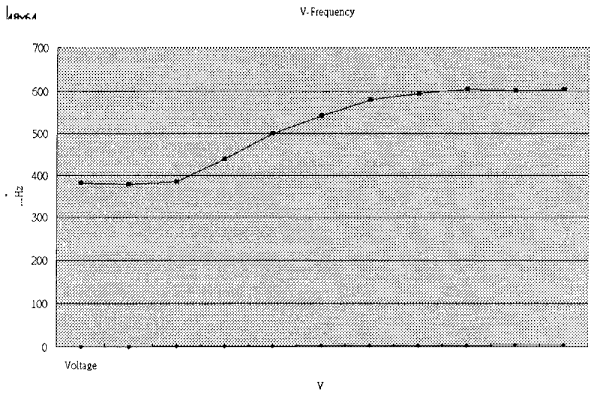

Fig. 3: V-f diagram of VCO

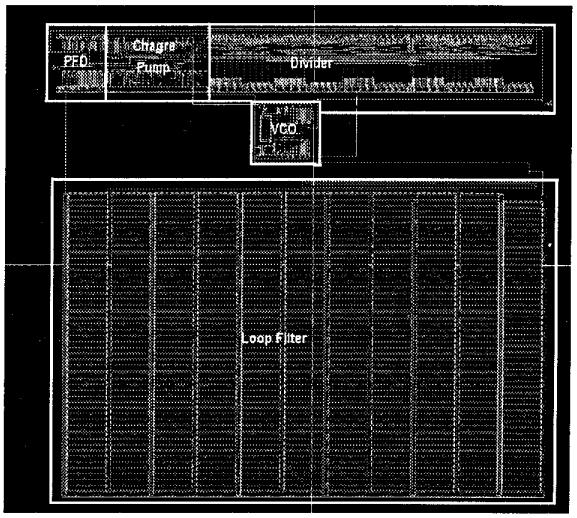

Fig 5: Layout of the propose PLL

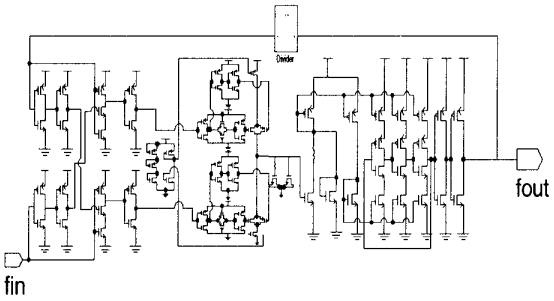

Fig. 4: Schematic of the entire PLL

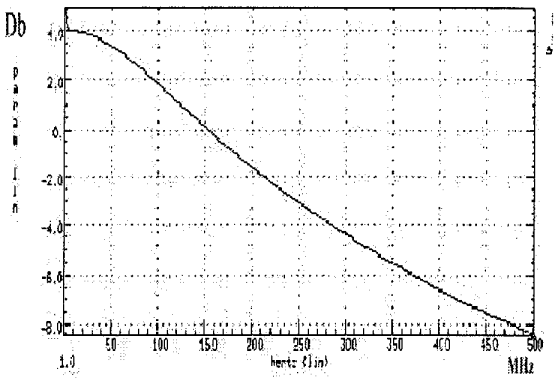

Fig. 6: Gain-bandwidth of the loop filter