A LOW-COST PLASMA DISPLAY PANEL DATA DISPATCHER FOR IMAGE ENHANCEMENT

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ABSTRACT

Plasma Display Panel (PDP) is one of the best solutions for TVsets, but its retail price remains higher than that of CRTs. This paper proposes a low-cost PDP Data dispatcher which focuses on converting the image signal inputs into the PDP display format and reducing the numbers of components as well as the cost used in the Dispatcher module at the same time.

1. INTRODUCTION

Many efforts have been thrown on improving the Plasma Display driving method [1], picture quality [2] and the driver ICs. However, there are only a few people paying attention to the Plasma Display Panel Data dispatcher [3], which is one of the most important parts in the whole PDP set. Statistically, the dispatcher consumes 10% of the PDP prime cost. Most of prior PDP Data dispatchers used large input buffers to convert image signals to the format requested by high-voltage data driver ICs (HVDIC, e.g., STV 7699). Meanwhile, these data are stored in the SDRAM modules. The data in SDRAMs are re-arranged by output buffers for the display at last. These designs consumed too many registers in data transformation among the input signals, the input buffers, the SDRAMs, and the output buffers. Unavoidably, these prior works needed 4 or 5 advanced and large FPGAs to carry out this dispatcher.

2. PLASMA DISPLAY PANEL DATA DISPATCHER

We propose a novel design to reduce these I/O buffers by using SRAMs instead of SDRAMs to achieve the same converting functions while alleviate the so-called "dynamic false contours" problem. The PDP Data dispatcher consists of an Average Picture Level (APL) module, an 8-to-10 sub-field translator, a control module, an output buffer module, an SRAM module, and a High-voltage control signal generator. Figure 1 shows the entire proposed PDP dispatcher architecture.

Average Picture Level (APL) module
The APL module determines the brightness of the image. It will reduce the afterimage and image sticking effects, and also can increase phosphor's lifetime if the brightness is larger than a pre-determined threshold. The final result will be signaled to the High-voltage control signal generator.

8-to-10 sub-field translator
The PDP displays natural colors through "Address Display Separate" (ADS) method, which is 1 TV frame consists of 8 sub-fields and each sub-field represents a different portion of brightness. Nevertheless, the ADS introduces a serious image defect named "dynamic false contours." We reduce the dynamic false contours by redefining the number of sub-fields from 8 to 10 in the sub-field translator. The timing format is shown in Figure 2.

Control module
We align the pixel data in the input buffers according to the data format of the HVDIC. These buffered data are stored in the SRAM module. We only utilize two byte-wide registers alternatively to buffer pixel data which are written to SRAM module following the buffering operations. The control module is also in charge of the timing control of the SRAM module and the output buffers, and commanding the high-voltage control signal generator.

SRAM module
The HVDIC module is divided into 2 sections, which are respectively in charge of the display operations of odd-numbered driver ICs and even-numbered driver ICs. The HVDIC module delivers pixel data in 64 clocks by the following manner: the first clock cycle feed sub-field of pixel 1 data (R,G,B) to the 1st drive IC and the next clock cycle feed sub-field of pixel 33 data to the 2nd driver IC, ..., and so on. Hence, we arranged the data by 3(HVDIC format)*8 (a divisor of 32)=24 in one SRAM line. The output buffer is, thus, only responsible for reading the data. Figure 3 shows the data arrangement in the SRAM module.

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0-7803-7300-6/02 $17.00 © 2002 IEEE

Output buffer
This module reads data from the SRAM module. The read data are output to HVDIC. Meanwhile, it also buffers the control signals from the control module to HVDIC, when the control module receives the address scan fetch signal from the High-voltage control signal generator.

High-voltage control signal generator
This module converts driving voltage waveforms of which the formats are stored in a ROM into the control signals for the high-voltage switches in the Maintain board and the Scan board.

3. CONCLUSION

The proposed Plasma Display Panel Data dispatcher consists of 2 Altera 10K FPGA and 1 Xilinx SPARTAN FPGA. The PDP (supported by AU Optronics Corp.) displays an improved image shown in Figure 4. Our design reduces 20% of the cost and 50% of the data processing time, which in turn increases the sustain period for brightness control. The prior work [3] spent a total of 962.2 μs. On the other hand, besides the initialization to fill output buffer, our design operates pipelinedly which can continuously send the pixel data to the HVDIC module. Hence, the data processing time is shorten to 350 ns (initialization) + (25 ns*(64+2)*300) = 495.35 μs. Table 1 tabulates all of the comparisons.

	prior work [3]	our
FPGA No.	5	3
memory module	SDRAM	SRAM
input buffer reg.	4098	480
output buffer reg.	5120	1344
data processing time	962.2 μs	495.35 μs

Table 1: The hardware cost analysis

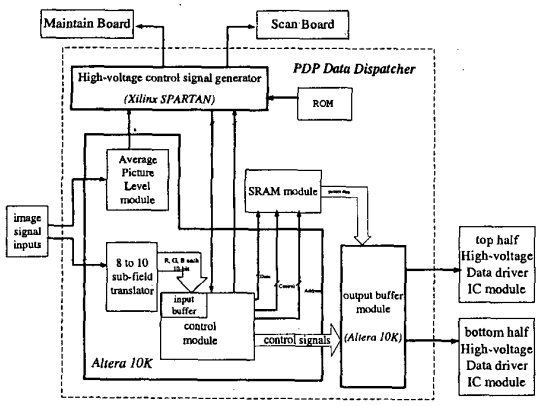

Figure 1: The proposed PDP Data dispatcher

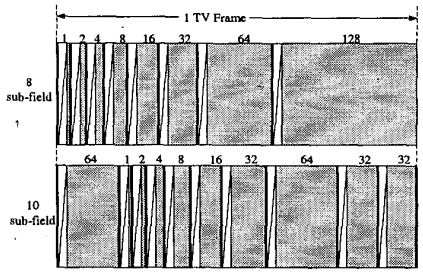

Figure 2: The 8 and 10 sub-field timing diagram

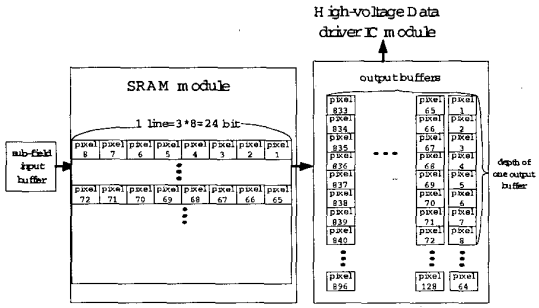

Figure 3: The data arrangement in SRAM module

Figure 4: Improved image on PDP

4. REFERENCES

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