A 1.2 GHZ PROGRAMMABLE DLL-BASED FREQUENCY MULTIPLIER FOR WIRELESS APPLICATIONS §

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ABSTRACT

A CMOS local oscillator using a programmable DLL-based frequency multiplier to synthesize carrier frequency from 1.1 GHz to 1.5 GHz is presented. The frequency of the output clock is 7× to 10× of an input reference clock. No LC-tank is used in the proposed design such that the power dissipation as well as the active area are drastically reduced. The design is carried out by TSMC 1P5M 0.25 μm CMOS process at 2.5 V power supply. The average lock time is optimally shortened by initializing the start-up voltage of the VCDTL (voltage-controlled delay tap line) at the midway of the working range. Meanwhile, the power dissipation of physical chip measurements is only 52.2 mW at 1.2 GHz output.

1. INTRODUCTION

Ever since the low-cost RF CMOS technology becomes the challenger of its conventional discrete counterpart [4], the quality of the local oscillator (LO) has been demanded to possess better phase-noise performance and lower power consumption [1].

Many CMOS RF transceivers were proposed, e.g., [5], and [1]. Although [5] proposed a fixed-frequency RF LO to block-downconvert the entire RF band to IF band, it requires another channel-select LO to downconvert the desired channel to baseband. [1] proposed a non-programmable design basing upon a DLL, but noise-prone and slow current-driven OPAMPs are used to construct the replica bias. What even worse in [1] is that larger inductors are required for LC-tanks to enhance the load impedance at the resonance frequency. Besides, none of these prior works is programmable. This paper, by contrast, describes an enhanced implementation of LOs using the programmable DLL-based frequency multiplier.

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2. DLL-BASED FREQUENCY MULTIPLIER

Most of the current wireless systems utilize a PLL-based synthesis approach typically implemented with a VCO. If such a design is intended to be implemented and integrated in a CMOS RF transceiver, the low-Q of the CMOS components will deteriorate the phase noise. The key to have a clean LO signal is take advantage of a high-Q reference clock. e.g., from a crystal clock source, such that the close-in VCO phase noise will be suppressed.

2.1. DLL-based architecture

The proposed programmable frequency multiplier is given as shown in Fig. 1, including a PFD (phase-frequency detector), a charge pump (CP), a loop filter (LF), a programmable VCDTL (voltage-controlled delay tap line), a positive edge collector (PEC), and a clock generator (CG). The design as well as the function of the PFD, the charge pump, and the LF, is well known in the literature. Regarding the function of the rest of the modules are described as follows.

VCDTL : It comprises a plurality of cascaded stages. One stage is composed of one delay cell and one demultiplexer (DEMUX). Such a serial of cascaded stages is called the tap line. The first stage of the tap line is driven by the external reference clock, f_{ref}, which is assumed to be crystally clean. At the output node of each stage, different clocks with different phase shift are generated, which is named $\phi_1, \ldots, \phi_{2n}$. The DEMUXs are controlled by external signal, $S1[1]$ to $S1[n]$, to determine the feedback path to PFD from VCDTL.

PEC : This module monitors the rising edge of those clocks generated in VCDTL. As soon as the rising edge is detected, a corresponding low pulse is triggered, e.g., $PULSE_2$, $PULSE_4$, ..., $PULSE_{2n}$. A low pulse train, $PULSE_{2\times i}$, namely the corresponding rise edge, is determined by every two adjacent generated clocks, i.e., ϕ_i and ϕ_{i+1}. The digital design to realize such a detection will be addressed in the following sections.

CG : The module is in charge of generating the desired frequency by reading the external selection signals, $S2[1]$ to $S2[n]$.

2.2. Circuit designs

The details of the modules in the proposed design are disclosed in this section. Notably, most of the designs are carried out by digital components in order to diminish the sensitivity problem of the prior works.

Programmable VCDTL : The schematic of the leftmost part of the tap line is shown in Fig. 2. The current through MP2 of the first delay cell is a mirror current of that via MP1. The amount of the current of MP2 determined the delay of each delay cell. Hence, it is voltage controlled. The current in MP1 is the summation of the currents through MN1 and MN2. MN2 is a fixed amount current sink as long as it is saturated. The current via MN1 is determined by the voltage at its gate, i.e., V_{ctrl}, which is supplied by the LP. The resistor R is a current limiter.

Notably, a simple thought to shorten the lock time is that the start-up voltage of V_{ctrl} is biased to the middle of the entire operating range. For instance, if the range of operating voltage is 1.4 V to 2.6 V, we initialize the V_{ctrl} to be 2.0 V by a bandgap voltage reference every time before the clock generation is executed.

It is noted that the DEMUX at the output of the odd-numbered stages is a dummy DEMUX. Its function is nothing but to equalize the load of each delay cell. Hence, the control lines of these dummy DEMUXs are all grounded. That is, they are all connected to an external signal, S_{GND}.

Positive edge collector : Its major operation is to detect the rising edges of the generated clocks and then produce corresponding low pulse trains. A PEC cell is shown in Fig. 3 which consists of two DFFs and one MUX. For the sake of clarity, Fig. 4 shows a 4-stage tap line. On the top of Fig. 4 is the waveforms of the generated clocks at the respective output node of each stage. Assume the (0,0,0,0) is the initial state of Q_1, Q_2, Q_3, Q_4. Table 1 is the truth table of Q_1, Q_2, Q_3, Q_4, and the resulted low pulse trains, $PULSE_2$ and $PULSE_4$. Notably, the function of the PEC cell is independent of the initial conditions of the DFFs. The best advantage of such a design is that it is noise immune, since they are all digital circuits.

Clock generator : Low pulse trains can not be used as an ideal clock source apparently and directly. A pseudo-N logic is utilized to realize such a generator as shown in Fig. 5. $S2[i]$ is the ith control line to determine whether the ith clock generator is enabled or not. If $i = 1$, then $S2[i]$ is low, and accordingly MN3 is on which grounds the gate of MN4 to disable the corresponding ith cell. By contrast, if $S2[i]$ is high, MN3 is off and the low pulse train $PULSE_{2\text{-}i}$ is propagated to the gate of MN4. Then, f_{out} is generated.

In short, all of the circuits except the current mirror at the leftmost section of the VCDTL are digital and programmable. It will outperform the prior works regarding the noise immunity, and sensitivity to power drifting and temperature variations.

3. SIMULATIONS & IMPLEMENTATION

In order to verify the correctness and performance of our proposed design, we adopt TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 μm 1P5M CMOS process to implement the entire circuits. Note that several well known and proven circuits besides those circuits in Section 2 are also carried out, including a high-speed and low-power PFD and charge pump by Lee's [3], and a glitch-free single-phase dual-O/P DFF by Huang's [2].

Fig. 6 shows the scenario that the V_{ctrl} changes when the programmable numerical inputs increase from 8× to 10× given a 150 MHz reference clock. The corresponding output waveforms are shown in the bottom of the Fig. 6. The lock time is 0.6 μs. Fig. 7 shows the working range of the output frequency vs. V_{ctrl}. Fig. 8 is the spectrum of f_{out} given that the numerical input is 10× as well as a 120 MHz reference clock. The overall characteristics of the post-layout simulation of the proposed design is summarized in Table 2.

The proposed design is carried out on silicon. The top of Fig. 9 is the die photo of the design. The HP4433B Signal Generator is used to feed the chip with f_{ref} which is ranged from 100 MHz to 150 MHz. Spectrum analyzers used for physical measurements are HP8563E and HP8594E. Fig. 10 shows the SSB (single sideband) phase noise occurring at f_{out} = 120 MHz × 10 = 1.2 GHz. By contrast, Fig. 10 shows the spurious tones occurring at the same output. The overall characteristics of the physical chip measurements is shown in Table 3.

4. CONCLUSION

This paper presents a programmable LO design approach using DLL-based frequency multiplier. Besides a current mirror, the rest of the design is purely digital logic which in turn eliminates the noise prone problem. No large inductors are required to balance the output impedance. The power consumption is pretty low compared to the prior works. The lock time is also drastically shorten, since the start-up voltage has been biased to the middle of the operating range.

5. REFERENCES

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charge pump," *Design Automation Conference - Asia and South Pacific (ASP-DAC'99)*, vol. 1, pp. 269-272, Jan. 1999.

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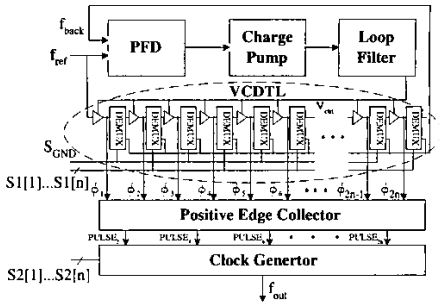

Figure 1: proposed programmable frequency multiplier

clocks	Q_1	Q_2	Q_3	Q_4	$PULSE_2$	$PULSE_4$
ϕ_1	1	0	0	0	0	1
ϕ_2	1	1	0	0	1	1
ϕ_3	1	1	1	0	1	0
ϕ_4	1	1	1	1	1	1
ϕ_1	0	1	1	1	0	1
ϕ_2	0	0	1	1	1	1
ϕ_3	0	0	0	1	1	0
ϕ_4	0	0	0	0	1	1

Table 1: Truth table of the 2-stage tap line.

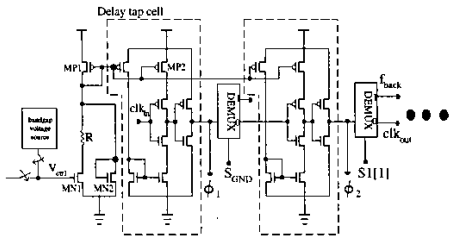

Figure 2: the leftmost part of VCDTL

VDD	2.5 V $\pm$ 5%
Temperature	$-15°$C - 55°C
Technology	0.25 μm CMOS
Max. O/P freq	1.5 GHz
Programmable factor	7 $\times \sim$ 10$\times$
Spurious tones (dBc)	-29.0 dBc (60 MHz o/s)
(120 MHz $\times$ 10 = 1.2 GHz)	-21.4 dBc (120 MHz o/s)
Average power (1.5 GHz)	26.1 mW
Worst lock time	1.0 μs
Chip area	1061$\times$125 μm^2
Transistor count	777 (w/o loop filter)

Table 2: Characteristics of post-layout simulation.

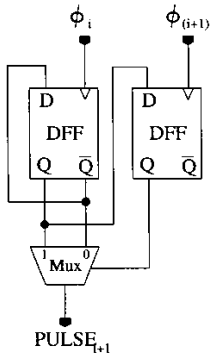

Figure 3: PEC cell

VDD	2.5 V
Ref. clock	120 MHz
Multiply factor	10 $\times$
Output level	-17 dBm
Phase noise	-93.5 dBc/Hz @ 10 KHz
	-103.4 dBc/Hz @ 50 KHz
Spurious tones	-18.0 dBc @ 60 MHz o/s
	-20.0 dBc @ 120 MHz o/s
Average power @ 1.2 GHz	52.2 mW

Table 3: The measurement summary of the proposed design at 1.2 GHz output.

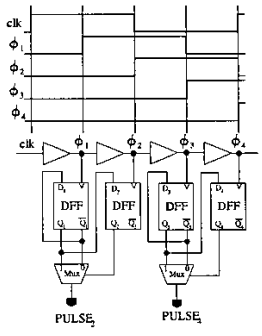

Figure 4: an example of a 4-stage tap line

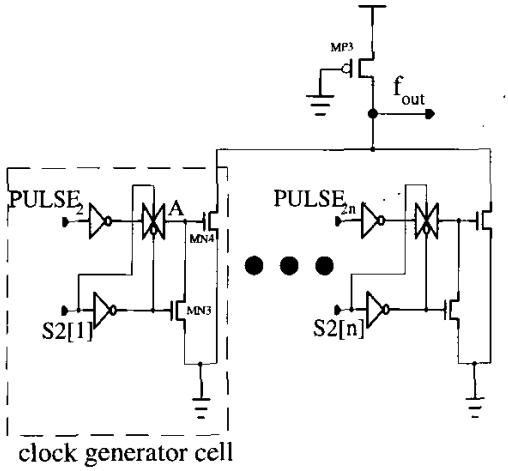

Figure 5: clock generator

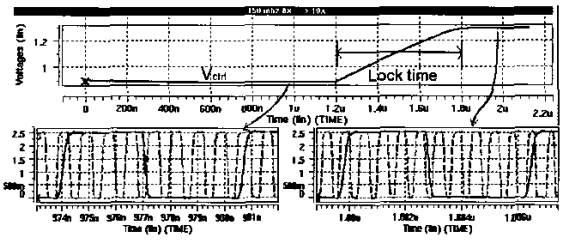

Figure 6: simulation waveforms given from 8× to 10×

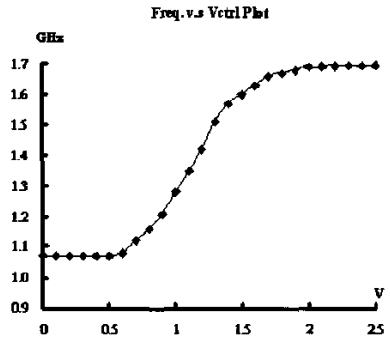

Figure 7: working range of V_{ctrl} vs. freq

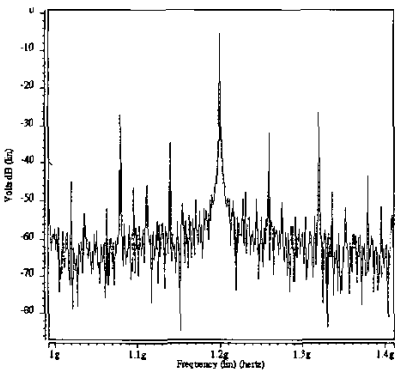

Figure 8: frequency spectrum of f_{out} at 10×

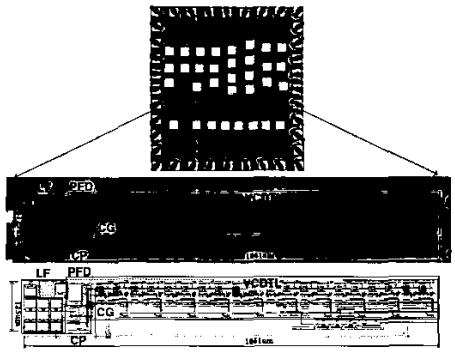

Figure 9: die photo of the proposed design and the layout

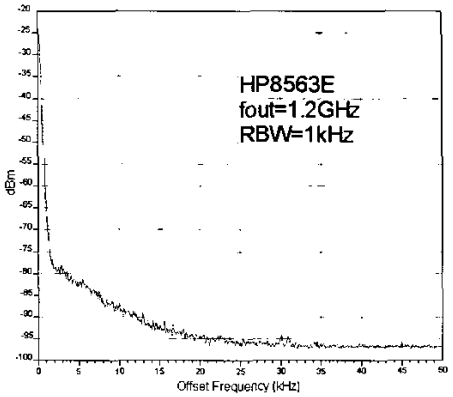

Figure 10: SSB (signle sideband) phase noise at f_{out} = 1.2 GHz

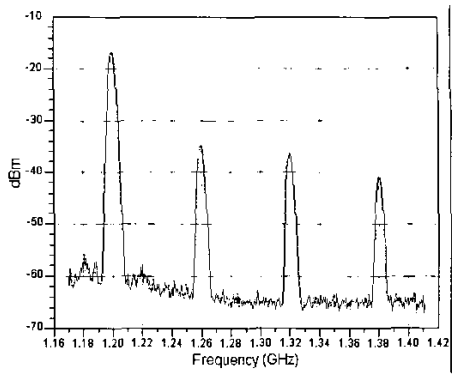

Figure 11: spurious tones performance at f_{out} = 1.2 GH = 120 MHz input × 10