

AN IMPLANTABLE NEURAL INTERFACE MICRO-STIMULATOR CHIP WITH EXTERNAL CONTROLLABILITY[§]

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ABSTRACT

Various implantable micro-stimulators have been proposed for clinical applications in recent years. A small and flexible implanted device is the key component to any field application. This multi-parameter implantable SOC (system-on-chip) chip design is aimed at neural interface stimulation, which includes controllable stimulators, and telemetry for data and power transmission. The micro-stimulator consists of 2-channel addressable current-source stimulators with seven parameters can be controlled by the external device. The external transmitter employs the RS232 format as the data transmission protocol and utilizes the NRZ code to transmit instructions and data to the implanted SOC chip. The entire SOC circuit is implemented on silicon by 0.35 μm CMOS 2P4M technology.

1. INTRODUCTION

Traditional medical treatments have been drastically influenced by the advance of modern sciences and technologies. One of the astonishing medicare tools is the implantable micro-electrical stimulators thanks to the deeply miniaturized silicon technology. The implantable micro-electrical stimulators as well as the entire system are widely used in the treatment of the bladder leakage control [1], interrupt of pains, shaking syndromes of Parkinson's disease, muscle nerve stimulation [3], and Cochlear implants [2]. The frequency, current, and waveform of each application are different. The SOC chip is focused on controlling flexible stimulators for different treatments.

There are two major types for the implantable device design. The first type is to employ microcontrollers [4]. It has a better flexibility to change different functions by programming, but the size is extremely large. The second type is based on deep submicron silicon semiconductor technology, which must follow certain design requirements to fabrication. The chip size, by contrast, is very small, which might be only 1~3 mm² and very suitable for implantable micro-stimulators [6, 7]. The critical drawback of this kind of chips is lack of flexibility. We, thus, propose to increase the parameters encapsulated in transmitted packets to resolve this

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problem. There are a total of seven parameters in the protocol that we propose in this paper, including address, polarity, magnitude, continuity, duration, interval, and waveform. They are all controllable from an external device to serve most of the currently required medical stimulations.

2. MULTI-PARAMETER NEURAL INTERFACE MICRO-STIMULATOR SYSTEM

The infrastructure of the entire micro-stimulator system is given in Fig. 1. Due to the small receiver coil of the implanted device, the power transmission efficiency in many of these micro-devices is rather low. In order to supply enough power to the implanted device, a high efficiency transmitter/amplifier must be used. Class-E power amplifiers show efficiency above 90%, which is considered suitable for this low coupling application. Self-oscillating power amplification is carried out by a Class-E amplifier.

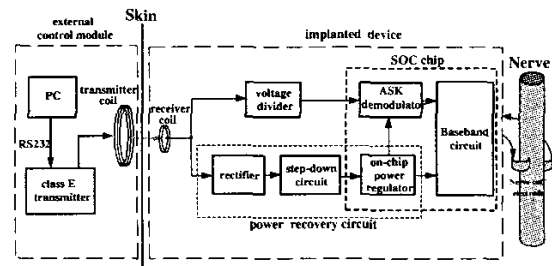


Fig. 1. Wireless neural stimulating system

The selection of the RF carrier frequency should consider the trade-off between the transmission bit rate and the tissue absorption. The carrier frequency at 2 MHz [10] allows an adequate transmission rate and minimal tissue absorption.

The transmitted RF electromagnetic wave is picked up by receiver coil of the implanted device, and the electromagnetic energy is transferred into a regulator serving for the implanted chip. Meanwhile, the transmitted data modulated in RF signal is demodulated and decoded to determine stimulation patterns and channel selections. The internal transceiver needs a stable system clock for the digital circuit. The system clock can be extracted from the 2 MHz RF carrier by the synchronization of a built-in clock. According to

the received data, micro-stimulators generate constant currents as well as monophasic or biphasic stimulation waves for the selected nerve stimulation functions.

The external control module is composed a PC, a Class-E amplifier and a transmitter coil. Amplitude shift keying (ASK) modulation is employed to transfer the external command data and power to the internal chip by the Class-E amplifier. Fig. 2 is circuit design of Class-E. It uses the serial-parallel LC resonant circuit and switching behavior to induce the high resonant AC voltage and current through transmitter coil. The circuit is operated between series and parallel resonant networks via switching (IRL510). Resonant networks consist of capacitor C_1 , C_2 , and transmitter coil L_2 . There are two different resonant frequencies provided by the Class-E amplifier: when the switch (IRL510) is on, the resonant frequency is determined by C_2 and L_2 ; if it is off, the resonant frequency depends on C_1 , C_2 , and L_2 in series.

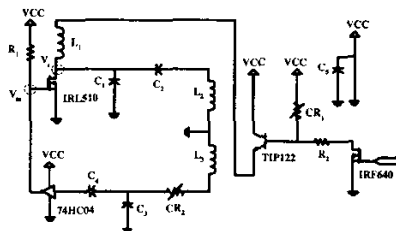


Fig. 2. Schematic diagram of the Class-E amplifier

3. SOC DESIGN OF A MULTI-PARAMETER NEURAL INTERFACE MICRO-STIMULATOR

We propose an SOC (system-on-chip) chip to carry out the controllable micro-stimulation mission utilizing wireless and non-penetrating transmission to accept external instructions and execute required stimulations.

3.1. System design

3.1.1. Power, Regulator and ASK demodulator

As we mentioned in previous sections, a high efficiency Class-E amplifier is used to transmit power to the implanted device. The power of the core circuit is on the chip generated by the induced RF signal. The voltage swing of the induced signal is as high as ± 24 V. Therefore, the signal must be rectified and regulated before it is delivered to the chip. On-chip power regulators are required to supply stable VDD output voltages to the internal digital core by regulating the power transmitted generated by on-chip coupling coils. There are a total of 4 regulators in this SOC chip, including 1 for I/O PADs, 1 for ASK demodulator, and 2 for the baseband module and stimulator circuits. The data flow of C-less (capacitor-less) ASK demodulator is shown in Fig. 3.

3.1.2. Packet Format

The control data are provided by the PC in the external control module. The data packet format follows the RS232 standard for the consideration of a limited bandwidth. The valid packets in the system protocol are listed in Table 1, including synchronization,

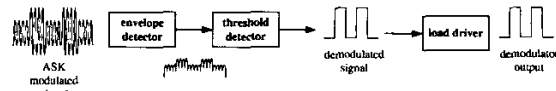


Fig. 3. The data flow of ASK demodulator

start, data, and end packets. This protocol also contains the error detection capability.

Table 1. The system protocol

packet1	0	1	0	1	0	1	0	1	0	1
packet2	0	1	0	1	0	1	0	1	0	1
START	0	1	0	1	0	1	0	0	1	1
DATA1.1	0	AD		P	MAG					1
DATA1.2	0	CONT	DUR	INTV		WAVE	PAR	1		
...	...									
END	0	0	0	0	0	0	0	0	0	0

- 1). synchronization: The packets 1~2 are used to synchronize the external and internal clocks.
- 2). START: The packet 3 is a start packet, which triggers the stimulating function.
- 3). data packets (DATA1.1~DATA1.2...): All of the stimulation control parameters are encoded in these packets.

DATA1.1: The first bit is the RS232 start bit. The 2nd~3rd bits (AD) are the address bits selecting which one or both of the two channels are enabled and excited. The 4th bit (P field) determines the polarity (positive or negative) of the output stimulating current. The magnitude field is composed of 5 bits (MAG) which denoted the magnitude of the stimulating current. These 5 bits will be fed to the DAC (digital to analog converter) associated with each channel. The last "1" bit is the end bit.

DATA1.2: The first bit is the RS232 start bit. The 2nd bit (CONT field) is the continuous mode selection. The micro-stimulator keeps stimulation pattern the same as that given by the command in the continuous mode. Hence, the external device only needs to transfer the power without the necessity of encoding data. The 3rd~4th bits (DUR field) are the stimulation pulse duration. The detailed specification is tabulated in Table 2. The pulse interval is determined by the of 3 bits in the INTV field to select the pulse frequency as shown in Table 3. The 8th bit (WAVE field) selects the stimulation waveform to be monophasic or biphasic. The 9th bit is the parity check bit (PAR field) of all data packets to avoid any erroneous stimulation. The recieved data are ignored when its validity is not confirmed. The last "1" is the end bit.

Notably, the received data packets will be kept without repeating the transmission of the same packets for a constant stimulation. Eqn. (1) and (2) are the frequency equations of monophasic and biphasic waveforms, respectively.

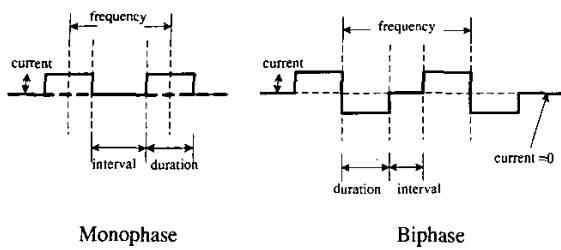


Fig. 4. The definition of duration and interval

$$Freq_{monophase} = \frac{1}{duration + interval} \quad (1)$$

$$Freq_{biphase} = \frac{1}{2 \cdot duration + interval} \quad (2)$$

where the definitions of "duration" and "interval" are, respectively, shown in Fig 4.

Table 2. The specification of stimulation duration time

DUR field	00	01	10	11
real duration	100 μs	500 μs	1 ms	2 ms

Table 3. The specification of stimulation interval time

INTV	000	001	010	011	100	101	110	111
interval (ms)	0	0.1	0.2	1	3	5	10	50
freq. (Hz)	10 k	5 k	3.3 k	1 k	330	200	100	20

The proposed chip is focused on the most popular stimulation applications like denervated muscle, pain relief, bladder stimulated, nerve blocking, muscle stimulation. Users are able to choose the type of output by combined the duration, interval, and waveform setup.

4). END: The END packet means this stimulation is finished.

3.1.3. Baseband schematic design

Referring to Fig. 5, the internal architecture of the implantable SOC chip is revealed. OSC is a ring-based 5 MHz clock generator, while the "built-in reset" initialization of the system is also included in the same mixed-signal module.

3.1.4. data and clock recovery

When the synchronization packets are received, the number of the external clock is sampled and recovered by the internal OSC. The recovered clock is send to other modules. The NRZ bit stream generated by the ASK demodulator (not shown) is in charge of recovering the bits for the RS232 format. The data recovery is also carried out in this module.

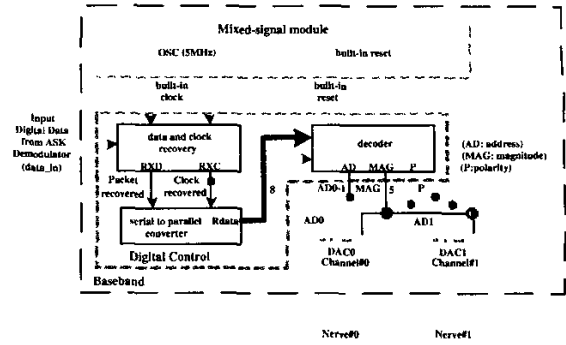


Fig. 5. Baseband architecture of the implantable device)

3.1.5. serial to parallel converter

The recovered packet is converted into a parallel format to decode the control command by the serial to parallel converter.

3.1.6. decoder

The decoder determines the valid commands and controls the stimulating channels which contain one DAC (digital-to-analog converter) each. The polarity and magnitude will be determined in this part, too. The stimulation pulse width as well as the frequency is adjusted by the DUV and INTV field of data packets. The output waveform is selected by P and WAVE fields. As soon as the END packet is received, the stimulation stops.

3.1.7. DAC

The DACs directly supply driving currents to their associative nerves to serve as a stimulus. The magnitude of the current is determined by the MAG field of the data packets which denoted by M4, M3, M2, M1, M0 in Fig. 6. The aspect ratio (W/L) for MOSs (in the Fig. 6) gated by M4, M3, M2, M1, M0 is 16:8:4:2:1, which produces a binary-weighted stimulating current, respectively. That is, the overall final stimulating current is of the summation of the currents via the mentioned MOSs.

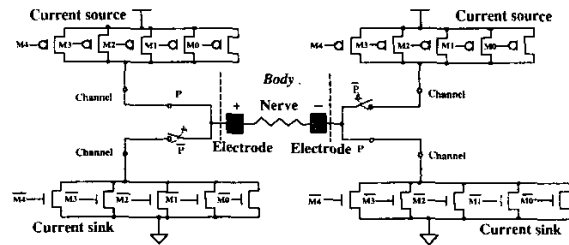


Fig. 6. Interface of DAC and the nerve

4. SIMULATION AND IMPLEMENTATION

The chip is designed using TSMC 0.35 μm 2P4M CMOS process. The layout is shown in Fig. 7. Fig. 8 is the post-layout simulation

of the proposed SOC chip. The channel 2 is selected to generate the maximal magnitude (1.8 mA at 1K ohm load) stimulating current given the testing condition of TT model, 37°C, and VDD = 3.3 V. The comparison of the proposed design with several prior works is summarized in Table 4. Our design possesses the edge regarding parameter numbers, chip size, and core power consumption.

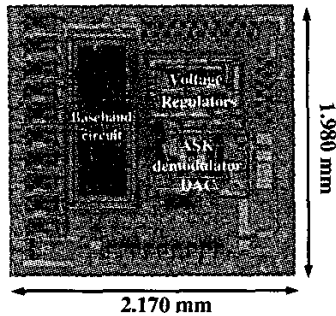


Fig. 7. Layout of the proposed design

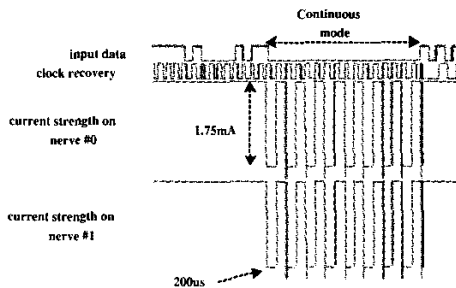


Fig. 8. Nanosim post-layout simulation result of the proposed SOC chip

5. CONCLUSION

An SOC-based solution for implantable neural interfacing design is present. The small-area solutions for an ASK demodulator and a stable 3.3 V on-chip voltage regulator design are also present in this work. The feature of the chip is that we are trying to support the same flexibility of traditional electrical stimulators in the implantable device and minimize the size at the same time. It can support several parameters for different usages in the neural electrical stimulation applications.

6. REFERENCES

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Table 4. Comparison with prior works

	[5]	[6]	[7]	ours
Technology	CMOS 1.2 μ m	Bi-CMOS 3 μ m	Bi-CMOS 3 μ m	CMOS 0.35 μ m
size (mm ²)	16 \times 2	1.36 \times 7.5	2.0 \times 8.7	2.17 \times 1.98
Channel #	4 (bipolar)	1	8	2 (bipolar)
Parameter #	5	2	5	7
Regulated voltage (V)	N/A	4.5 and 9	4	3.3
Carrier Freq. (Hz)	AM (20M)	AM(2M)	ASK(4M)	ASK(2M)
Data rate (bps)	300K	N/A	8.3K	10K
Stim. freq. (Hz)	2~1500	1~40	\leq 170	20~10K
Duration (μ s)	10~2550	10~200	4~2025	100~2000
Output (mA)	0~6.3	10	0~2	0~1.8
Power (mW)	N/A	45~55	15	80 (average), 120 (max.)

†: the power consumption of the 4 regulators and demodulator are 50mW,

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