

A CMOS IF-BAND MIXED-SIGNAL CONVERTER DESIGN FOR DVB-T RECEIVERS[§]

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ABSTRACT

This paper describes a CMOS IF-band converter (IFC) which is applied in the analog front end (AFE) circuitry of DVB-T receivers. The proposed IFC is composed of a down-conversion mixer, an automatic gain controller (AGC), and an anti-aliasing filter (AAF). The down-conversion mixer uses a current folded-mirror technique which converts a 36 MHz intermediate frequency (IF) input into a 4.5 MHz baseband signal. A temperature-compensated 6th order transconductance-C (Gm-C) filter with digitally tunable bandwidth (6, 7, 8 MHz) is used to constitute the proposed anti-aliasing filter (AAF). SpectreRF simulations reveal that the conversion gain of the down-conversion mixer is -2.54 dB. The accuracy of the AAF bandwidth is better than 3.28 %. 1-dB compression point and IIP3 of the proposed IFC are -7.668 dBm and -5.435 dBm, respectively.

Keywords : mixer, frequency converter, conversion gain, DVB-T, DBM

1. INTRODUCTION

The function of a DVB-T (terrestrial digital video broadcasting) receiver AFE is to convert an input signal from the RF tuner into a bit stream for following OFDM demodulation processing. The AFE consists of a radio frequency (RF) tuner, a down-conversion mixer, an AGC, an AAF, and an analog to digital converter (ADC), as shown in Fig. 1. The RF tuner selects a desired channel and converts the received signal into a 36 MHz IF signal. The down-conversion mixer then converts the 36 MHz IF signal into a 4.5 MHz baseband signal. The AGC block is used to ensure that the amplitude of the received signal is kept in a constant level

which is large enough for the following circuitry. The AAF is used to remove the adjacent-channel coupled noise generated by the mixer to avoid inter-channel interferences and then passes the desired signal to the ADC [1]. Since a wideband AGC design has been proposed in [4], this paper will be focused on the down-conversion mixer and the AAF which are enclosed by the dotted lines in Fig. 1.

2. DOWN-CONVERSION MIXER AND AAF DESIGN

2.1. Down-Conversion Mixer

Fig. 2 shows a current folded-mirror mixer which is a DBM structure and is used to implement the desired DVB-T down-conversion mixer. M1 and M2 convert the IF voltage into a current signal. M3 - M6, and two R_{E2} resistors consist of two current mirrors to bias M7 - M10. The mixer attains the mixed waves by a LO signal with a large amplitude to drive M7 - M10 such that the IF currents in M4 and M6 can be changed. According to [3], The conversion gain G_c of the DBM is as follows,

$$\begin{aligned} G_c &= \frac{V_{out}}{V_{IF}} \\ &= \frac{2}{\pi} \times \frac{m \cdot gm_{3,5} gm_{4,6} Rc^2}{1 + gm_{3,5} R_{E2}} \frac{2Z_T}{1 + 2R_s gm_{1,2}} \\ &= \frac{2}{\pi} \times gm_c Z_T, \end{aligned} \quad (1)$$

where $m = \frac{i_{d3,5}}{i_{d4,6}}$, $gm_1 - gm_6$ are the transconductances of M1 - M6, respectively, Z_T is the parallel equivalent impedance of R_T , L_T , and C_T . An RLC parallel resonant tank [2] is used as the mixer's load to select the desired bandwidth. The tuned load can provide a large output swing and a fixed gain, i.e., $gm_c Z_T$, at the resonant frequency. The mixer employs external

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LC elements to compose the resonant tank due to large area cost and poor performance if they are realized on silicon. Besides, a source degeneration resistor R_s is inserted between the sources of M1 and M2 in Fig. 2 to increase the mixer's linearity, i.e., P_{1dB} and IIP3. Notably, a large R_s can improve the linearity with the loss of the gain of the mixer.

2.2. Gm-C AAF Design

1) *AAF*: A 6th order Gm-C AAF is proposed in Fig. 3 which is a 6th order passive LC ladder filter [6]. In order to carry out the feasibility, the passive inductors are replaced with active inductors, while the resistors are replaced with active Gm elements.

Referring to Fig. 4, which is the architecture of Nauta's transconductor [5]. Assume that all inverters in Fig. 4 are identical. The V-I transfer function of the transconductor is as follows.

$$\begin{aligned} I_{od} &= I_{o1} - I_{o2} \\ &= V_{id} \cdot (V_{DD} - V_{thn} + V_{thp}) \cdot \sqrt{\beta_n \cdot \beta_p} \\ &= V_{id} \cdot gm_N, \end{aligned} \quad (2)$$

where V_{id} is the differential input voltage, V_{thn} and V_{thp} are the threshold voltages of NMOS and PMOS transistors, respectively, β_n and β_p are the transconductance parameters of NMOS and PMOS transistors, respectively, and gm_N is the equivalent transconductance of Nauta's transconductor. The transconductor can be denoted as a single element.

Passive inductors usually occupy large area on chip, which is not acceptable in SOC designs. Hence, we utilize the symmetrical floating gyrator in Fig. 5 instead, which is equivalent to an inductor [7]. The equivalent inductance, thus, is derived as follows.

$$L_{eq} = \frac{V}{I} = \frac{C_L}{gm_N^2}, \quad (3)$$

The resistor can also be replaced with the symmetric transconductor in Fig 4. Fig. 6 shows the equivalent circuit of the resistor.

$$R_{eq} = \frac{V}{I} = \frac{V}{gm_N \cdot V} = \frac{1}{gm_N} \quad (4)$$

The DVB-T specifications [1] require three different baseband bandwidths: 6, 7, and 8 MHz. Therefore, the cut-off frequencies thereof are set to 7.5, 8.0, and 8.5 MHz, respectively. In order to meet the requirements, the digital controlled switches, SW_6M, SW_7M, SW_8M in Fig. 2, are used in the AAF circuit such that the bandwidth of the output signal can be selected. Notably, SW_RC is added to select an external RC filter for the purpose of testing.

2) *High PSRR regulator*: The Gm-C filter needs a stable bias to resist the variations of power supply voltage and temperature. A high PSRR (power supply rejection ratio) regulator which provides a stable voltage to all of the AAF sub-circuits. Besides, a voltage divider composed of resistors supplies 1.5 V voltage to the AGC as the common mode voltage such that the following ADC can attain maximum input signal swing. The post-layout simulations prove that when the power supply voltage varies within $\pm 15\%$, the output voltage drift of the regulator is less than $\pm 4\%$.

3) *Temperature-compensated circuit*: The gm_N of the Nauta's symmetric transconductor varies with the temperature drifting, because there is no protection or compensation devices in the circuit. Consequently, the filtering bandwidth will be drifting, and unwanted noise might appear. Hence, a modified Nauta's symmetric transconductor structure as shown in Fig. 7 is employed. The NMOS transistors (M131 - M136), namely foot switches, are inserted between the GND and the pull-down NMOS in each inverter as a tail current control mechanism. If V_{bias} provides a stable voltage to fix the bias current, the gm_N will be kept at a constant to reduce the variation of the filtering bandwidth.

3. SIMULATION AND IMPLEMENTATION

In order to verify the performance of the proposed IFC, TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed design. Fig. 8 shows the layout of the proposed IFC.

3.1. Down-Conversion Mixer

The operating condition of the down-conversion mixer is summarized in Table 1. Fig. 9 shows the simulations of the conversion gain, where A is a -34.0119 dBm, 36 MHz signal, B is the mixer's output signal. Hence, the conversion gain is -2.54 dBm. The design characteristics of the down-conversion mixer are tabulated in Table 2.

3.2. AAF

Fig. 10(a) shows the post-layout simulations of the frequency response given 6 MHz baseband bandwidth at TT model, $V_{DD} = 3.3$ V, 25°C . Given the 6 MHz baseband bandwidth with a 7.5 MHz cut-off frequency, all of the PVT corner simulation results are revealed in Fig. 10(b). The accuracy of the cut-off bandwidth is 3.28% in the worst case.

3.3. Integrated Simulation

Finally, the down-conversion mixer, the AGC (gain = 0 dB), and the AAF are integrated to carry out a full-scale simulation due to that the AGC and the AAF might deteriorate the mixer's linearity. The P_{1dB} and IIP3 plots are shown in Fig. 11(a) and (b), respectively, to justify the decibel linearity of the proposed design. The characteristics of the proposed mixed-signal converter are summarized in Table 3.

4. CONCLUSION

We have proposed a CMOS IF band mixed-signal converter for DVB-T receivers. The proposed converter converts a 36 MHz IF input into a 4.5 MHz baseband signal. The down-conversion mixer adopts the current folded-mirror architecture to provide a superior performance in conversion gain and linearity. The AAF employs the modified Nauta's symmetric transconductor to suppress the gm and filtering channel bandwidth variations because of temperature drifting.

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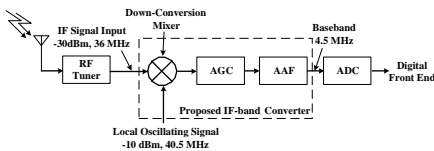


Figure 1: DVB-T receiver analog front end

Table 1: Summary of the mixer's operating condition

Input Condition	Values
VDD	3.3 V
RF Frequency	36 MHz
RF Power	-30 dBm
LO Frequency	40.5 MHz
LO Power	-10 dBm

Table 2: Characteristics of the down-conversion mixer

Conversion Gain	-2.54 dBm
P_{1dB}	0.236 dBm
IIP3	2.16 dBm
Noise Figure	29.5 dB
Power Consumption	9.217 mW

Table 3: Characteristics of the proposed mixed-signal converter

P_{1dB}	-7.668 dBm
IIP3	-5.435 dBm
Power Consumption (Down-Conversion Mixer+AGC+AAF)	75.5 mW

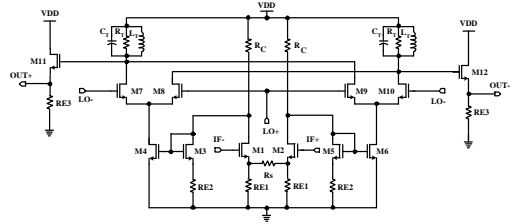


Figure 2: Current folded-mirror mixer circuitry

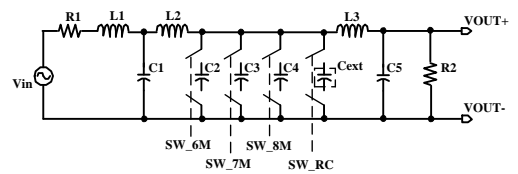


Figure 3: 6th order passive LC ladder filter

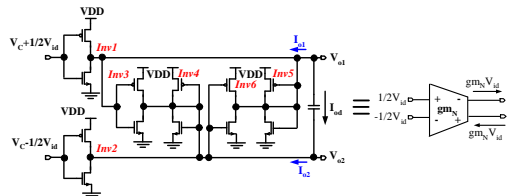


Figure 4: Nauta's symmetric transconductor

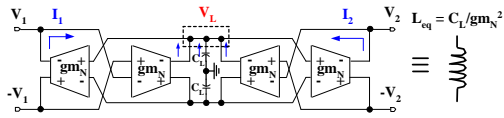


Figure 5: Symmetrical floating gyrator which is equivalent to an inductor

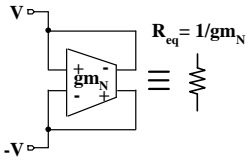


Figure 6: Equivalent circuit of the resistor

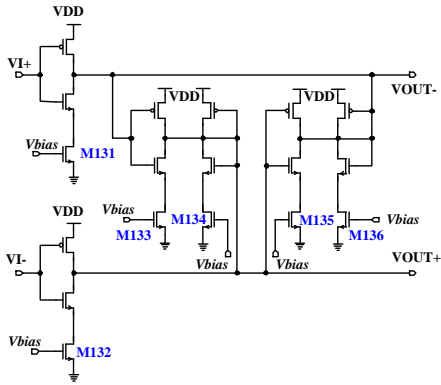


Figure 7: Modified Nauta's symmetric transconductor

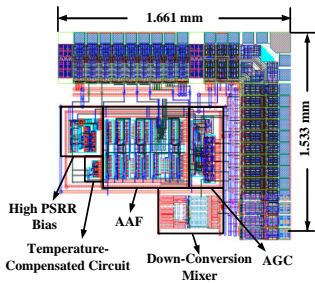


Figure 8: Layout of the proposed mixer-signal converter

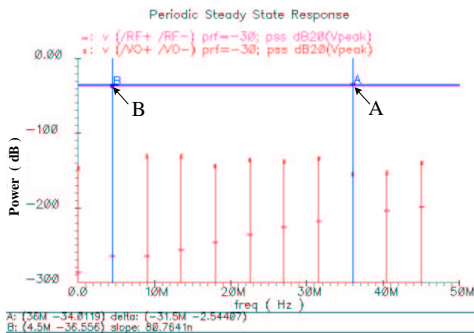


Figure 9: Conversion gain

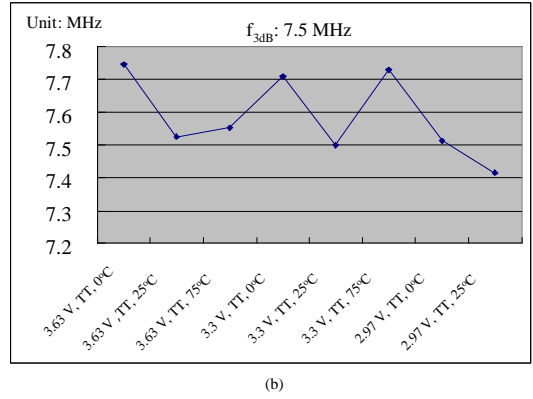
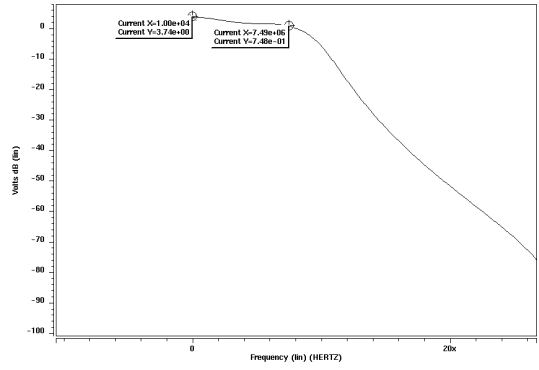


Figure 10: Post-layout simulation of 6 MHz baseband bandwidth

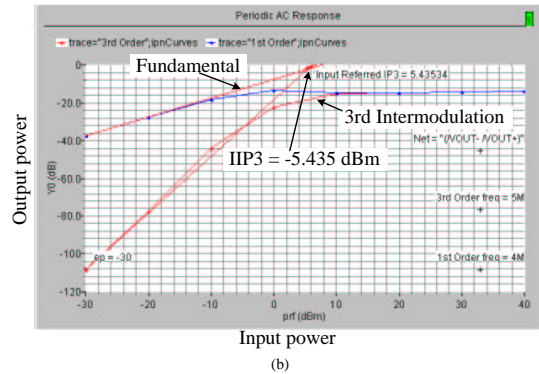
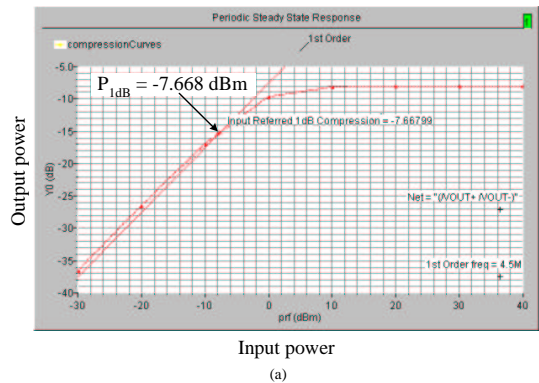


Figure 11: P_{1dB} and IIP3 plot