A LOW POWER HIGH-SPEED 8-BIT PIPELINING CLA DESIGN USING DUAL THRESHOLD VOLTAGE DOMINO LOGIC[§]

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ABSTRACT

A high speed and low power 8-bit carry-lookahead adder (CLA) using two-phase modified dual threshold voltage (dual-V_t) domino logic blocks which are arranged in a PLA-like design style with pipelining is present. The modified domino logic circuits employ dual-V_t transistors for reducing subthreshold leakage current when advanced deep submicron process is used. Moreover, an NMOS transistor is inserted in the discharging path of the output inverter such that the modified domino logic can be properly applied in the pipeline structure to reduce the power consumption. The addition of two 8-bit binary numbers is executed in 2 cycles. Not only is it proved to be also suitable for long adders, the dynamic power consumption is also drastically reduced by more than 10% at the worst-case process corner.

Keywords : CLA, domino logic, dual threshold voltage CMOS, pipeline, PLA-like

1. INTRODUCTION

Fast adders are key elements in digital circuits, including multipliers, and DSP chips. Many efforts have been focused on the improvement of adder designs [4] - [7]. CMOS dynamic logic has been recognized as one of the promising options to challenge the GHz operations for the adder design, [1]. Other logics suffer from different difficulties which were addressed in [5]. However, the major trade-off of these prior GHz logic circuits is the high power consumption which is not a tolerable price to pay in recent mobile technologies. These circuits unavoidably consume power even if they are in a standby condition. A dual-V_t circuit technique was proposd in [2] for reducing standby power dissipation while still maintaining high performance in domino logic. [3], then, employed sleep switches and dual-V_t CMOS technology to place an idle domino logic circuit into a low leakage state. In this paper, we propose a low power PLA-like structure using modified dual-V_t domino logic blocks. An 8-bit CLA using the dual-V_t domino logic blocks which are arranged in a PLA-like manner and synchronously triggered is implemented to verify the power reduction as well as the preservation of high speed. The major advantage of the low power design methodology is that it is robust regardless of long data words, e.g., 64-bit binary data. The power reduction is found to be more than 10% compared to the prior works by simulations.

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2. LOW POWER HIGH-SPEED 8-BIT CLA

2.1. Typical dual-V_t domino logic circuits

Employing dual-V_t transistors for reducing subthreshold leakage current in domino logic circuits was proposed by [2]. We, then, utilized such a dual-V_t scheme to propose a typical dual-V_t domino logic circuit in Fig. 1. The high-V_t transistors are reprensented in Fig. 1 by a thick line in the channel region. The domino logic circuits operation is divided into two phases: precharge phase and evaluation phase.

1). During the precharge phase, clock = 0, P1 is on and N1 is off. Then, node A is precharged to V_{DD} and the output is initialized to be low.

2). During the evaluation phase, clock = 1, P1 is off and N1 is on. If the low-V_t evaluation block is evaluated to be "pass", the charge at node A should be ground through the low-V_t evaluation block and N1. The output then is a logic high. If the low-V_t evaluation block is evaluated to be "stop", there will be no discharging path for node

A. A "keeper" PMOS is added to help keep node A at V_{DD}. The output then is a logic low.

Summarized in the above, the output will be high when the low-V_t evaluation block is evaluated "pass", i.e., "1", during clock = 1. On the contrary, the output will be low when the low-V_t evaluation block is evaluated "stop", i.e., "0", during clock = 1.

The critical signal transitions that determine the delay of the domino logic ciruits occur along the evaluation path. Hence, in the dual-V_t domino logic circuits, high-V_t transistors are employed on the non-critical precharge paths. Alternatively, low-V_t transistors are employed on the speed critical evaluation paths [2]. As a result, the subthreshold leakage current of the dual-V_t domino logic circuits is smaller as compared to the low-V_t domino logic circuits while still maintaining high performance.

2.2. Modified dual-V_t domino logic circuits

However, there is a problem with such a typical dual-V_t domino logic. That is, the output of the typical dual-V_t domino logic circuit can not hold the logic state during the precharge phase in the next cycle. Therefore, it can not be directly applied in any pipeline structure. Hence, a modified dual-V_t domino logic circuit as shown in Fig. 2 is proposed to resolve such a difficulty. An NMOS transistor is inserted in the discharging path of the output inverter. The operation of the modified dual-V_t domino logic circuit is similar to that of the typical dual-V_t domino logic circuit apart from the precharge phase. During the precharge phase, clock = 0, P1 is on, N1 and N3 are all off. Thus, P2 is switched off. The output has neither charging path nor discharging path such that the state will be kept as the previous state. This means that the circuit will consume less power.

2.3. PLA-styled 8-bit CLA design

The formulation of a 8-bit CLA is represented by the following equations:

$$\begin{aligned} S_i &= C_{i-1} \bigoplus P_i \\ C_i &= G_{i-1} + P_{i-1}G_{i-2} + P_{i-1}P_{i-2}G_{i-3} + \\ &\quad \ldots + P_{i-1}P_{i-2}\ldots P_1P_0C_0 \end{aligned} \quad (1)$$

where $A_i, B_i, i = 0...7$, are inputs, and P_i, G_i are *propagate* and *generate* signals, respectively, $P_i = A_i \bigoplus B_i$, $G_i = A_i \cdot B_i$.

If the P_i's and G_i's are produced by combinatorial logic function blocks before they are fed into the function blocks for S_i's and C_i's, then Eqn. (1) implies that a two-level AND-OR logic function block is a possible solution to achieve high speed operations. Thus, the PLA-styled design is suitable for such a function block. A conceptual PLA-styled design for CLA is shown in Fig. 3. A typical PLA consists of an AND array and an OR array. It is well known that the series NMOS in the evaluation block of NAND or AND gates will produce long discharging delays which subsequently slow down the entire circuit. We can take advantage of the non-inverting feature of the domino logic to utilize a NOT-OR-NOT-OR configuration instead of the typical AND-OR style, where the two OR planes are made of the modified dual-V_t domino logic circuits. Meanwhile, it can also minimize the series transistor count in the low-V_t evaluation block. The OR array is made of the modified dual-V_t domino logic with a predefined low-V_t evaluation block. The inputs to the first OR array is the inverted P_i's (propagate) and G_i's (generate) signals which are also produced by other modified dual-V_t domino logic units as shown in Fig. 4. Notably, we define the propagate signals in a different way from the traditional $P_i = A_i + B_i$, because the $P_i = A_i \bigoplus B_i$ can be reused to generate the sum term, i.e., S_i.

2.4. Speed and area analysis

Speed : The critical path of an adder resides on the generation of carry signals, i.e., C_8 in the 8-bit adder. After the binary data are ready, the generation of P_i's and G_i's by using the modified dual-V_t domino logic takes the high half of a full cycle. That is, the results of GP blocks will be ready when the clock is low. The inverted P_i's and G_i's will then be fed into the first OR plane of the the modified dual-V_t domino-based PLA. The inverted outputs of the first OR plane will be presented to the second OR at the high half of the second cycle. The final C_i's results then are ready in the low half of the second cycle. Right after the generation of every C_i's, they are inverted and fed into the S_i's function blocks. Another half cycle then is required to produce all of the S_i's. The final result will be latched after 2 cycles as shown in Fig. 5.

Area : As for the transistor count of the PLA-styled implementation for CLA using the modified dual-V_t domino logic, an analytic form is obtained after detailed derivations. In summary, if an n-bit CLA is to be realized by our methodology, the transistor count can be computed as : $T_{total} = \frac{1}{6}(n+1)(n+2)(n+3) + \frac{9}{2}n(n+1) + 48n + 9$.

3. PERFORMANCE SIMULATIONS AND COMPARISON

The detailed schematic and layout of the CLA implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm 1P6M CMOS process shown in Fig. 6 and 7, respectively. An example of the

output waveform of the proposed CLA using the modified dual-V_t domino logic shown in Fig. 8 illustrates that the result of an addition appears after two clock cycles. The characteristics of the proposed low power CLA is tabulated in Table 1.

To reveal the power-saving advantage of the proposed low power design, two 8-bit adders are, respectively, implemented by the modified single-V_t domino logic and the modified dual-V_t domino logic using the same CMOS process. Both power consumption are shown in Table 2 given the same input sequences. The simulations are carried out by HSPICE Monte Carlo method with sweep = 30.

A power consumption comparison with a prior work [6] is shown in Table 3. It is obvious that the proposed design possesses the smaller power consumption.

4. CONCLUSION

We propose a low power high speed PLA-styled dual-V_t domino logic design for the adders' implementation. A modified dual-V_t domino logic circuit is used for pipeling structure and the unnecessary power consumption is avoided. Not only the correctness of the function in the giga hertz range is preserved, but also the power dissipation is reduced. The PLA-styled dual-V_t domino logic structure using only one clock makes the result of an 8-bit adder appear in two cycles. It can be easily expanded to a hierarchical 64-bit adder such that the result will be attained in 4 cycles.

Table 1: Characteristics of the modified dual-V_t domino logic 8-bit adder

	proposed CLA
VDD	1.8 V
highest system clock	1.0 GHz
input data rate	500 MHz
avg. power	2.63 mW ‡
area	1.02×1.02 mm^2
transistor count	882

‡ : at TT model 25°C.

Table 2: Power reduction by using the modified dual-V_t domino logic circuitry

data rate	modified single-V_t	modified dual-V_t	reduction
500 MHz	3.21 mW	2.63 mW	18% ‡

‡ : at TT model 25°C.

Table 3: Comparison of power consumption

	[6]	modified dual-V_t
CMOS Process	1P5M 0.25 μm	1P6M 0.18 μm
VDD	2.5 V	1.8 V
data rate	500 MHz	
avg. power	7.5 mW	2.63 mW

5. REFERENCES

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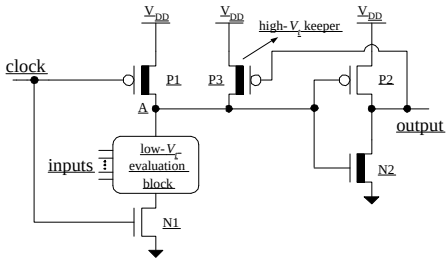

Figure 1: Typical dual-V_t domino logic

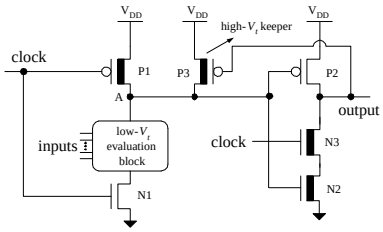

Figure 2: Modified dual-V_t domino logic

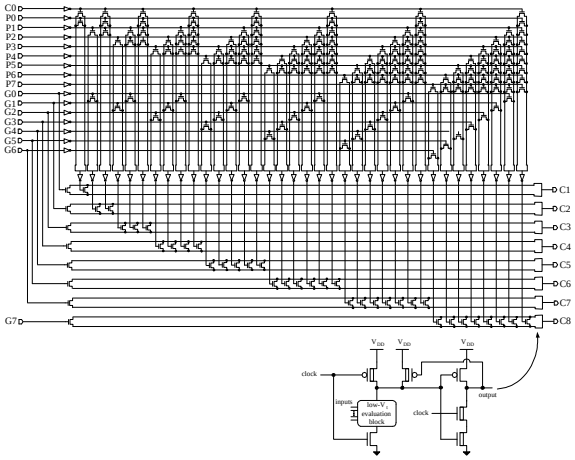

Figure 3: PLA-styled CLA

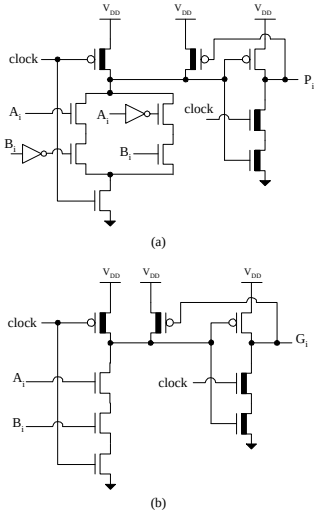

Figure 4: GP block

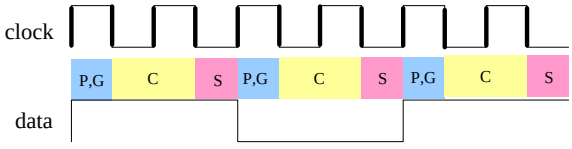

Figure 5: Operation timing of the PLA-styled CLA

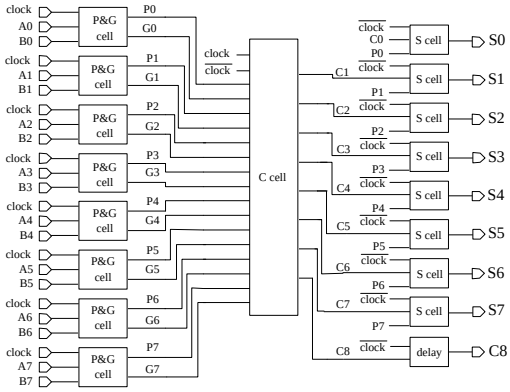

Figure 6: Schematic of the proposed CLA

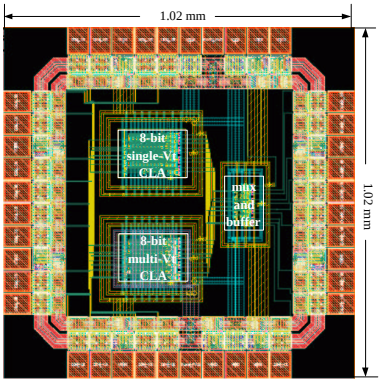

Figure 7: Layout of the proposed CLA

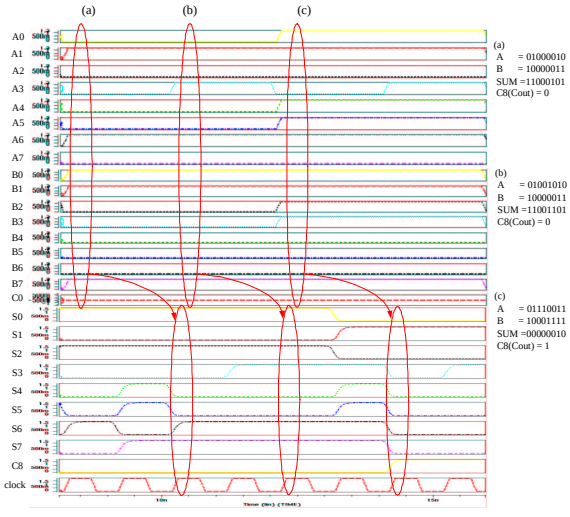

Figure 8: Post-layout simulation result