A 19-T Full Adder With High Impedance Circuits and Conflict Circuits for Mobile Devices' Controllers

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***Abstract* — This paper presents a 19-T (19 transistors) full adder with high impedance circuits and conflict circuits. The transistor count is dramatically reduced such that the power dissipation as well as the area on chip is very small. The output stage is full-swing without output buffers. The sum circuit has only 11 transistors, while the carry circuit has only 8 transistors. The power-delay product is 4.72e-14 fJ. The die size of the 1-bit full adder is merely 40 × 12 μm². A 8-bit full adder which consists of a total of eight proposed full adders is also implemented by TSMC 1P6M 0.18 μm CMOS process.**

***Key Words* — full adder, asynchronous, high impedance, conflict circuit**

I. INTRODUCTION

rFull adders have been renowned as fundamental components for filters, controllers, and CPUs in communication systems' base-band circuitry. Many adders have been proposeded in literature, [4] – [9]. The 28-T full adder in [4] is a classical CMOS full adder. Because [4] has too many VDD or GND paths, the P-N matching is very difficult. Many glitches are generated when input state switches. [4] has an alternative implementation which is designed by complementary pass-transistor logic (CPL) [11]. The CPL full adder has 32-T to consume more die area. A transmission function full adder [5] and a transmission gate adder [6] have less transistor counts. Since the output stages of these two full adders are transmission gates, output buffers must be added at the output to restore the swing. Pass transistor circuits, such as [8] and [9], also have less transistor count. However, the output swings of the pass transistor circuits are shrunk when a PMOS passes 0 or a NMOS passes 1 [1] – [3]. In order to have a full swing output, the output stage of the pass transistor circuit needs output buffers, too. This paper presents a novel full adder using high impedance circuits and conflict circuits to generate full-swing output without any buffer. The proposed adder not only reduces the transistor count, but also maintains full output swing to reduce area as well as power dissipation.

II. THE PROPOSED 19-T FULL ADDER

The proposed 19-T full adder is designed by utilizing high impedance circuits and conflict circuits. A simple high impedance circuit is shown in Fig. 1. OUT is at high impedance state when NM0 and NM1 are both OFF. In the high impedance state, OUT is floating, and the voltage of OUT is basically decided by the prior state. In order to avoid a state transition at OUT during the high impedance state, $I_{leakage}$ must be small. A long channel transistor has the leakage current from 10e-14A to 10e-17A. A deep-submicron transistor has the leakage from 10e-12A to 10e-10A [10]. Therefore, $I_{leakage}$ does not cause any state transition at OUT if the operation frequency of the proposed full adder is more than several mega-hertz.

A simple conflict circuit is shown in Fig. 2. OUT is at a conflict state when NM0 and NM1 are both ON. The voltage of OUT is decided by the strong signal path (V1-NM0-OUT) of the inputs. The state equation of OUT is shown as follows,

$$P1(V1) + P2(V2) \rightarrow P1(V1)_s + V2_w \qquad (1)$$

R_{NM0} is the equivalent path resistance of the signal path V1-NM0-OUT, and R_{NM1} is the equivalent path resistance of the signal path V2-NM1-OUT. R_{NM0} and R_{NM1} must satisfy Eqn. (2) and (3) to resolve the conflict scenario.

When OUT=0, then

$$VDD\frac{R_{NM0}(strong)}{R_{NM0}(strong)+R_{NM1}(weak)} < \frac{1}{2}VDD \qquad (2)$$

When OUT=1, then

$$VDD\frac{R_{NM0}(weak)}{R_{NM0}(weak)+R_{NM1}(strong)} > \frac{1}{2}VDD \qquad (3)$$

A. The carry circuit

The I/O port of the proposed 19-T adder is defined as Fig. 3. The carry circuit of the 28-T classical full adder in [4] is shown in Fig. 4. The carry circuit of the 28-T classical full adder has 14 transistors as shown in Fig. 5. By the high impedance circuits and the conflict circuits, four MOSs can be saved. The K-map of COUT is simplified by high impedance and conflict concept as shown in Fig. 6. When AB={11} or AB={00}, CIN does not flip the state of COUT. When AB={10} or AB={01}, COUT equals to CIN. Then, the proposed carry circuit in shown in Fig. 7. The transistor count of the proposed carry circuit is reduced to 8. The W/L ratio of the transistors in the strong path and the weak path must satisfy Eqn. (2) and Eqn. (3). Besides, the P-N mobility and path transistor numbers must also be considered when deciding the W/L ratio of the transistors.

B. The sum circuit

The sum circuit of the 32-T CPL full adder [11] shown in Fig. 8 has 14 transistors. Although the CPL full adder can operate at low voltage, the CPL full adder occupies large die area and power [11]. By the high impedance circuits and the conflict circuits, the four MOSs controlled by CIN and $\overline{\text{CIN}}$ are replaced by one transistor. What even better is that the pull-up PMOSs, PM0 and PM1 are saved. The proposed sum circuit is shown in Fig. 9, which has a strong path and a weak path. When CIN=1, SUM is decided by the strong path. When CIN=0, the strong path is at high impedance such that SUM is decided by the weak path. The transistor count of the proposed sum circuit is reduced to 11 transistors. The transistor count is dramatically reduced.

III. SIMULATION & IMPLEMENTATION

The proposed 19-T full adder is carried out by TSMC 1P6M 0.18 μm CMOS process. Fig. 10 is a thorough simulation of the proposed full adder at $25^{o}C$ TT model. Fig. 11 shows the simulation results at another two PVT corners, $0^{o}C$ FF model and $75^{o}C$ SS model, respectively. The die size of the 1-bit 19-T adder is 40 μm × 12 μm as shown in Fig. 12. Table I is a comparison of the power-delay product between our full adder and several prior adders without any I/O buffers. The proposed full adder has a better power-delay product. Table II is a comparison of the power-delay product between our full adder and the prior adders with I/O buffers operating at 200 MHz frequency. The proposed adder still has a better power-delay product than the other works. In order to prove physical feasibility of our full adder based on the proposed full adder is carried out. The post-layout simulation given a 200 MHz data frequency is shown in Fig. 13. The layout of the 8-bit ripple adder is shown in Fig. 14.

VI. CONCLUSION

This paper presents a 19-T asynchronous full adder with high impedance circuits and conflict circuits. The proposed adder has a low transistor count adder without I/O buffers. The power-delay product compared with state-of-art works is very appealing. A 8-bit adder based on the proposed adder given a 200 MHz data frequency.

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Table I: Power-delay products of the full adders without buffers

	transistor count	power-delay product
the proposed full adder	19	4.72E-14 fJ
CMOS28T [4]	28	8.30E-14 fJ
CPL32T [4]	32	9.53E-14 fJ

Table II: Power-delay products of the full adders with I/O buffers (Each buffer has four transistors.)

	transistor count	power-delay product
the proposed full adder with buffers	19+20	1.59E-13 fJ
TGA20T [5]	20+20	2.33E-13 fJ
TFA16T [6]	16+20	2.03E-13 fJ
14T [7]	14+20	1.64E-13 fJ
10T [8]	10+20	1.22E-12 fJ

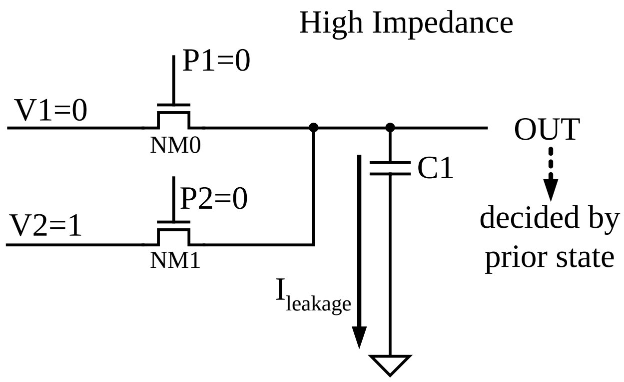

Fig. 1: The high impedance state of a circuit

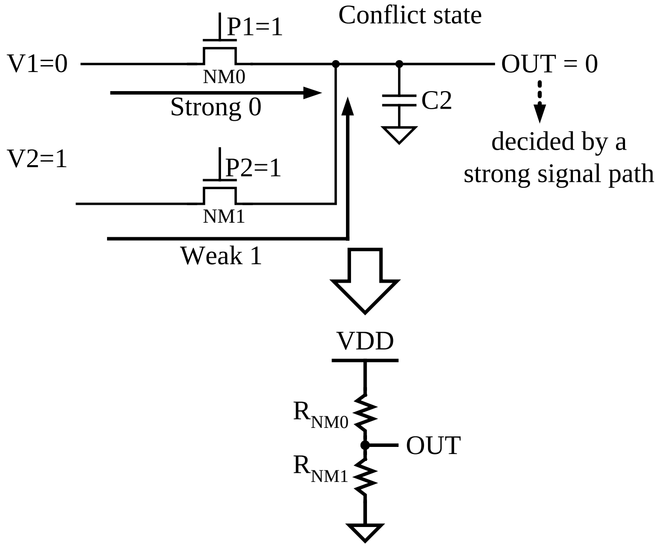

Fig. 2: The conflict state of a circuit

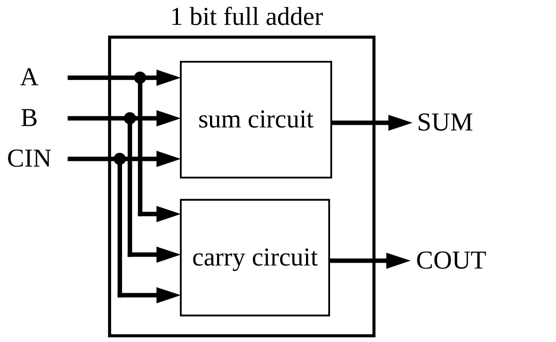

Fig. 3: The port definition of the proposed 1-bit full adder

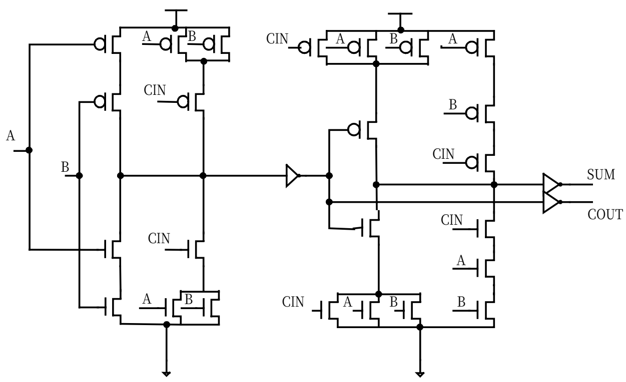

Fig. 4: The schematic of the 28T adder [4]

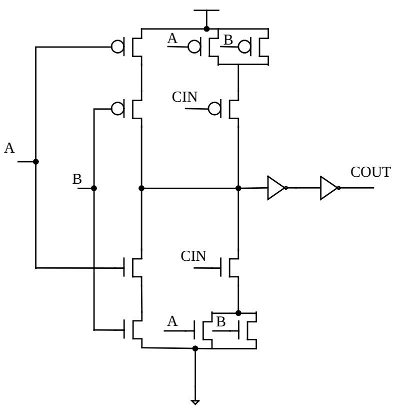

Fig. 5: The carry circuit of the 28T adder

COUT

CIN \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

COUT

B \ A	0	1
0	0	Z
1	Z	1

Conflict

COUT = CIN

Fig. 6: Simplified carry table by high impedance logic and conflict logic

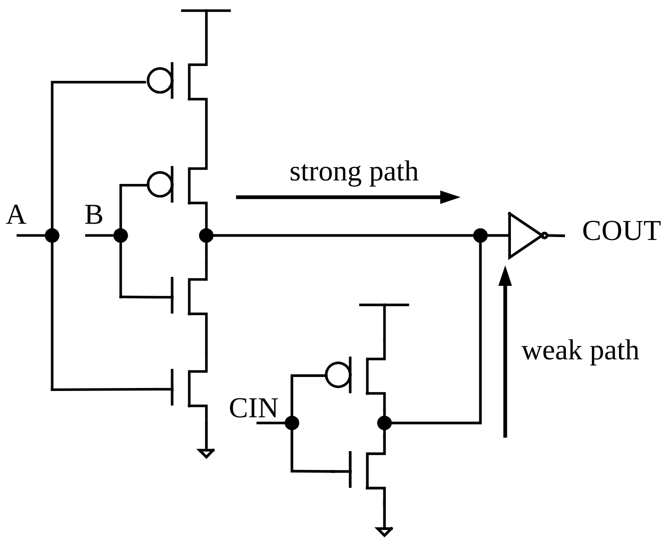

Fig. 7: The schematic of the proposed carry circuit

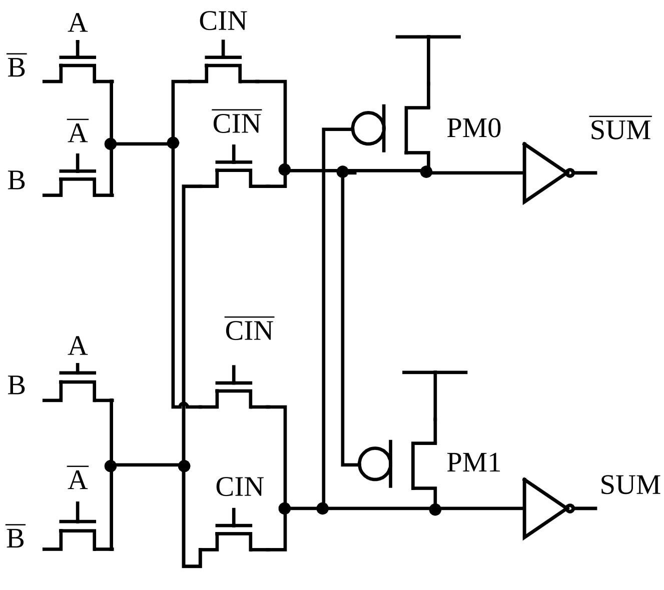

Fig. 8: The CPL sum circuit

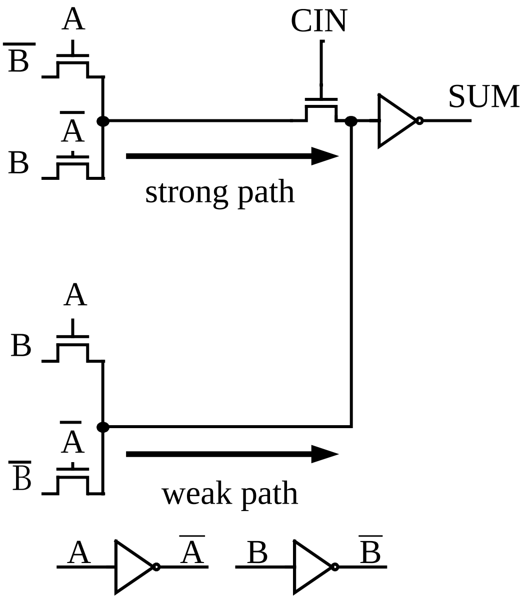

Fig. 9: The proposed sum circuit

Fig10: The simulation results of the proposed adder 25^{o}C TT model

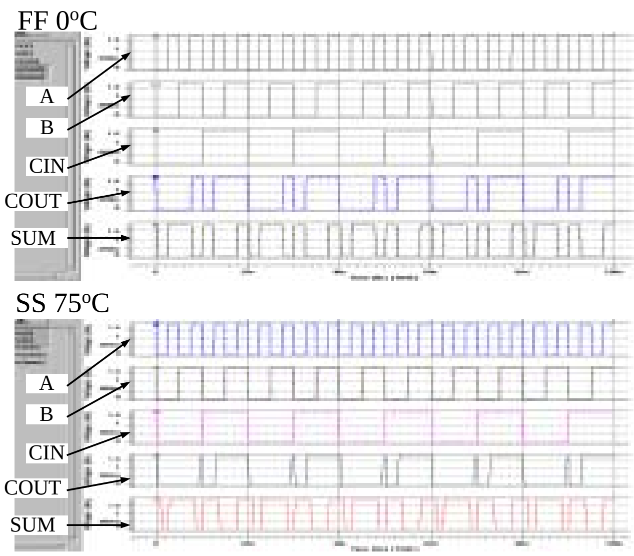

Fig. 11: The simulation results of the proposed adder at 0^{o}C FF model and 75^{o}C SS model

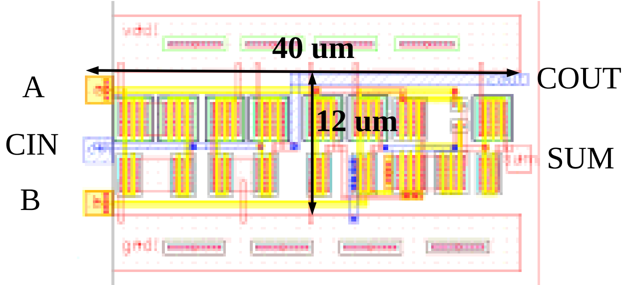

Fig. 12: The layout of the proposed 1-bit full adder

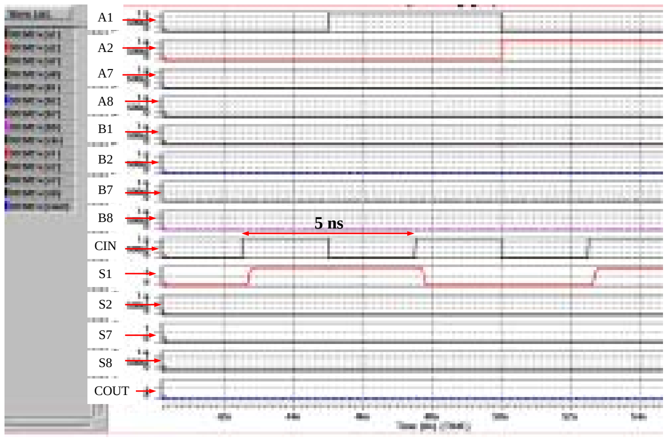

Fig. 13: The simulation waveform of the 8-bit ripple adder at 200 MHz data frequency

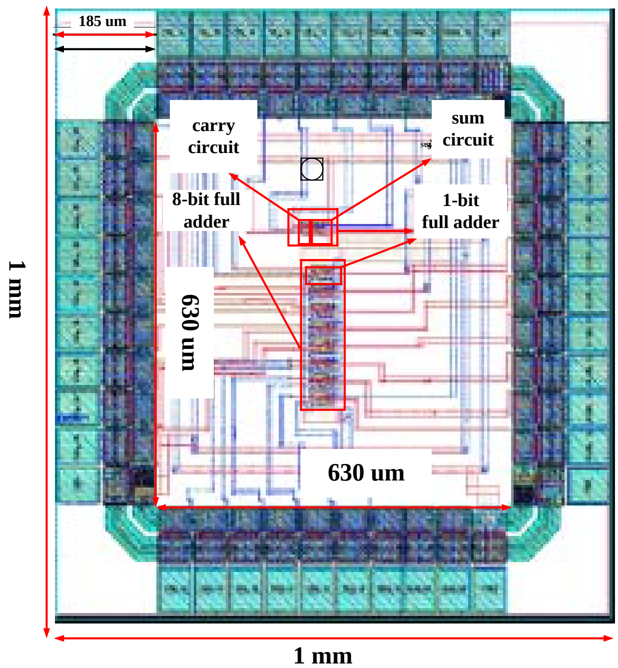

Fig. 14: The layout of the 8-bit ripple adder