A 9-bit 20-MSample/s Pipeline ADC for NTSC Video Decoders

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***Abstract* — This paper presents a 9-bit, 20 MSample/s pipeline analog-to-digital converter (ADC) for NTSC video decoders. The sharing amplifier technique is employed to reduce the overall number of the amplifiers wherein dynamic comparators are adopted to reduce the power consumption. The proposed design is implemented by 0.35 μm CMOS technology. The post-layout simulation results show that the maximum power consumption is 45mW given a 3.3 V power supply, and the SFDR is 54 dB with a sinusoidal input at 5 MHz. The ADC occupies 2.75 mm^2 on silicon**

***Key Words* — analog-to-digital converter, pipeline, NTSC.**

I. Introduction

The NTSC (national television system committee) video decoder is the key component of traditional analog televisions. The subcarrier frequency of NTSC signal is 3.58 MHz, such that the sampling frequency of the ADC is usually set to be five or six times of that of the incoming signal to reduce the quantization error [1], [2]. In this paper, we develop a 9-bit, 20 MSample/s ADC for NTSC video decoder to resolve the requirement. The architectures of the ADCs satisfying the requirement of such a high speed and medium resolution ADC include flash ADC, two step flash ADC and pipeline ADC. Although the flash ADC has the fastest conversion speed, it requires a large number of comparators such that the power consumption and the die size are not acceptable in many applications. By contrast, the two step flash ADC requires fewer comparators compared to the full flash ADC, but its input signal is limited to relatively low frequency due to the inherent parallel signal quantization scheme [7]. Hence, pipeline ADC becomes an attractive option in video-rate applications. The primary advantages of the pipeline architecture are the high throughput rate due to the concurrent operation of each stages in the pipeline structure, and its power-and area-efficiency compared to the other architectures.

This paper presents the 9-bit, 20 MS/s pipeline ADC suitable for the quantization of the RF tuner output prior to the NTSC video decoder. The proposed ADC employs a 8-stage pipeline architecture. The resolution of first 7 stages is 1.5-bit per stage, while the last stage utilizes a 2-bit resolution flash ADC. The redundant bits are used to perform the error correction against the nonideality of the ADC.

II. Pipeline ADC architecture

The architecture of the 9-bit pipeline ADC is composed of seven stages of the 1.5-bit ADC and one stage of the 2-bit flash ADC, as shown in Fig. 1. Each 1.5-bit ADC, which means the resolution per stage is 1.5 bit, contains an sample-and-hold (S/H) circuit, a low-resolution analog-to-digital subconverter sub-ADC, a low resolution digital-to-analog subconverter sub-DAC, and a fixed-gain amplifier. The sub-ADC resolves two bits output by quantized the input signal. The quantization result of the sub-ADC is converted into an analog magnitude by the sub-DAC. Thus, the residue is obtained by subtracting this magnitude from the input signal. The residue is multiplied by the gain of 2 for the next stage. The residue computation and the precise amplification of the gain of 2 are realized by a multiplying digital-to-analog converter (MDAC) [4]. Since there is no need to produce residue in the last stage, the 2-bit flash ADC is adopted in the last stage to resolve the overall resolution of 9 bits. In order to reduce the power consumption, the comparators in each stage are implemented by the dynamic comparators [5], and the sharing amplifiers technique [6] is also adopted to reduce the overall number of the operational amplifiers (opamp) by sharing the opamp between every two adjacent 1.5-bit ADCs.

A. 1.5-bit ADC

The block diagram of the 1.5-bit ADC, which is composed of two comparators and one MDAC, is illustrated in Fig. 2. Fig. 3 depicts the block diagram of MDAC. In order to possess a large tolerance to component nonidealities, redundancy is introduced by making the sum of the resolutions in each stage greater than the total resolutions. The 1.5-bit ADC which has 1.5 bit resolutions per stage is preferable because it benefits from two advantages: large bandwidth of the switched capacitor circuit and large tolerance of comparator voltage offset. Since the bandwidth of the switched capacitor circuit depends on the inter-stage gain, low closed-loop gain configuration is preferable for retaining a fast settling time of the output signal. With the 1.5 bit resolution per stage, the closed-loop gain of 2 cooperates to achieve the large bandwidth due to the low load capacitance and large feedback factor compared to the prior large resolution per stage configuration. The second advantage is that the resolution of 1.5 bit per stage allows large correction tolerance for comparators, since only

two comparaotrs are required in a sub-ADC where the comparator tolerance is up to $\pm V_{ref}/4$ [7].

Referring to Fig. 2, the relationship between the input V_{n-1} and the output V_n of 1.5-bit ADC can be expressed as following equation :

$$V_{n-1} = \begin{cases} (1+\frac{C_s}{C_f})V_n - V_{ref}, & \text{if } V_n > V_{ref}/4 \\ (1+\frac{C_s}{C_f})V_n, & \text{if } -V_{ref}/4 \le V_n \le V_{ref}/4 \\ (1+\frac{C_s}{C_f})V_n + V_{ref}, & \text{if } V_n < -V_{ref}/4 \end{cases} \quad \ldots(1)$$

where C_f and C_s are the sampling capacitor and feedback capacitor, respectively, in the MDAC depicted in Fig. 2. In the 1.5 bit/stage architecture, C_s is set to be equal to C_f to attain the gain of two. Fig. 4 shows the relationship between V_n and V_{n-1}. Since the mismatch of C_s and C_f will directly result in the non-linearity of the ADC, the layout of these two capacitors should be extremely careful.

B. Dynamic comparator

Fig. 5 shows the schematic of the dynamic comparator adopted in the MDAC. Since there are a total of 17 comparators in the proposed 9-bit ADC (2 comparators per 1.5-bit ADC, and 3 comparators per 2-bit flash ADC), the dynamic comparator is utilized to reduce the power consumption. The dynamic comparator only operates at the low-to-high transition of LATCH signal such that it consumes less power than traditional comparators.

C. Amplifier sharing

Since the amplifier is the primary component consuming most power in the ADC, reduction of the number of the amplifiers leads to a significant reduction of the power consumption. This approach can be accomplished by sharing the amplifier between two adjacent stages. The sub-ADCs of two adjacent stages execute different tasks on opposite phases: one is sampling the incoming signal, when the other is performing the amplification and subtraction. The amplifier of the MDAC is not required to do anything when sampling the incoming signal. Thus, MDACs between two adjacent stages can share the same amplifier. Fig. 6 is the schematic showing the sharing of an amplifier between two adjacent stages. The sharing amplifier technique suffers from two drawbacks. First, the switches which are used to accomplish the sharing amplifier scheme introduce the series resistance which might affect the settling behavior of the stage. Second, since the amplifier will never be reset, every input sample is affected by the finite-gain error due to previous sampling [6]. However, the first problem can be resolved by using large switches, and the second problem can be negligible if the amplifier gain is sufficiently large.

III. Implementation and Simulation

The proposed ADC design is carried out by TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 1P4M CMOS technology to verify the performance. The layout of the proposed prototype on silicon is shown in Fig. 7. Fig. 8 presents the differential nonlinearity (DNL) of the proposed ADC where the maximum is 0.41 LSB. Meanwhile, Fig. 9 depicts the integral nonlinearity (INL) where the maximum is 0.74 LSB. Fig. 10 shows the spurious-free dynamic range (SFDR) of 54 dB with a sinusoidal input at 5MHz. The specifications of the proposed prototype are summarized in Table I. A comparison of our proposed ADC and several prior works is summarized in Table II. Our design possesses least area as well as acceptable power consumption.

TABLE I
SPECIFICATIONS OF THE PROPOSED ADC

Technology	0.35 μm
Conversion rate	20 MS/s
Resolution	9 bits
DNL	0.41 LSB
INL	0.74 LSB
area	2.57 mm^2
Power consumption	45 μW @ 20 MHz

TABLE II
COMPARISON

	ours	[7]	[8]	[9]
Conversion rate (MS/s)	20	20	20	14.3
Power consumption (mW)	45	35	240	14.3
Resolution (bits)	9	10	10	10
Area (mm^2)	2.75	10.5	8.7	5.75

VI. Conclusion

A 9-bit, 20 MS/s pipeline ADC for the NTSC video decoder is presented in this paper. By using the sharing amplifier technique, only five amplifiers are required to accomplish a 9-bit ADC. The dynamic comparator is adopted to reduce the power consumption. The post-layout simulation results show the SFDR of 54 dB with a sinusoidal input at 5MHz. The proposed ADC occupies 2.75 mm^2 and consumes 45 mW given 3.3 V power supply.

Acknowledgement

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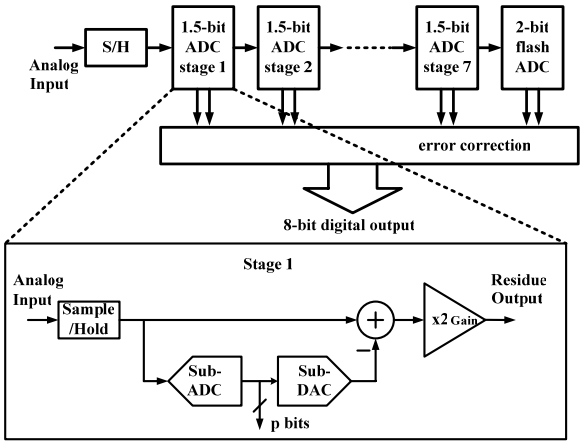

Fig. 1. Block diagram of the proposed pipeline ADC

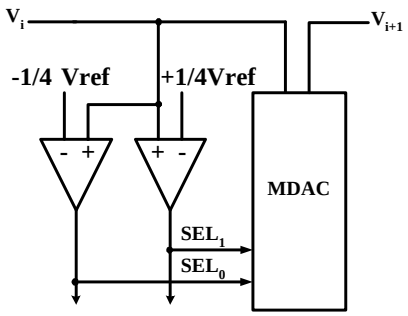

Fig. 2. Block diagram of the 1.5-bit ADC

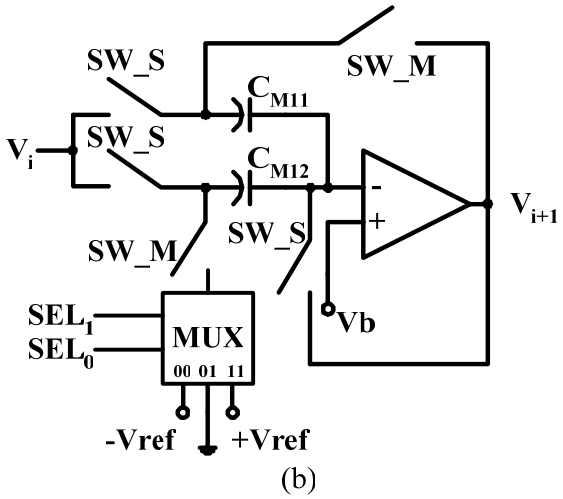

Fig. 3. Block diagram of the MDAC

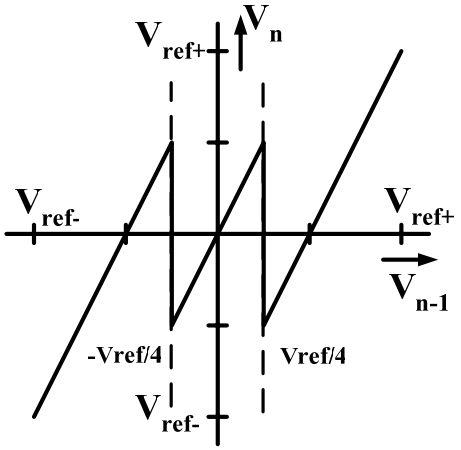

Fig. 4. V_{n-1} versus V_n

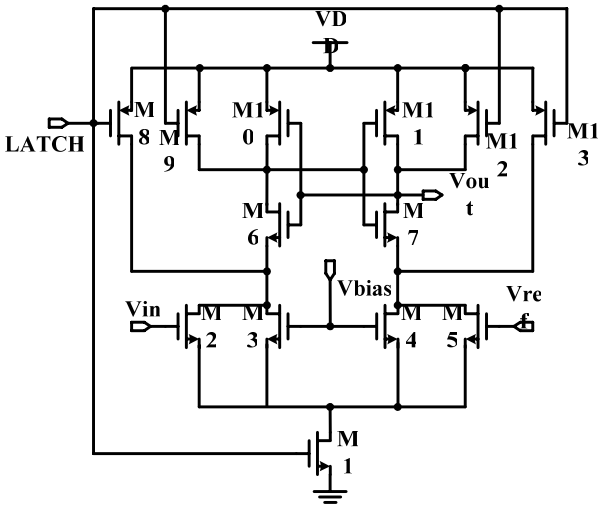

Fig. 5. The schematic of the dynamic comparator

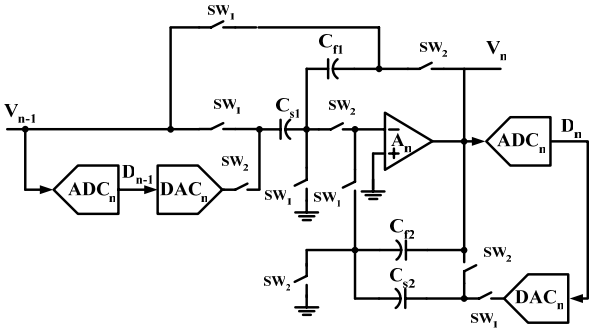

Fig. 6. The schematic showing the sharing of an amplifier between two adjacent stages

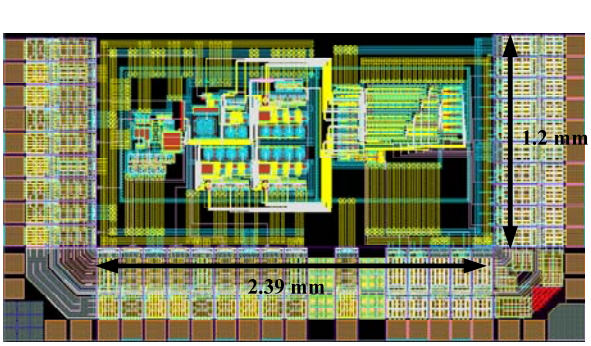

Fig. 7. Layout of the ADC

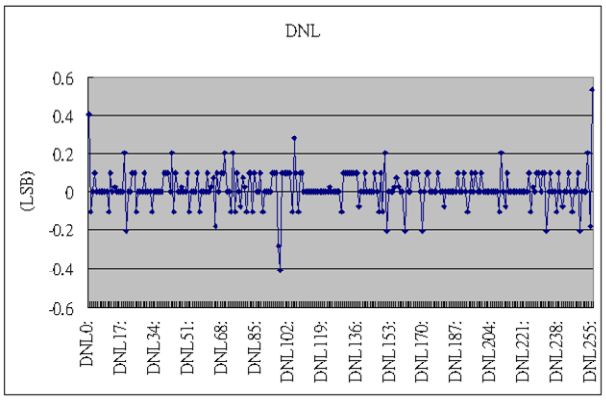

Fig. 8. DNL of the ADC

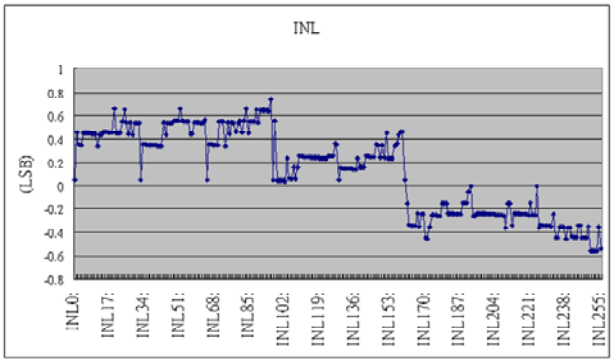

Fig. 9. INL of the ADC

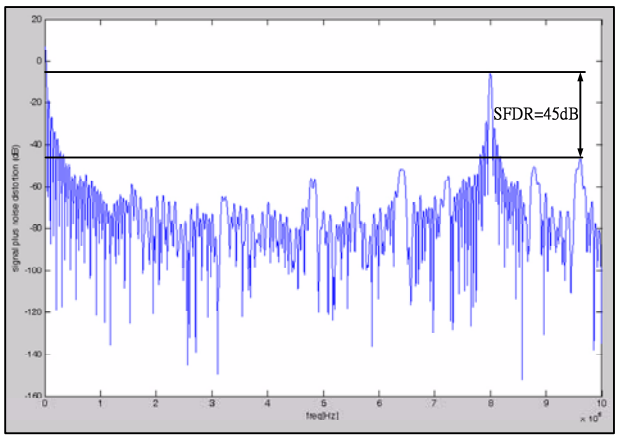

Fig. 10. SFDR of the ADC