868/915 MHz ZigBee Receiver for Personal Medical Assistance*

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***Abstract*-- This paper presents an architecture as well as circuit implementation of ZigBee receiver using 868/915 MHz band, which is compliant to the physical layer of IEEE standard 802.15.4. The post-layout simulation shows the packet error rate is less than 1% given SNR = 5 dB. The maximum power consumption is merely 183 μW at 2.5 MHz.**

I. INTRODUCTION

ZigBee is a novel wireless standard aiming at a low data rate, low cost, and low power wireless data transformation. ZigBee is similar to Bluetooth, but it is simpler and spends most of time dozing. The major applications of ZigBee focus on sensor and automatic control, such as personal medical assistance, industrial control, home automation [1], and remote control and monitoring. It is particularly suitable to be installed in a personal medical monitoring device for senior citizens because of low power consumption. The physical (PHY) layer and media access control (MAC) layer of ZigBee follow the IEEE 802.15.4 wireless personal area network (WPAN) standard [2]. The specification of the application layer and the security layer are defined by ZigBee Alliance [3]. The IEEE 802.15.4 standard specifies that a compliant system shall operate in three licence-free bands: 2.45 GHz, 868 MHz for North America, and 915 MHz for Europe. This paper presents a ZigBee receiver using 868/915 MHz band.

II. ZIGBEE RECEIVER FOR 868/915 MHZ BAND

Fig. 1 depicts the format of the ZigBee physical layer protocol data unit (PPDU) packet. The preamble field, which contains 32 bits "0", is for the packet detection and the synchronization in the receiver. The SFD field denotes the start of the packet data. The frame length field indicates the number of octets of the physical layer service unit data unit (PSDU). The PSDU carries the data of the packet.

The ZigBee transmitter for the 868/915 MHz band is illustrated in Fig. 2. The PPDU packet is composed of the binary data from PSDU and the header added by the header insertion stage. The differential encoder stage encodes the PPDU packet for error correction. The bit-to-chip stage performs the direct-sequence spread spectrum (DSSS), where each bit of the PPDU packet is mapped into a 15-chip pseudo-random noise (PN) sequence ("0" to "111101011001000", and "1" to "000010100110111"). The binary phase shift keying (BPSK) modulation is adopted. The modulated signal goes along with the pulse shaping stage to reduce the inter-symbol interference (ISI) [4]. Table 1 summarizes the specification of 868/915 MHz band [2].

Octets: 4	1	1		variable
Preamble	Start of frame delimiter	Frame length (7 bits)	Reserved (1 bit)	PSDU
Synchronization header		PHY header		PHY payload

Fig. 1. PPDU packet format

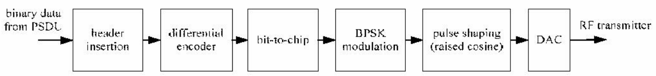

Fig. 2. ZigBee transmitter model for 868/915 MHz band

TABLE I
FREQUENCY BAND AND DATA RATE

Band (MHz)	Bit Rate (kb/s)	Chip Rate (kchip/s)	Modulation
868/915	20/40	300/600	BPSK

According to the receiver sensitivity defined in [2], the packet error rate (PER) should be less than 1% when the PSDU length is 20 octets and the signal-to-noise ratio (SNR) is 5 to 6 dB.

Fig. 3 shows the block diagram of the ZigBee receiver for 868/915 MHz band. The RF signal is down-converted to basdband (300/600 KHz in 868/915 mode) by RF module and quantized by the analog-to-digital converter (ADC). In order to reduce quantization error such that a better frequency estimation can be attained, the sampling rate of the ADC is four times of the input signal frequency. The packet detector discriminates whether the incoming signal is data or noise. It enables the following stage if the incoming signal is determined to be data. Each 15-chip PN sequence is sampled to be 60 samples by the ADC. The energy detector is in charge of positioning the chips from the samples. The frequency estimation block computes the frequency offset from samples and corrects the frequency of local oscillator by returning a control signal. The time synchronization indicates the start of each PPDU packet. With the acknowledgement of the start of the packet, the differential decoder proceeds to decode the packet. The confirm SFD stage acquires the length of the PSDU and notifies the MAC layer of receiving the PSDU from receiver.

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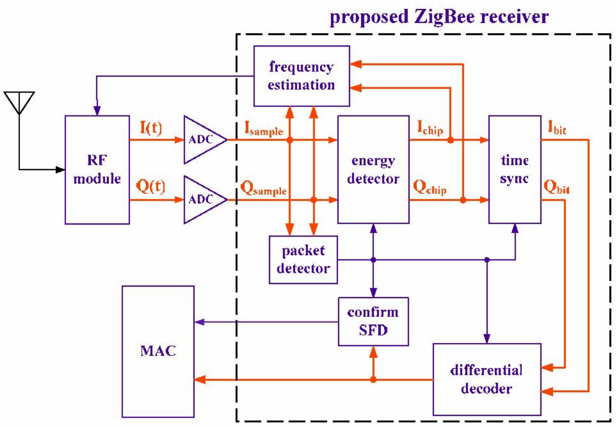

Fig. 3. Block diagram of the proposed ZigBee receiver for 868/915 MHz band

A. *ADC Specification*

The requirement of the ADC resolution is derived from the system simulation illustrated in Fig. 4. Accordingly, a 4-bit resolution is sufficient even when the SNR is 4 dB.

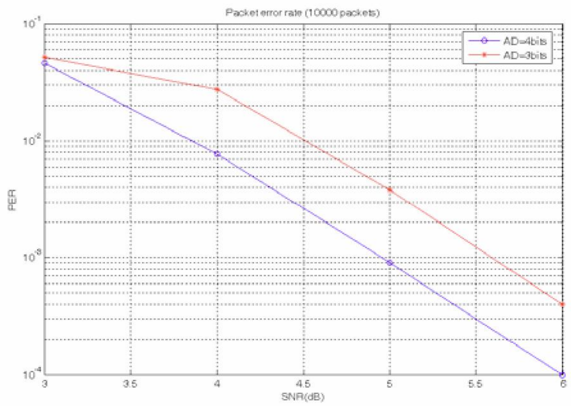

Fig. 1. Simulation of the requirement for ADC resolution

B. *Packet Detector and Energy Detector*

The absolute value of I_{sample} and Q_{sample} are accumulated for certain time interval. If the accumulated value is greater than the threshold, the incoming signal is determined as data. This threshold is derived from detailed system simulations. The energy detector derives the positions of the chips from I_{sample} and Q_{sample}.

C. *Frequency Estimation*

The operation of the frequency estimation consists of two phases, *coarse* and *fine*. The frequency estimation stage performs the similar operations in these two phase such that the same hardware is reused. The phase angle of a pair of I_{sample} and Q_{sample} can be obtained by mapping the I_{sample} and Q_{sample} to the Cartesian coordinate. A phase rotation is the difference between two adjacent phase angles. In the *coarse* phase, the frequency estimation stage calculates the average phase rotation of 128 pairs of I_{sample} and Q_{sample}. Then, it corrects the frequency of the local oscillator by returning an 8-bit control signal. In the *fine* phase, it uses I_{chip} and Q_{chip}, which are derived from I_{sample} and Q_{sample} by the energy detector, to calculate the average phase rotation and send an 8-bit control signal to the local oscillator.

D. *Time Synchronization*

The time synchronization stage de-spreads the received chips by a matched filter [5] and acquires the preamble of PPDU. The incoming I and Q chips is converted from chips to bits for decoding.

E. *Confirm SFD*

The confirm SFD stage determines the frame length by acquiring the SFD field of the PPDU packet and acknowledges the MAC layer to receive the PSDU by sending an alarm signal.

III. Measurement and Simulation Result

The function of the proposed ZigBee receiver for 868/915 MHz band is verified by FPGA Xilinx Virtex-II XC2V1500. In order to evaluate the power consumption, the proposed design is implemented by a standard 0.18 um 1P5M CMOS technology to verify the power consumption. The post-layout simulation manifests the PER is less than 1% when the SNR is 5 dB. Table 2 summarizes the results of the post-layout simulation.

TABLE II
Post-Layout Simulation Results

maximum clock frequency	2.5 MHz
power supply	1.8 V ± 10 %
core size	0.107 mm^2
power consumption	183 μW @2.5 MHz

References

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