A 0.18 μm CMOS Prototype of COFDM Demodulator for European DVB-T Standard*

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Abstract--This paper presents a prototype of the COFDM demodulator conforming to the European DVB-T standard. The proposed prototype mainly contains four blocks: time synchronization, frequency synchronization, 2K/8K FFT processor, and channel estimation. Each block is implemented by the relatively simple algorithm to avoid the overhead of hardware complexity. TSMC 0.18 μm CMOS technology is adopted to carry out the proposed COFDM demodulator. The proposed prototype uses 637 Kbits of SRAM and occupies a total area of 17.2 mm^2.

INTRODUCTION

The standard of digital video broadcasting for terrestrial transmission (DVB-T) [1] was finalized in 1997. This standard was developed upon the earlier DVB standard for satellite and cable system. Since the effect of multipath in terrestrial transmission is much greater than the transmission in the satellite and cable system, the terrestrial broadcasting is more challenging. Owing to the coded orthogonal frequency division multiplexing (COFDM) modulation, which is a multicarrier modulation used in conjunction with channel encoding, it copes well with multipath so much so that the concept of a single frequency network (SFN) becomes feasible [2].

In Fig. 1, the conceptual block diagram of the COFDM modulation and demodulation for DVB-T system is presented. The channel encoding methods in DVB-T are Viterbi and Reed-Slomon coding. The modulator in DVB-T supports following modulation schemes: quadrature phase-shift keying (QPSK), 16 quadrature amplitude modulation (16-QAM), 64-QAM, and multiresolution constellation for hierachical modes. The frequency division multiplexing scheme, such as COFDM, was proven to be equivalent to an inverse discrete Fourier transform (IDFT) at the transmitter, and a discrete Fourier transform (DFT) at the receiver [3]. In general, IDFT and DFT are replaced with inverse fast Fourier transform (IFFT) and fast Fourier transform (FFT).

However, there are still many challenges in the COFDM demodulation for DVB-T system. The timing offset in the receiver will cause the misalignment of the FFT window, which will result in a phase rotation of the demodulated signals. The timing offset can be reduced by adjusting the position of the FFT window. The frequency offset due to the frequency difference of local oscillator between the transmitter and the receiver disturbs the orthogonality of the subcarriers of COFDM symbols. Hence, a demodulated subcarrier is interfered by the other subcarriers [4]. The interference described above is known as inter-carrier interference (ICI). In order to maintain the integrity and the orthogonality of the received signal, the timing synchronization and the frequency synchronization are critical parts in the COFDM demodulator. The effects of the transmission channel, such as noise, co-channel interference, and fading channels, will lead to the degradation of the bit error rate (BER). Hence, the channel impulse response should be estimated, and the received carriers should be compensated according to the results of the channel estimation.

Numerous algorithms have been proposed to solve the degeneration of the performance resulting from timing offset, frequency offset, and nonideal channel response, but most of them are not cost-efficient for hardware implementation. This paper presents a prototype of COFDM demodulator for DVB-T system, which adopts relatively simple but effective algorithm. The proposed prototype contains timing synchronization, frequency synchronization, FFT, and channel estimation. The algorithm adopted and the block diagram of each part will be covered in the following section.

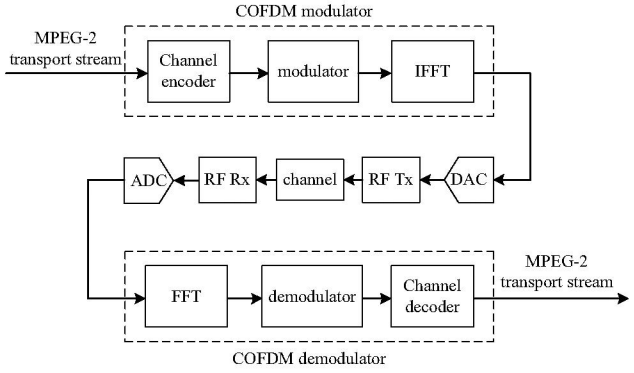

Fig. 1. The conceptual block diagram of the COFDM modulation and demodulation for DVB-T.

PROPOSED COFDM DEMODULATOR FOR DVB-T

Fig. 2 shows the block diagram of the proposed COFDM demodulator for DVB-T. The received time-domain COFDM signals are transferred into frequency-domain subcarriers by a 2K/8K FFT. The time synchronization block adjusts the position of the FFT widow by acquiring a correct start of the COFDM symbol. The fine frequency synchronization block estimates the decimal frequency offset, which is the frequency offset smaller than one subcarriers spacing, and it corrects this frequency offset by sending a control signal to the frequency correction block. After the processing of the FFT, all the signals processing are performed in frequency-domain.

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The subcarriers of COFDM symbol contain continual pilots and scattered pilots, these pilots can be utilized to perform the coarse frequency synchronization and channel estimation. The coarse frequency synchronization block adjusts the position of subcarriers in bit-reverse stage to reduce the frequency offset.

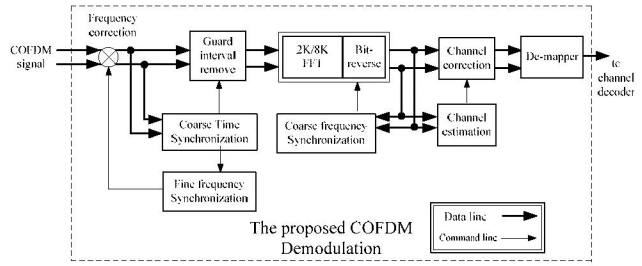

Fig. 2. The block diagram of the proposed COFDM demodulator for DVB-T.

Time synchronization block

In the COFDM demodulation, the start of symbol should be acquired before any further processing. Fig. 3 depicts the guard interval of a COFDM symbol, where N and N_g are the size of a COFDM symbol and guard interval, respectively. The guard interval is a replica of the end of the symbol and is inserted to the beginning of the symbol. The guard interval is mainly employed to absorb the inter-symbol interference (ISI) and help COFDM to acquire the correct start of the COFDM symbol.

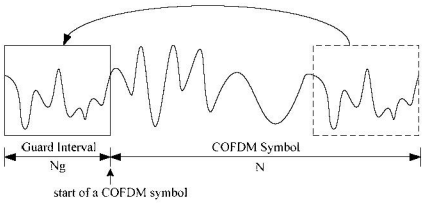

Fig. 3. The guard interval of the COFDM symbol.

The adopted algorithm of the time synchronization [5] is as follows:

$$F(n) = \sum_{l=1}^{N_g-1} y^*_{i,l+n-N} \cdot y_{i,l+n}\ , 0 \le n \le N + N_g, N = 2K \text{ or } 8K, \quad (1)$$

where i is the index number of the COFDM symbols, and n is the index number of the samples of the COFDM symbol.

The start of COFDM symbols is acquired when the $F(n)$ achieves its maximum, which means the correct start of the FFT window is obtained. Fig. 4 shows the block diagram of the time synchronization block, where the comp block is a comparator used to find the maximum of $F(n)$.

Frequency synchronization block

In the communication system, the frequency difference between the local oscillator of the transmitter and receiver causes the frequency offsets of the received signals. These frequency offsets should be estimated and corrected to ensure the orthogonality of the subcarriers, in other words, the frequency of the subcarriers should be synchronized. The frequency synchronization is composed of two parts, the coarse frequency synchronization corrects the frequency offset which is the multiple of one subcarrier spacing, and fine frequency synchronization corrects the decimal frequency offset, which means the frequency offset that is less than one subcarrier frequency spacing.

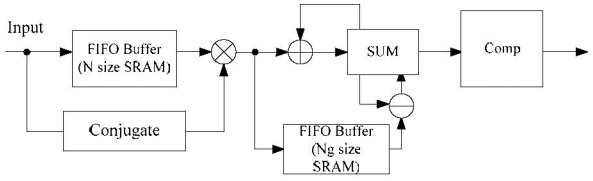

Fig. 4. The block diagram of the time synchronization block.

Coarse frequency synchronization block: The coarse frequency synchronization in the proposed design is performed after the processing of the FFT. The selected scheme is based on the frequency-domain data-aided (DA) algorithm [6]:

$$\mu(d) = \sum_k w(k-d) \cdot Y_{i,k}\ ,\ w(k) = \begin{cases} X^*_{i,k}\ ,\ if\ k \in \mathrm{K_{cpt}} \\ 0\ ,\ \text{otherwise} \end{cases} \quad (2)$$

where i and k are symbol index and subcarrier index, respectively. The $Y_{i,k}$ in Eq. (2) is the subcarrier derived from the received samples by the FFT. The $w(k)$ in Eq.(2) is the set of the continuous pilots, $X^*_{i,k}$. The coarse frequency offset is estimated by correlating the complex conjugate of the known continuous pilots with the subcarriers, and the value of d where $\mu(d)$ achieves its maximum is denoted as d_{opt}, which is the value of the frequency offset. Since the d_{opt} represents a multiple of the one subcarrier frequency spacing, we can directly adjusts the positions of the subcarriers in the bit-reverse stage to correct the frequency offset. The block diagram of the coarse frequency synchronization is shown in Fig. 5.

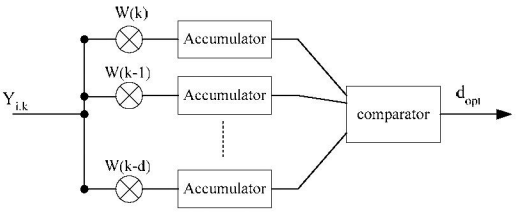

Fig. 5. The block diagram of the coarse frequency synchronization block.

Fine frequency synchronization block: The algorithm of the fine frequency synchronization is mainly based on [6]. The computation of the timing synchronization can contribute to the estimation of the frequency offset less than one subcarrier frequency spacing. To illustrate this characteristic, Eq. (1) can be expressed as follows:

$$\begin{aligned} F(n) &= \sum_{l=0}^{N_g-1} y^*_{i,l+n-N} \cdot y_{i,l+n}\ ,\quad 0 \le n \le N + N_g, N = 2K\ or\ 8K \\ &= \sum_{l=0}^{N_g-1} \dot{y}^*_{i,l+n-N} \cdot e^{-j\frac{2\pi}{N}(l+n-N)\cdot\hat{\varepsilon}} \cdot \dot{y}_{i,l+n} \cdot e^{+j\frac{2\pi}{N}(l+n)\cdot\hat{\varepsilon}} \\ &= e^{j2\pi\cdot\hat{\varepsilon}} \cdot \sum_{l=0}^{N_g-1} \left|\dot{y}_{i,l+n}\right|^2 \end{aligned} \quad (3)$$

where $\dot{y}_{i,l+n}$ and $\dot{y}_{i,l+n-N}$ are the received signals without frequency offsets, and $\hat{\varepsilon}$ is the decimal frequency offset. Eq. (3) shows that the computation of the time synchronization also reveals the decimal frequency offset. Therefore, we can estimate the decimal frequency offset by the following means:

$$\hat{\varepsilon} = \frac{1}{2\pi} Arg\{F(n)\}_{n=\hat{\Omega}} \tag{4}$$

where the $\hat{\Omega}$ is the estimated timing error. Hence, we can correct the frequency offset in time domain according to the value of $\hat{\varepsilon}$. Fig. 6 shows the block diagram of the fine frequency synchronization, where the cordic phase calculator computes the decimal frequency offset, and the frequency synthesizer synthesizes a sine wave for frequency correction.

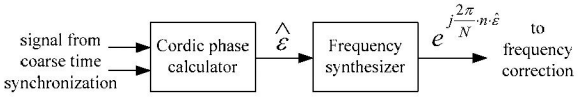

Fig. 6. The block diagram of the fine frequency synchronization block.

2K/8K FFT

A 2K/8K mode small-area FFT processor design [7] is employed in the proposed COFDM demodulator. Since COFDM modulation is based upon the utilization of multiple subcarriers, the decimation-in-frequency (DIF) scheme is adopted instead of the decimation-in-time (DIT) to avoid any transformation between time domain and frequency domain. The DVB-T specification requires that the symbol data rate is 8 MHz. Given such a high data rate, the stage of memory as well as the routing area will be very demanding particularly in the 8K mode (8192 subcarriers). The pipeline structure seems to be an unavoidable option to carry out the high data rate design. Fig. 7 shows the pipeline structure of the 2K mode FFT design. Every block in Fig. 7 is called a butterfly stage.

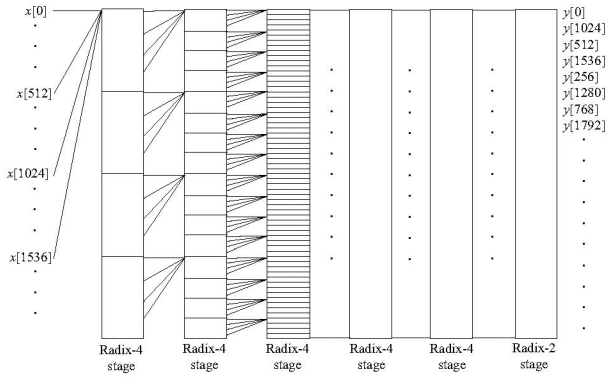

Fig. 7. The pipelined structure of the 2K FFT.

The butterfly stages widely used in prior FFT designs are radix-2, radix-4, radix-*n*, and split-radix. The radix-2 unit is the most popular one owing to its simplicity. However, when the points of the FFT required to be computed increase, radix-4 will possess the edge of less computation complexity [8]. The radix-4 unit used in the FFT is shown in Fig. 8. The temporary storage elements are SRAMs which consume much less area than DFF-based registers, and no self-refreshing dynamic power consumption as the DRAM-based storage cells.

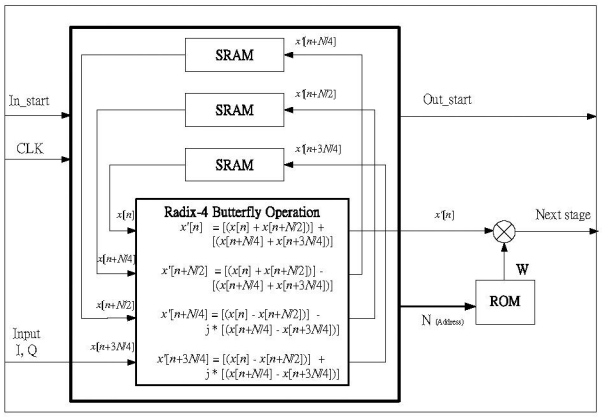

Fig. 8. The schematic of the radix-4 butterfly.

Channel estimation block

The transmission in the terrestrial channel is more hostile than the transmission in the satellite or the cable system. Fading channel, noise, and power lose will degrades the BER of the receiver. Hence, we must estimate the channel impulse response to compensate the subcarriers.

The scattered pilots are inserted into the subcarriers of the transmitted COFDM symbols every 12 subcarriers. The power level of each scattered pilot is 4/3 times of the average power of subcarriers, where the boosted power level lessens the interference caused by the nonideal channel during transmission. Before performing the channel estimation, the average power of the received subcarriers, P_{avg}, should be calculated first. The channel estimation can expressed as follows:

$$H_p \approx \frac{Y_p}{X_p} = \pm \frac{3}{4 \cdot \sqrt{P_{avg}}} Y_p \tag{5}$$

where Y_p are the received scattered pilots, and X_p is the transmitted scattered pilots. Since the scattered pilots are 12 subcarriers apart from each other, the results of the channel estimation, H_p, should be linearly averaged to obtain the channel response of each subcarrier between two scattered pilots. The algorithm used to perform linear averaging is the least square method, and it is implemented by a 23-tap linear interpolation filter.

SIMULATION RESULTS

The proposed COFDM demodulator for DVB-T is implemented by the TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm CMOS technology. The layout of the proposed design is shown in Fig. 9, and the area is about 17.2 mm^2. The proposed design use 36 Kbits ROM and 637 Kbits SRAM. The specification of the proposed design is summarized in Table I. The simulation results shows the proposed design can effectively estimate the timing offset and frequency offset and correct it. Fig. 10 shows the constellation map derived from the output of the proposed prototype under the SNR of 10 dB and frequency offset of 20.3 subcarriers spacing.

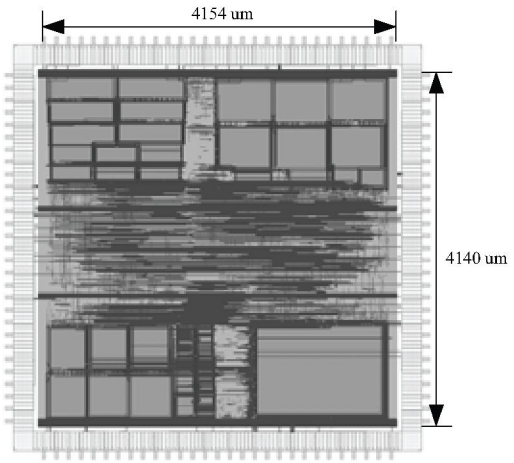

Fig. 9. The layout of the proposed prototype

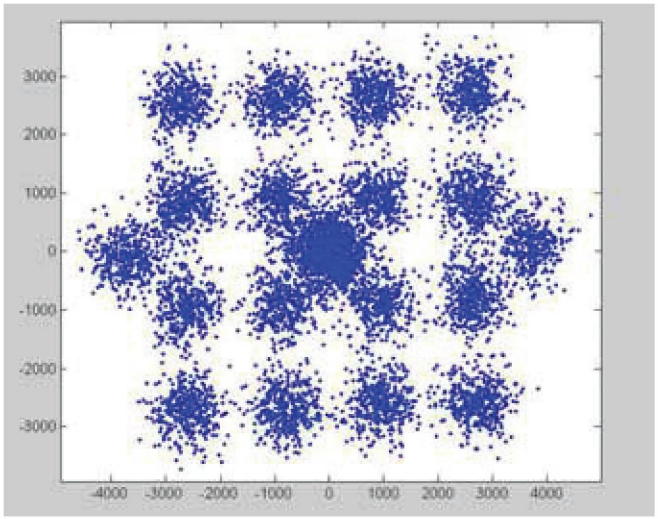

Fig. 10. The constellation map of a COFDM symbol under the SNR of 10 dB and frequency offset of 20.3 subcarriers spacing .

TABLE I
SPECIFICATION OF THE PROPOSED DESIGN

technology	0.18 μm CMOS
power supply	1.8 V
core size	17.2 mm^2
ROM capacity	36 Kbits
SRAM capacity	637 Kbits

CONCLUSION

This paper presents a prototype of COFDM demodulator for European DVB-T standard. The proposed prototype covers the critical parts of the COFDM reception including FFT processing, time synchronization, frequency synchronization, and channel estimation. The algorithms adopted in the proposed design are relatively simple but effective compared to those state-of-the-art technology. Therefore, the proposed design achieves reliable performance without the overhead of the hardware complexity.

REFERENCES

[1] European Telecommunications Standards Institute (ETSI) ETSI 300 744 v1.1.2(1997-08): *Digital Video Broadcasting (DVB); Framing Structure, Channel Coding and Modulation for Digital Terrestrial Television.*

[2] J. H. Stott, "The DVB terrestrial (DVB-T) specification and its implementation in a practical modem,'' *International Broadcasting Convention*, pp. 255-260, Sept. 1996.

[3] M. Massel, *Digital television DVB-T, COFDM, and ATSC 8-VSB*, Digitaltvbooks.Com, 2000.

[4] H. Nogami, and T. Nagashima, "A frequency and timing period acquisition technique for OFDM systems," *1995 IEEE International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC'95),* vol. 3, pp. 1010-1015, Sept. 1995.

[5] D. Lee, and K. Cheun, "A new symbol timing recovery algorithm for OFDM systems," I*EEE Transactions on Consumer Electronics*, vol. 43, no. 3, pp. 767 – 775, Aug. 1997.

[6] J. Echavarri, M. E. Woodward, and S. K. Barton, "A comparison of time and frequency synchronisation algorithms for the European DVB-T system," *1999 IEEE Vehicular Technology Conference (VTC 1999)*, vol. 2, pp. 678 – 682, Sept. 1999.

[7] C.-C. Wang, J.-M. Huang and H.-C. Cheng, "A 2K/8K Mode Small-Area FFT Processor for OFDM Demodulation of DVB-T Receivers," *IEEE Transactions on Consumer Electronics*, vol. 51, no. 1, pp. 28-32, Feb. 2005.

[8] J.-H. Suk, D.-W. Kim, T.-W. Kwon, S.-K. Hyung, and J.-R. Choi, "A 8192 complex point FFT/IFFT for COFDM modulation scheme in DVB-T system," *2003 Inter. SOC (System-on-Chip) Conference*, vol. 5, pp. 131-134, Dec. 2003.