Cost-effective Residue Amplifier Design for Sensorless BLDC Motor Control

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***Abstract*— A low-cost and low-power residue amplifier (RA) used in inverter control of sensorless BLDC (brushless DC) motors is designed and implemented. It is implemented basing on a folded-cascode operational amplifier without using any extra bias circuit or CMFB (common mode feedback) circuit. The RA is aimed at the real-time voltage difference estimation between the neutral voltage and the average of the voltages on the 3 phase windings of the motors. The correctness as well as the performance of the RA seriously affects the success of the sensorless inverter control of the BLDC motors, since the back-EMF (back-electromotive force) estimation method, which detects the commutation moment for rotation control of the brushless DC motors, relies on the accuracy of the RA. The proposed RA is low power and low cost because expensive power consuming Hall sensors are no longer needed in the motor inverter controller. Physical measurement of the RA on silicon has shown the error is less than 3%.**

Keywords : inverter, sensorless, brushless DC motor, residue amplifier, zero-crossing

I. Introduction

Power requirements of large motors in home appliances dictate the overall power consumption of a house, such as, air conditionings, washing machines, refrigerators, and water pumps. The BLDC motors probably are the most widely-used motors in these applications, [1], [2]. The conventional controls of motors are quite simple : either ON or OFF. However, such a simplicity will result in lots of collateral damages, e.g., high power dissipation, large noise, large harmonics, and heat problems. If the motors are driven by inverters, e.g., air conditionings, they are no longer controlled by a simple switch to be turned on or off. On the contrary, the rotation speed and the direction of the motors will be automatically adjusted by certain well-developed algorithms such that the temperature will be kept stably, and the power consumption is reduced. Hence, by adopting inverters, not only is the motor power saved, the noise, harmonics, and heat problems are also expected to be resolved. The development of such a motor inverter controller IC is particularly important to the widely used DC motors in home appliances as shown in Fig. 1. Although advanced microprocessors with higher computing capability and execution speed are used in motor control [9], certain interface ICs are still required in the build-up of control systems [7]. Several problems need to be resolved in such a motor application scenario. First, the reduction or the removal of the noise since the motor usually operates in such an imperfect environment. Second, the rotational direction of the rotor must be determined. Therefore, the RA in charge of detecting the voltage difference of the neutral voltage and the average of the 3 terminal voltages of the motor play a very critical role. Traditional amplifier designs, e.g., [3], [8], are not capable meeting the required low cost and low power performance. We, thus, in this work, propose a novel RA design utilizing two non-overlapping clocks such that high performance and low cost can be achieved. The measurements on silicon justify the fidelity of the proposed RA design.

II. RA Design for BLDC Inverter Control

Fig. 2 reveals the block diagram of a brushless DC (BLDC) motor control system using a sensorless inverter controller, where no Hall sensor will be utilized to detect the position of the rotor. The individual function of major blocks is briefly described as follows.

(1). 8-bit Microcontroller : Although DSPs possess higher speed and precision than the general microprocessor, they suffer from the overhead of area, cost and large power consumption. A 8051-compatible MCU (microcontroller) with a power-saving algorithm based upon the feedback signals from the zero-crossing detector and the ADC (analog-to-digital converter)is used in this work.

(2). PWM Generator : A total of six channels with six groups of registers are needed to generate required voltage waveforms. However, PWM signals applied to the motor control system have an interdependent relationship among the control signals. Then, the output of six signals can be simplified with a single group of registers to save area cost.

(3). Zero-Crossing Detector : Since the proposed system mainly is focused on the applications where the required revolution is less than 4500 rpm (75 rotations per second), the slowest transfer time of 58.0 ns is far more than enough to carry out the zero-crossing detection.

(4). ADC : In order to reduce the power consumption of ADC, we adopt the charge-redistribution successive approximation (SA) architecture is this work.

A. Analysis of prior RA design

It is obvious that RA has to carry out an accurate estimation of the voltage difference between the neutral voltage and the average of the voltages on the three phase windings [6]. In other words, it must estimate the non-excited back-EMF.

$$V_{out} = V_{natural} - \frac{1}{3} \cdot (V_a + V_b + V_c) \tag{1}$$

where $V_{natural}$ is the neutral voltage, V_a, V_b, V_c denotes the terminal voltages of the three phase windings, V_{out} is the output of the OPA.

Although Cheng *et al.* proposed an RA design in [6] basing on a capacitive reset gain amplifier [8], the operational amplifier (OPA) therein drastically affects the overall performance, including speed and noise immunity. For instance, the common-mode voltage, V_{cm}, which is coupled to the minus input of the OPA might be vulnerable to the power supply noise or the vibration of the motor. An additional CMFB (common-mode feedback) circuit and a bandgap bias might be needed to regulate the V_{cm}. What worse is that such an extra feedback loop might introduce an extra low-frequency pole

to deteriorate the speed performance and the DC gain. Meanwhile, the detailed schematic as well as the analysis in the prior works were never studied and explored.

B. Cost-effective RA design

Referring to Fig. 3, the architecture of the proposed RA is revealed. Notably, the minus input of the OPA is permanently ground due to two simple thoughts : Firstly, since the speed of the BLDC motor ($\approx$ KHz) is far less than switching speed of MOS transistors ($\approx$ 100 MHz), the noise in the high-frequency is unlikely to contaminate the low-frequency band of the motors, the CMFB and bandgap bias can be removed without causing any noise problem. What even better is that the poles introduced by the extra feedback loop can be avoided. By a similar thought, the offset voltage compensation biases are no longer needed. Therefore, the overall cost will be drastically reduced. In short, the RA can be modified to be the cost-effective design as shown in Fig. 3.

Another design issue is to reduce the notorious channel charge injection when the MOS-based switches are used in the RA circuit. Besides the required non-overlapping between the clock signals, $clk1$ and $clk2$, the signals, $clk1a$ and $clk2a$ which control switches, S3 and S4, respectively, must lead the corresponding $clk1$ and $clk2$ by a sufficient amount of phase shift. Otherwise, the charge stored in the capacitors will leak such that the terminal voltages drifts.

The entire operation of the RA is summarized as follows.

- **reset phase :** When $clk1a$ and $clk2a$ are both high, switches S1, S3, S5, S6, S7 are turned on while all of the other switches are off. The intrinsic offset voltage of OPA, V_{off}, will be copied to C_{1a}, C_{1b}, and C_{1c}, while $V_{neutral} - V_{off}$ will be copied to C2. The RA is degenerated into the circuit shown in Fig. 4.
- **compute phase :** As soon as both $clk2$ and $clk2a$ are pulled high, switches S2, S8, S9, and S10 are turned on to execute the desired voltage difference estimation. The three terminal voltages, V_a, V_b, V_c, respectively, are coupled to C_{1a}, C_{1b}, and C_{1c}. Meanwhile, the charge in C2 which is stored in the previous phase will be shared with these three capacitors. The RA, thus, is degenerated into the circuit in Fig. 5.

The charge sharing among these 4 capacitors can be derived as follows.

$$\begin{aligned} &\text{C2} \times (V_{neutral} - V_{off}) = Q(\text{C2}) \\ &+(C_{1a} \cdot V_a + C_{1b} \cdot V_b + C_{1c} \cdot V_c) \end{aligned} \tag{2}$$

where $Q(\text{C2})$ denotes the final charge on C2. Notably, since V_{off} can be ignored in the motor applications, the voltage difference estimation can be simplified as the following equation.

$$\begin{aligned} V_{out} &= V_{neutral} - \Big(\frac{C_{1a}}{\text{C2}} \cdot V_a + \frac{C_{1b}}{\text{C2}} \cdot V_b \\ &+ \frac{C_{1c}}{\text{C2}} \cdot V_c\Big) \end{aligned} \tag{3}$$

Thus, we choose C_{1a}=C_{1b}=C_{1c}=$\frac{1}{3}$C2 to further simplify Eqn. (3) into Eqn. (1).

C. Folded-cascode OPA

The fundamental requirements of a motor inverter controller include high noise immunity and fast computational speed. The folded-cascode amplifier [3] is adopted to realize the OPA in Fig. 3 so as to meet the mentioned requirements, because the folded-cascode amplifier possesses high PSRR (power supply rejection ratio) to resist the noise coupled in VDD and GND, and high GBW (gain-bandwidth product). Referring to Fig. 6, NM01 and NM02 constitute a differential input stage. PM04, PM14, PM06 and PM13 consists of two identical current sources. Notably, PM06 and PM07 are cascode transistors which provide additional noise rejection besides the current source function. Two cascode current mirrors providing a wide swing current are composed of NM08, NM09, NM10 and NM11, respectively. After a few derivation steps, the characteristics of the amplifier are found as follows.

$$\begin{aligned} R_o &\approx gm_{\text{NM09}} r_o\text{NM09} r_o\text{NM11} \;||\; \\ &\quad [gm_{\text{PM07}} r_o\text{PM07}(r_o\text{NM02} \;||\; r_o\text{PM05})] \\ A_V &\approx \frac{1}{2} gm_{\text{NM01}} \cdot R_o \\ p_1 &\approx \frac{1}{R_o \cdot C_L} \end{aligned} \tag{4}$$

where C_L denotes the load capacitor, A_V is the DC gain, p_1 is the first-order pole, R_o is the output impedance of the OPA, gm represents the transconductance of the corresponding transistor, and r_o represents the the output impedance of the corresponding transistor looking into the drain.

D. Clock generator

As we mentioned earlier, the computation of the RA heavily replies on the accuracy of the clocks, including non-overlapping $clk1$ and $clk2$, and the phase-leading $clk1a$ and $clk2a$. The clock generator in Fig. 7 is utilized to provide the four clock signals as shown in 8. Notably, the aspect ratios of the transistors in the buffers of the clock generator, buffer1 and buffer2, must be tuned empirically to ensure that the phase shift of $clk1a$ and $clk2a$ leads $clk1$ and $clk2$ by $\frac{1}{10} \cdot 2\pi$.

III. Simulation and Implementation

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed RA. The diephoto of the proposed RA on silicon is shown in Fig. 9, which shows that the area is 1.466$\times$1.466 μm^2 including pads. Let one of V_a, V_b, V_c take turn to be couple to $V_{neutral}$ while the other two terminal voltages are grounded. Fig. 10 shows the waveforms on Agilent Infiium mixed-signal OSC when the chip is under test. The peak-to-peak amplitude of V_{out} is roughly $\frac{2}{3}$ of that of the terminal voltages. It is then proved that the RA realizes the required funciton in Eqn. (1). The overall performance of the proposed design is summarized in Table I.

IV. Conclusion

We have proposed a modified RA design to realize the required voltage difference computation in a motor inverter control system. By removing redundant circuits and using a folded-cascode amplifier design, the RA is proved to be very cost effective. the measurements of the proposed design on silicon justifies the functionality and correctness.

Acknowledgment

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References

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chip area	$1.466 \times 1.466\ \mu m^2$
core area	$0.280 \times 0.203\ \mu m^2$
max. freq.	20.0 MHz (1.0 MHz by measurement)
avg. power	75.9 mW (59.58 mW by measurement)
max. error	$\leq$ 6% ($\leq$ 3% by measurement)

TABLE I

CHARACTERISTICS OF THE PROPOSED RA

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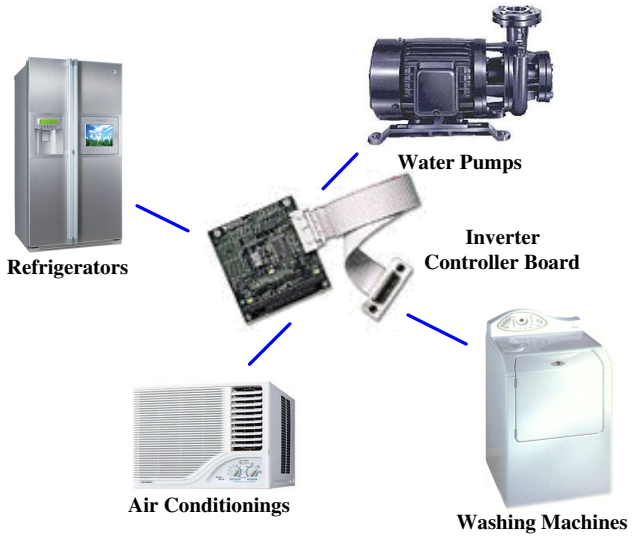

Fig. 1. Home appliances using motors

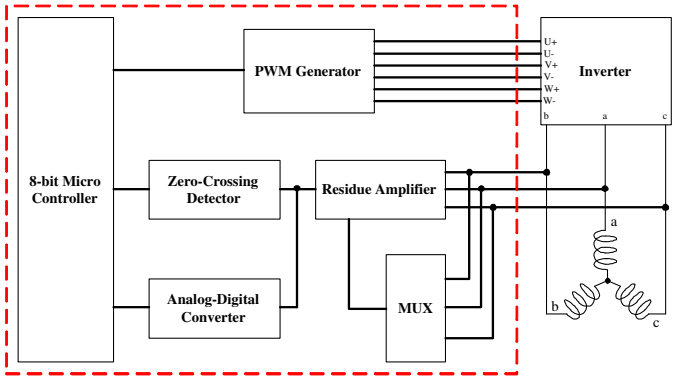

Fig. 2. Block diagram of the inverter controller of BLDC motors

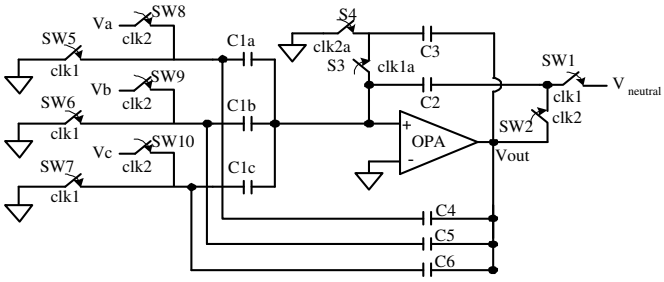

Fig. 3. Cost-effective RA

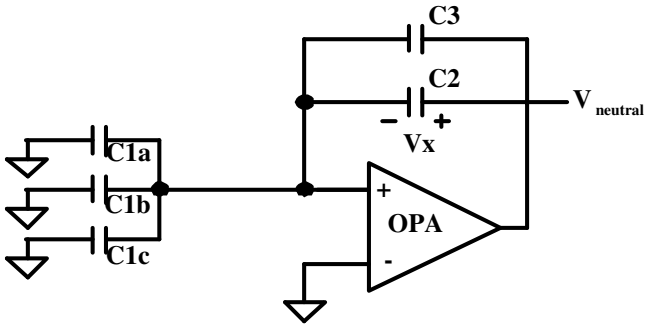

Fig. 4. Reset mode of the RA

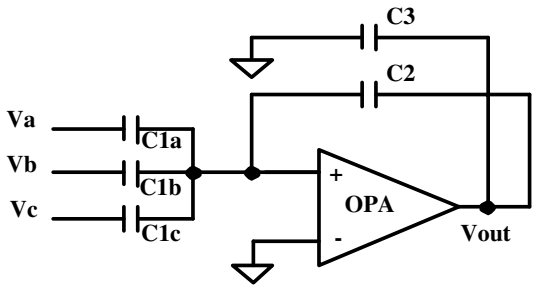

Fig. 5. Compute mode of the RA

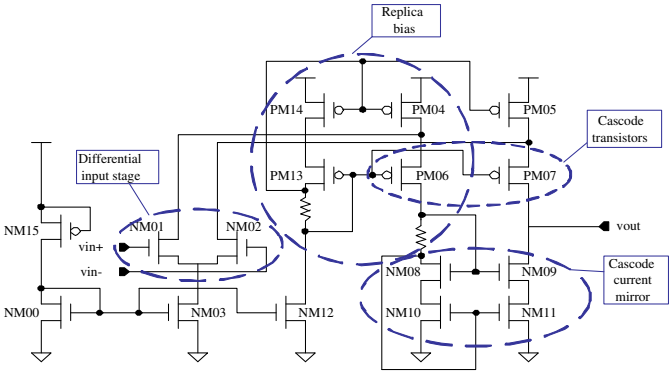

Fig. 6. Folded-cascode OPA in the RA

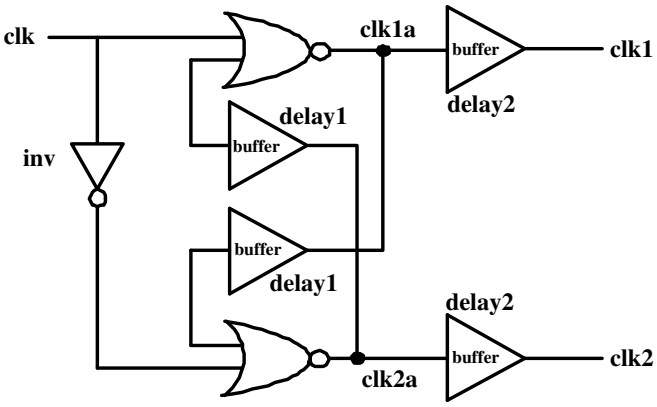

Fig. 7. Clock generator

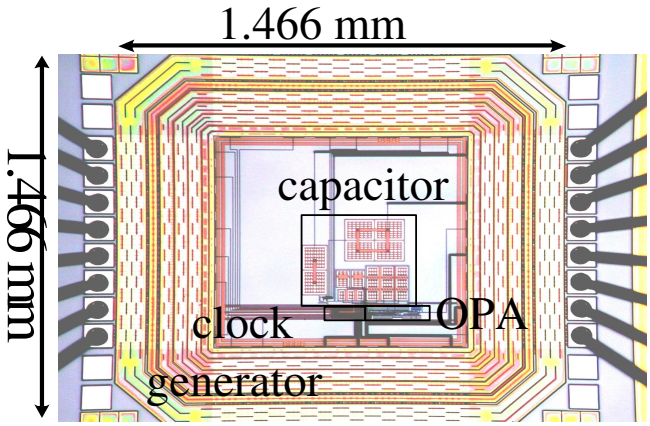

Fig. 9. Diephoto of the cost-effective RA

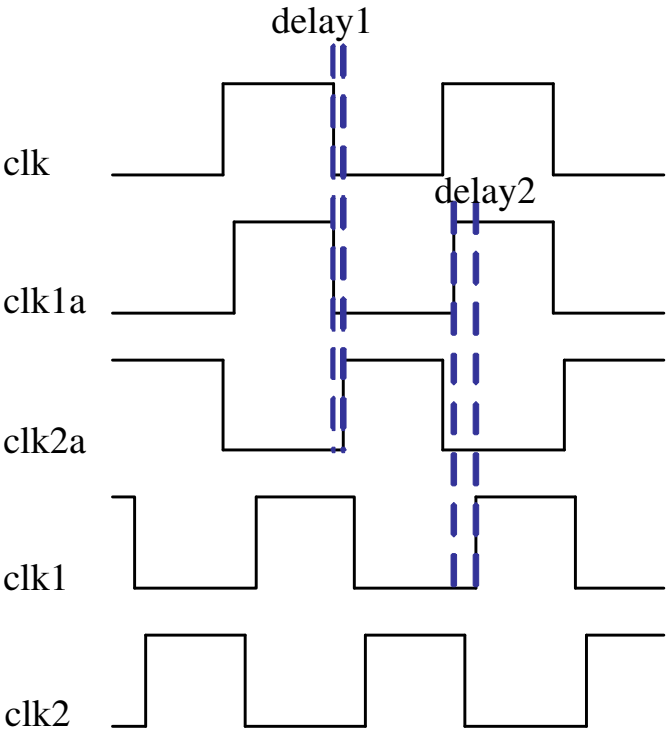

Fig. 8. Nonoverlapping clocks

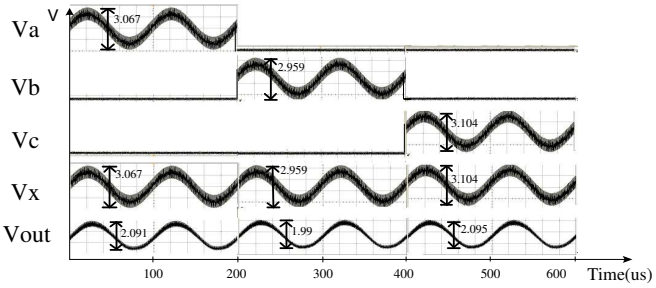

Fig. 10. Measured waveforms

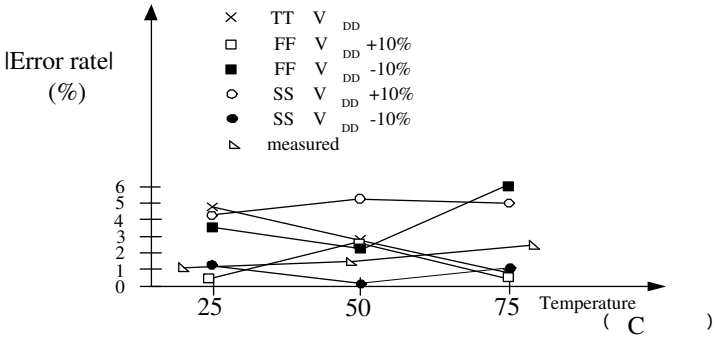

Fig. 11. Measurement of the error percentage