A Linear LDO Regulator with Modified NMCF Frequency Compensation Independent of Off-chip Capacitor and ESR

Chua-Chin Wang, *Senior Member, IEEE*, Chi-Chun Huang, Tzung-Je Lee, and U Fat Chio

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
email : ccwang@ee.nsysu.edu.tw

***Abstract*— This paper presents a novel compensation design for regulators, i.e., modified NMCF (nested Miller compensation with feedforward Gm stage), resulting in a linear LDO (low dropout) regulator whose performance is independent of the off-chip capacitor and its ESR (equivalent series resistor). The proposed compensation method ensures the stability of the feedback loop and the sufficient phase margin of the LDO regulator. Besides, the transient response is fastened. The analysis of the stability is derived to solidify the proposed design. The proposed design is implemented using TSMC 0.35 μm 2P4M CMOS process. The results verify the performance and the stability on silicon. The power supply rejection ratio is 25 dB @[200 Hz, 3 MHz], $[50\Omega,\ 500\Omega]$ provided that the input voltage varies from 4 V to 5 V.**

***Keywords*—LDO regulator, modified NMCF, frequency compensation, ESR**

I. Introduction

The LDO (low-dropout) regulator is generally utilized to translate a voltage level or provide a stable output voltage, which has been considered as one of the important components for the power management of wireless applications, e.g., cellular phones, hand-held computers, and particularly implanted wireless biomedical chips [1]. Traditional linear LDO regulators usually consist of a two-stage error amplifier, a power output stage and a negative feedback loop. However, since the stability and accuracy of the regulated output voltage is the most critical factor in many field applications such as biomedical chips, traditional designs suffer from poor efficiency as the difference between the input and output voltages is increased [5]. In order to attain a fast transient response and an accurate output voltage, several prior LDO regulators were proposed to use high gain amplifiers with a cascade or cascode technology. It results in the stability problem due to the appearance of inherent three poles. Besides, the varying load current also affects the stability [2], [3]. Thus, a frequency compensation technique to ensure the stability of the LDO regulator was proposed to resolve this problem [2], [3], [4]. Otherwise, the circuitry will become unstable due to the inherent three poles if there is no any compensation mechanism. What worse is that the equivalent loading impedance of the LDO regulator might not be a constant. It leads to the output pole drifting. Thus, the loop stability of the LDO regulator is uncertain. An off-chip capacitor C_{off}, as shown in Fig. 1, was proposed to maintain the stability of the LDO regulator in several research works, [5], [6], [7]. The off-chip capacitor and its ESR (equivalent series resistor) are designed to move the zero to achieve a pole-zero cancellation and keep the phase margin larger than zero degree. However, the off-chip capacitor increases the area of printed-circuit board and the value of the ESR might drift owing to the variation of the temperature and different materials. Therefore, the off-chip capacitor scheme is also not acceptable. In this work, a new compensation method independent of the off-chip capacitor and its ESR is presented to enhance the LDO regulator's performance regarding the transient response and the noise rejection.

II. LDO Regulator Using NMCF

A traditional LDO regulator is shown in Fig. 1, where a bandgap bias circuit generates a PVT-independent reference voltage V_{ref} . The series resistors, R_{cf1}, R_{cf2}, monitor the output voltage by a simple voltage division. A feedback voltage V_{fb} is fed back to be compared with V_{ref} by the error amplifier. The error amplifier then feeds a control voltage into the pass transistor M_{cpass} to regulate the output voltage according to the difference between V_{ref} and V_{fb}. The faster speed of the feedback loop comes along with the more stable output voltage. Therefore, a large gain is required to ensure that the feedback loop keeps stable. Hence, the frequency compensation becomes a critical issue in the LDO regulator design. However, there is a trade-off between the loop gain and the bandwidth of the circuit.

A. Modified NMCF compensation

The structure of the proposed LDO regulator is shown in Fig. 2. It is composed of the two cascaded error amplifiers, A_{op1}, A_{op2}, a pass transistor, M_{pass}, series resistors, R_{f1}, R_{f2}, two compensation capacitors, C_{m1}, C_{m2}, and a feed-forward transconductance amplifier stage, A_{opf}. What we propose is to insert a feed forward Gm boosting amplifier between the output of the first error amplifier and the resistor-based voltage divider. Meanwhile, two compensation capacitors are added on the source and the drain of the pass element to mimic the Miller capacitor compensation. It is then called the modified NMCF (nested Miller compensation with feedforward Gm stage) design.

In order to simplify the analysis of the frequency compensation, we assume that g_{mi}, R_{oi} are the transconductance and the output impedance of the amplifier A_{opi}, respectively, where $i = 1, 2$, or f. g_{mp} and R_{op} denote the transconductance and the output impedance of the transistor M_{pass}, respectively. Besides, we assume that the gain of each amplifier is much larger than the unit gain. The load capacitor, C_L, and the compensation capacitors are much larger than parasitic capacitors which could be neglected.

Based on these assumptions, the open loop transfer function is given by

$$\begin{aligned} T(s) &= \frac{V_{fb}(s)}{V_{fin}(s)} = \frac{TDC \cdot Zero(s)}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})(1+\frac{s}{p_3})}, \\ TDC &= (g_{m1}g_{m2}g_{mp}R_{o1}R_{o2})(\frac{R_{op}R_L}{R_{op}+R_L}) \\ &\quad \cdot(\frac{R_{f2}}{R_{f1}+R_{f2}}), \\ p_1 &= \frac{R_{op}+R_L}{C_{m1}g_{m2}g_{mp}R_{o1}R_{o2}R_{op}R_L}, \\ p_2 &= \frac{1}{R_{o2}C_{m2}}, \\ p_3 &= \frac{R_{op}+R_L}{R_{op}R_L C_L}, \\ Zero(s) &= 1 + (\frac{g_{mf}C_{m2}}{g_{m2}g_{mp}})s - (\frac{C_{m1}C_{m2}}{g_{m2}g_{mp}})s^2, \end{aligned} \quad (1)$$

where TDC is the DC loop gain, and p_1 is the dominant pole.
According to Eqn. (1), the LHP zero is found be as follows,

$$z_1 = -\frac{g_{mf}}{2C_{m1}}(\sqrt{1+4\frac{C_{m1}}{C_{m2}}\frac{g_{m2}g_{mp}}{g_{mf}}}+1). \quad (2)$$

By contrast, the RHP zero is also derived to be

$$z_2 = \frac{g_{mf}}{2C_{m1}}(\sqrt{1+4\frac{C_{m1}}{C_{m2}}\frac{g_{m2}g_{mp}}{g_{mf}}}-1). \quad (3)$$

The LHP zero should be located after p_2, p_3 for the stability purpose [4]. Thus, the following condition must be held, given $C_{m1} \ll C_{m2}$, and $R_{op} \ll R_L$: $g_{mf} \geq \frac{C_{m1}}{R_{op}C_L}$, $g_{mf} \geq \frac{C_{m1}}{R_{o2}C_{m2}}$.

By setting p_2 and p_3 larger than the required GBW (gain-bandwidth product), the GBW is then found to be

$$GBW = \frac{g_{m1}}{C_{m1}}. \quad (4)$$

The phase margin (PM) is also derived to be

$$PM \approx 60^o + tan^{-1}(\frac{GBW}{z_1}) - tan^{-1}(\frac{GBW}{|z_2|}) > 60^o. \quad (5)$$

As we know, if the phase margin of a loop greater than 60 degrees, the time domain response of this loop will get rid of ringing [8]. In short, a stable LDO regulator independent of the ESR can be attained by tuning g_{mf}, C_{m1}(=0.1 pF) and C_{m2}(=30 pF) despite that the load capacitor C_L varies.

B. Circuit Design

The schematic of the proposed design is shown in Fig. 3. R_1, R_2, R_3, Q_1, Q_2, and A_{opb} act as the bandgap bias circuitry. The reference voltage is easily derived as

$$V_{ref} = V_{EB1}(\frac{R_2}{R_3})V_t \ln(\frac{R_2 A_{Q2}}{R_1 A_{Q1}}), \quad (6)$$

where A_{Q1} and A_{Q2} are the emitter area of Q_1 and Q_2, respectively. M_{p11} - M_{p13}, M_{n11}, and M_{n12} constitute the first stage of the error amplifier, A_{op1}, while M_{p15}, M_{p16}, M_{n15}, and M_{n16} are the second stage, A_{op2}. R_{f1} and R_{f2} are the feedback series resistors. C_{m1} and C_{m2} are the compensation capacitors. M_f is the feedforward transconductance stage, i.e., A_{opf}, which generates a negative small signal to cancel the feedforward current passing through C_{m1} at high frequency. M_{p14}, M_{n13}, and M_{n14} are in charge of gm-boosting for the loop.

The pass transistor plays a critical role in the design of the LDO regulator. There are five types of pass transistors made up with different transistors to be chosen : Darlington pairs, NPN, PNP, NMOS, and PMOS. The first three components are bipolar junction transistors which could provide a large output current, but produce larger power consumption due to the small base current. Additionally, the dropout voltage is another important factor when it comes to the selection of the pass transistor. Since NMOS needs its gate voltage higher than its source voltage to get into the saturation region, the dropout voltage is high if it is used as the pass transistor. Therefore, PMOS is selected in the proposed design.

III. Simulation and Implementation

We select the value of C_{m1} and C_{m2} to be equal to 0.1 pF and 30 pF, respectively, basing on the analysis of Eqn. (1). Fig. 4 shows that the proposed design is stable in the temperature range [0^{o}C, 75^{o}C]. The PSRR (power supply rejection ratio) results given different C_L and R_L are shown in Fig. 5, and Fig. 6, respectively. Fig. 7 shows the overall PSRR given different temperatures. In short, the PSRR is 25 dB @[200 Hz, 3 MHz], [50Ω, 500Ω] provided that the input voltage varies from 4 to 5V. TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed design. The die photo of the proposed LDO regulator is shown in Fig. 8 and the chip area is 870 μm × 520 μm. Fig. 9 shows the regulated output voltage V_{dd_out} vs. the input voltage V_{dd_in} in different chips. Referring to Fig. 9, all V_{dd_out} value of these chips varies from 3.0 V to 3.6V given V_{dd_in} from 3.7 V to 5.2 V except chip 5. It is good enough to be used in RF-power-transferred. A performance comparison of the proposed design with several prior LDOs is summarized in Table I. Our design provides the least dropout voltage, the maximum operation frequency without using any off-chip capacitor.

IV. Conclusion

We have proposed a LDO regulator with a modified NMCF compensation design. Its outstanding performance is independent of the off-chip capacitor and its ESR. The detailed compensation analysis of the proposed design is also revealed to illustrate the methodology. The simulation and measurement results justify that the supply ripple rejection is independent of the load resistor in the range from 50 Ω to 500 Ω. Moreover, the PSRR keeps 25 dB even if the operating frequency is up to 3 MHz.

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References

[1] T. Akin, K. Najafi, and R. M. Bradley, "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," *1998 IEEE J. of Solid-State Circuits*, vol. 33, no. 1, pp. 109-118, Jan. 1998.

[2] K. C. Kwok and P. K. T. Mok, "Pole-zero tracking frequency compensation for low dropout regulator," *2002 IEEE Inter. Symp. on Circuits and Systems (ISCAS'02)*, vol. 4, pp. 735-738, May 2002.

[3] K. N. Leung, P. K. T. Mok, and W. H. Ki, "A novel frequency compensation technique for low-voltage low-dropout regulator," *1999 Inter. Symp. on Circuits and Systems (ISCAS'98)*, vol. 5, pp. 102-105, May 1998.

[4] K. N. Leung, and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Transactions on Circuits and Systems*, vol. 8, no. 9, pp. 1041-1056, Sep. 2001.

[5] T. J. Barber Jr., S. Ho, and P. Ferguson Jr., "Multi-mode CMOS low dropout voltage regulator for GSM handsets," *Symposium on VLSI Circuits Digest of Technical Papers, 2002*, pp. 284-287, June 2002.

[6] G. W. den Besten, and B. Nauta, "Embedded 5 V-to-3.3 V voltage regulator for supplying digital IC's in 3.3 V CMOS technology," *IEEE J. of Solid-State Circuits*, pp. 956-962, July. 1998.

[7] C. Stanescu, "Buffer stage foe fast response LDO," *2003 International Semiconductor Conference*, vol. 2, pp. 357-360, Sep. 2003.

[8] P. E. Allen, and D. R. Holberg, "CMOS Analog Circuit Design ," New York: Oxford, pp. 254-255, 2002.

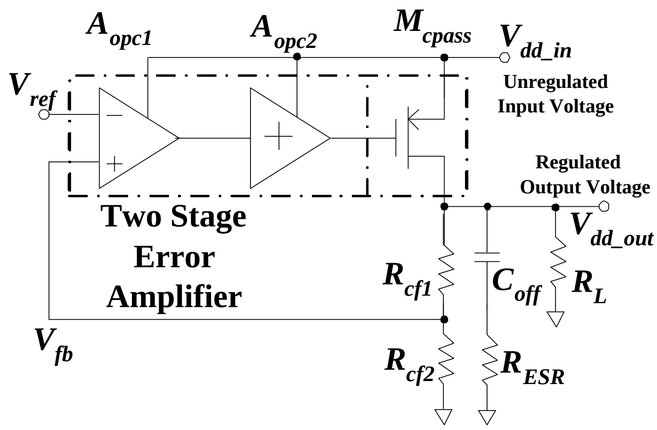

Fig. 1. The classical LDO regulator with the off-chip capacitor.

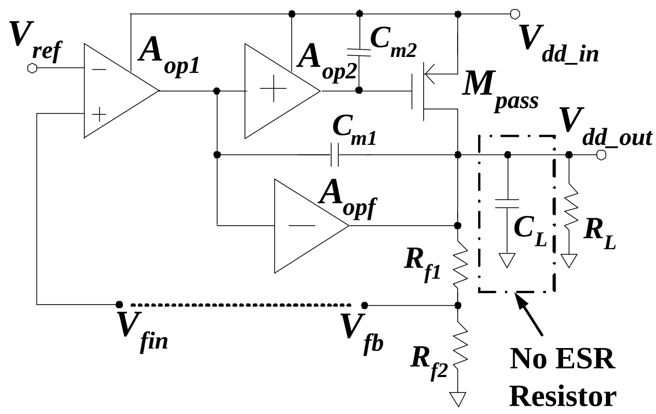

Fig. 2. The structure of the proposed LDO regulator.

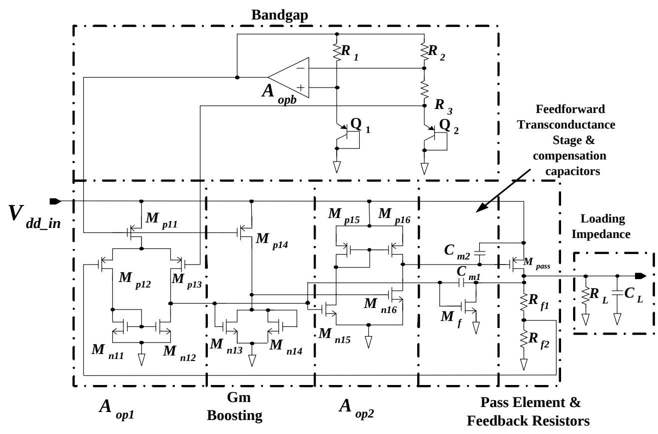

Fig. 3. The schematic of the proposed LDO regulator.

	[5]	[6]	ours
PSRR	54 dB	38 dB	25 dB
CMOS process	0.25 μm	0.5μm	0.35 μm
chip area (mm^2)	0.21	1	0.45
max. freq.	N/A	3 KHz	3 MHz
max. O/P power	720 mW	990 mW	360 mW
V_{dd_in} ripple	N/A	N/A	1 V
dropout voltage	0.5 V	0.3 V	0.3 V
$C_{\text{off-chip}}$ needed	Yes	Yes	No
Applications	battery-operated	DC-voltage-transferred	RF-power-transferred

TABLE I

PERFORMANCE COMPARISON OF LDO REGULATORS.

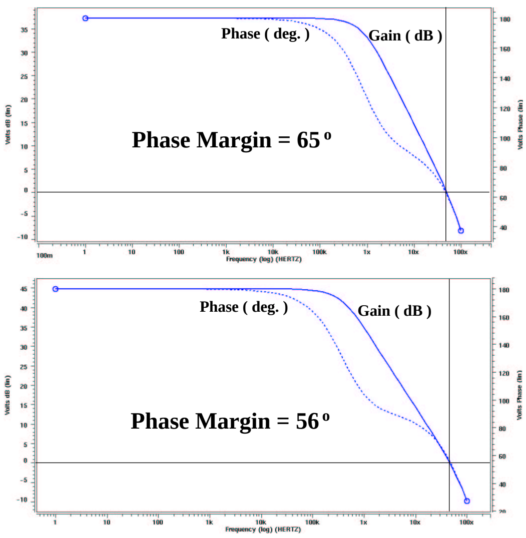

Fig. 4. Loop gain and loop phase at 0^{o}C and 75^{o}C.

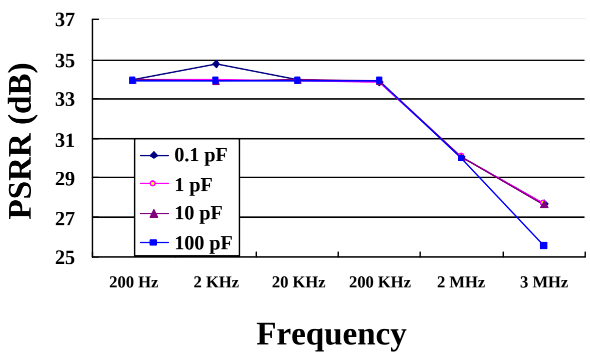

Fig. 5. PSRR of the proposed LDO regulator at different C_L (R_L = 100Ω).

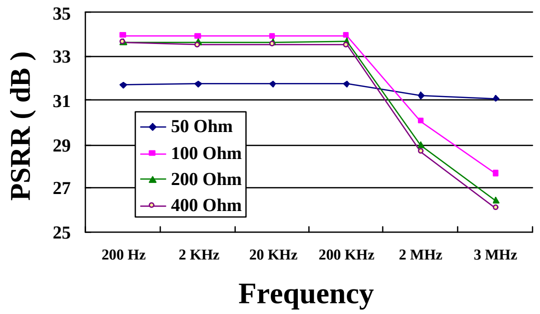

Fig. 6. PSRR of the proposed LDO regulator at different R_L (C_L=10 pF).

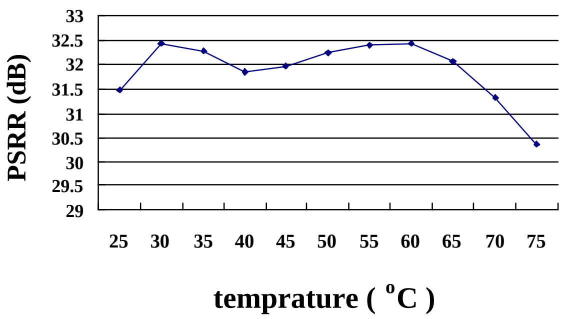

Fig. 7. PSRR of the proposed LDO regulator at [25^{o}C, 75^{o}C] (R_L = 100Ω, C_L=10 pF).

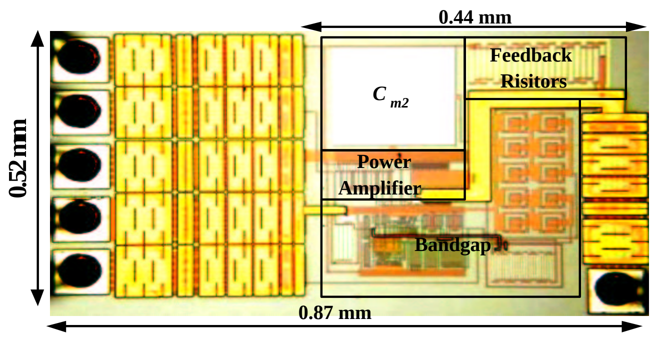

Fig. 8. Die photo of the proposed LSO Regulator.

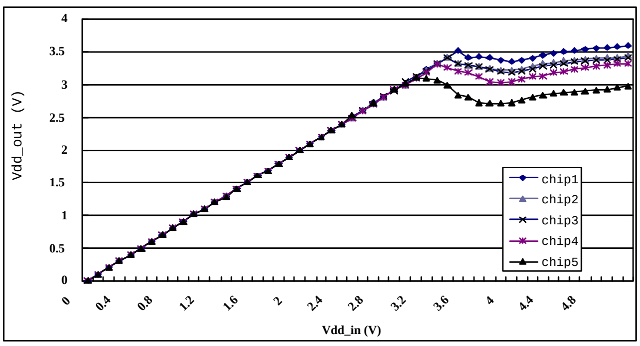

Fig. 9. Output voltage vs. input voltage at different chips.