# DVB-T Receiver With a Fully Digital I/Q Separator*

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***Abstract* -- This paper describes the design of a digital I/Q separator which is applied to DVB-T receivers. The proposed I/Q separator not only avoids problems caused by analog I/Q separators, e.g., gain error, phase error, DC offset, etc., it also resolves the difficulties of prior digital I/Q separators, e.g., large area, large gate count, and high power consumption by insertion of decimation filters. A prototypical system as well as a chip has been designed using 0.18-μm single-poly six-metal CMOS process with core area of 1.59 mm$^2$. The total power consumption is merely 433 μW at a 20.0 MHz system clock.**

**Key word: demodulation, I/Q separator, decimation filter, DVB-T, wireless network**

## I. INTRODUCTION

I/Q separator plays a very important role in most of the demodulators for wireless communication systems. The traditional analog quadrature demodulator with analog-to-digital converters (ADCs) is illustrated in Fig. 1. The intermediate frequency (IF) input signal, s(t), is mixed with the local oscillator (LO) and a 90 degree delayed signal of the same frequency. Two orthogonal channels known as the in-phase (I) channel and the quadrature-phase (Q) channel are generated. Several problems in which a traditional analog I/Q separator have been recognized, e.g., gain error, phase error [4], and DC offset [1]. By contrast, fully digital I/Q separators like Hilbert transform [2], band-pass signal [2] and decimation filter [2], can dodge these problems but pay the expense of large area, large gate count, and high power consumption.

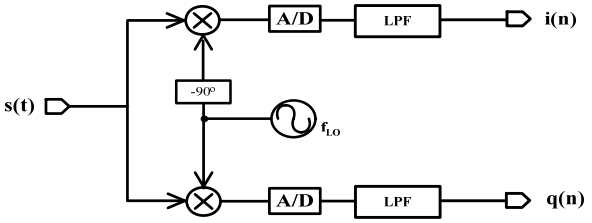


**Fig. 1. Conventional analog I/Q separator**

## II. FULLY DIGITAL I/Q SEPARATOR DESIGN

Fig. 2 shows a traditional digital I/Q separator. The basic component has an ADC, an LO, two multipliers, and two low-pass filters (LPF). We will transform such an architecture into a fully digital I/Q separator through detailed analysis both in time domain and frequency domain.

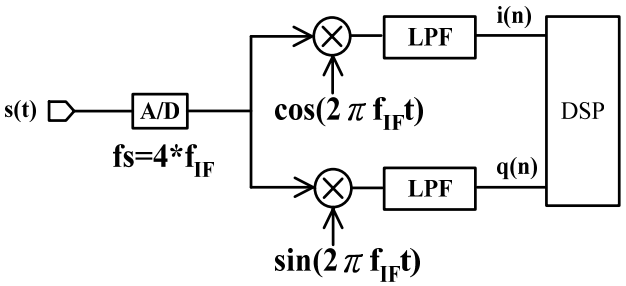


**Fig. 2. Traditional digital I/Q separator**

### A. Local Oscillator

The local oscillator (LO) frequency is set to be 1/4 of the ADC conversion frequency. Fig. 3 shows that the mixing in I channel between the output of the ADC and the LO is simplified to be a multiplication with a sequence of +1, 0, -1, 0... . By contrast, the mixing in Q channel becomes a multiplication with a sequence of 0, -1, 0, +1… . The LO signal generation is now degenerated to be a trivial digital operation, while the multipliers implementing the mixers in Fig. 2 are reduced to a circuit that simply passes, nullifies or reverses the sign of the data. For instance, at t = 0, the input signal is multiplied by +1 in the I channel and 0 in the Q channel. At t=T/4, the input signal is multiplied by +1 in the Q channel and 0 in the I channel, meaning that this sample is fed directly to the Q channel. At t = T/2, the signal is multiplied by -1 and fed to the I channel. Last at t = 3T/4, the signal is inverted and fed to the Q channel. This sequence is constantly repeated to produce the continuous I and Q streams.

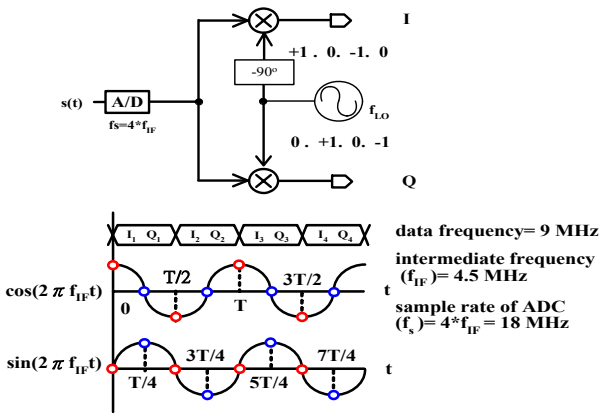


**Fig. 3. LO simplification**

In short, the sequence after the proper inversion and

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shuffling becomes the following stream.

$$I_1, Q_1, -I_2, -Q_2, I_3, Q_3, -I_4, -Q_4... \quad (1)$$

## B. Decimation Filter

In prior digital I/Q separators as shown in Fig. 2, a decimation filter which serves as the LPF is required. After system simulations, it is found a 41-tap LPF is needed for DVB-T receivers to subside the ripples. Assume $h_0$, $h_1$…, $h_{40}$ are the coefficient of the filter. Top of Fig. 4 shows that only $h_0$, $h_2$, $h_4$…, $h_{2n}$, for all n = 1…, 20, are needed in the computation of I channel. By contrast, the bottom of Fig. 4 shows the same for Q channel. In short, the LPF needs only the even-numbered terms (coefficients).

I channel

| period | | |
|---|---|---|
| 0 | $h_0(I_0)$ | keep |
| T/4 | $h_0(0)+h_1(I_0)$ | delete |
| T/2 | $h_0(I_1)+h_1(0)+h_2(I_0)$ | keep |
| 3T/4 | $h_0(0)+h_1(I_2)+h_2(0)+h_3(I_0)$ | delete |
| T | $h_0(I_2)+h_1(0)+h_2(I_1)+h_3(0)+h_4(I_0)$ | keep |

Q channel

| period | | |
|---|---|---|
| 0 | $h_0(0)$ | delete |
| T/4 | $h_0(Q_0)+h_1(0)$ | keep |
| T/2 | $h_0(0)+h_1(Q_0)+h_2(0)$ | delete |
| 3T/4 | $h_0(Q_1)+h_1(0)+h_2(Q_0)+h_3(0)$ | keep |
| T | $h_0(0)+h_1(Q_1)+h_2(0)+h_3(Q_0)+h_4(0)$ | delete |

**Fig. 4. The operation of decimation filter**

Fig. 5 shows the impulse response of the decimation filter with 41-tap, where only $h_{20}$ is 0.5, the rest of coefficients are 0. Therefore, the coefficients of decimation filter can be simplified to a divided-by-2 operation to carry out the coefficient, 0.5. In summary, the correct stream of I and Q can be generated after the outputs of the mixers are multiplied with 0.5. Thus, the complicated digital I/Q separator in Fig. 2 can be simplified to be the I/Q separator in Fig. 6. The multiplier, LPF, a phase shifter, and an LO are no longer needed to reduce area as well as power.

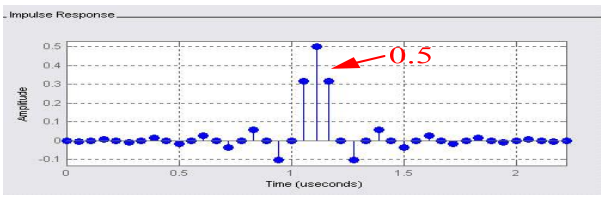


**Fig. 5. Impulse response of decimation with 41-tap**

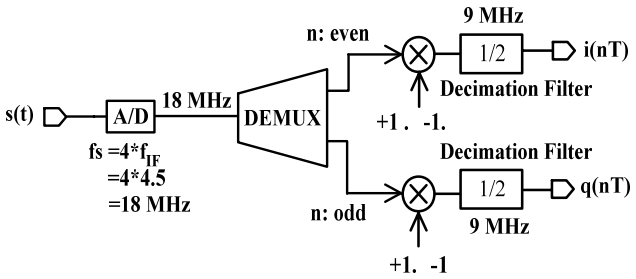


**Fig. 6. Structure of the proposed**

## III. Implementation and Simulation Result

The proposed design is carried out by FPGA and TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm single-poly six-metal CMOS technology. The specifications of the proposed design is summarized in Table 1. Table 2 shows the comparison between a prior work and the our design.

TABLE I
SPECIFICATIONS OF THE PROPOSED DIGITAL I/Q SEPARATOR

| | |
|---|---|
| Technology | **0.18-μm CMOS Process** |
| Power supply | 1.8 V |
| Clock frequency | 20 MHz |
| Core size | 336.68×374.24 $\mu m^2$ |
| Power consumption @ 20MHz | 433 μW |

TABLE II
COMPARISON BETWEEN THE PRIOR SCHEME AND THE PROPOSED

| Design | Die size | Power supply | Power consumption | Technology |
|---|---|---|---|---|
| Ours | 1.24× 1.28$mm^2$ | 1.8 V | 433 μW | TSMC 0.18 um 1p6m |
| [3] | 4.7× 7.7$mm^2$ | 5V | 1.5 mW | 1.2 um CMOS |


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