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A Low-Power 2.45 GHz ZigBee Transceiver for Wearable Personal Medical Devices in WPAN

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Abstract – This paper presents the architecture as well as the circuit implementation of a ZigBee transceiver using 2.45 GHz band, which is compliant with the physical layer of IEEE 802.15.4 standard. A prototypical system and chip has been designed using 0.18- μm CMOS process with core area of 0.16 mm². The simulation results shows the packet error rate is less than 1% given $E_b/N_0 = 9$ dB. The total power consumption is merely 271 μW at a 8.0 MHz system clock.

Index Terms — WPAN, ZigBee, matched filter, direct sequence spread spectrum, wireless network

I. INTRODUCTION

ZigBee is a wireless standard aiming at a low data rate, low cost, and low power wireless data transmission. The physical (PHY) layer and media access control (MAC) layer of ZigBee follow the IEEE 802.15.4 wireless personal area network (WPAN) standard [1]. The standard specifies that a compliant system shall operate in three license-free bands: 2.45 GHz, 868 MHz for North America, and 915 MHz for Europe, where the 2.45 GHz ZigBee possesses the highest transmission bit rate owing to that the O-QPSK (offset-quadrature phase shift keying) modulation is employed. The expected bit rate is 250 Kbps (62.5 Ksymbols/s) which are sufficient for conveying security information or personal medical monitoring usage, [2], [3]. ZigBee is designed to spend most of time dozing. The major applications of ZigBee are focused on sensor and automatic control, such as personal medical assistance, industrial control, home automation, and remote control and monitoring. It is particularly suitable to construct a wireless personal area network for medical assistance as shown in the scenario in Fig. 1.

II. ZIGBEE RECEIVER FOR 2.45 GHz BAND

Fig. 2 depicts the structure of the ZigBee physical layer protocol data unit (PPDU) packet. The preamble field containing 32 bits "0" is for the packet detection and the synchronization in the receiver. The start of frame delimiter (SFD) field denotes the start of the packet data, which is "11100101". The frame length field indicates the number of

octets of the physical layer service data unit (PSDU). The PSDU conveys the payload of the packet.

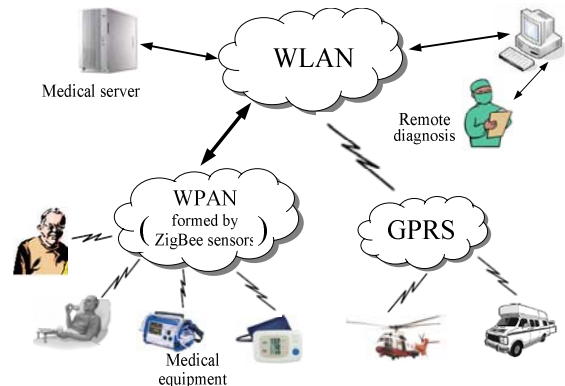


Fig. 1. Application of using ZigBee in personal medical assistance

Octets: 4	1	1	variable
Preamble	Start of frame delimiter	Frame length (7 bits)	Reserved (1 bit)
Synchronization header		PHY header	
			PHY payload

Fig. 2. PPDU packet format

Fig. 3 shows the block diagram of the proposed ZigBee transceiver. The RF signal is down-converted to baseband by the RF receiver (Rx) and quantized by the analog-to-digital converters (ADC). These digital signals are sent to the MAC after the digital demodulation performed by the proposed Rx. The PSDU from MAC is modulated by the proposed transmitter (Tx), and the resultant PPDU packet is transmitted by the RF Tx. The details of each block are described in the following text.

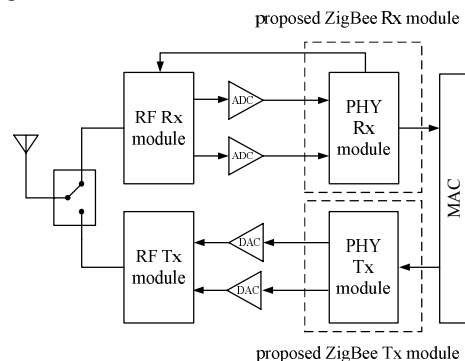


Fig. 3. Block diagram of the ZigBee transceiver for 2.45 GHz band

A. Proposed ZigBee Tx

The proposed ZigBee Tx in Fig. 4 is based on [1]. The

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PPDU packet is composed of the PSDU from MAC and the header added by the header insertion stage. Every 4 bits are mapped into one data symbol. The symbol-to-chip stage performs the direct-sequence spread spectrum (DSSS), where each symbol is mapped into a 32-chip pseudo-random noise (PN) sequence. Notably, the O-QPSK modulation is adopted in 2.45 GHz mode. The fundamental O-QPSK method is to sum the *in-phase signal* with quadrature phase signal delayed by half a cycle in order to avoid the sudden phase shift change.

Then, the modulated O-QPSK signal goes along with the pulse shaping stage to reduce the inter-symbol interference (ISI). Each baseband chip is represented as a half-sine pulse shape. The resultant signal is transmitted by the RF transmitter.

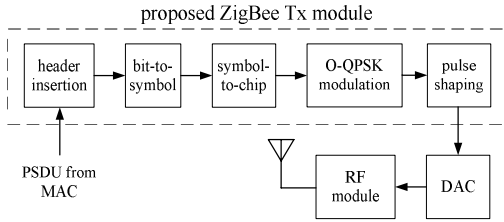


Fig. 4. Detailed block diagram of the proposed ZigBee Tx

B. Proposed ZigBee Rx

Fig. 5 shows the block diagram of the ZigBee Rx. The Packet Detector discriminates whether the incoming signal is data or noise. It enables the following stage if the incoming signal is determined to be data. Each 32-chip PN sequence is sampled to be 128 samples by the ADC. The Phase Difference Detector is in charge of finding the phase difference of each sample. The Downsampling stage finds the maximum phase difference and performs the downsampling. The Frequency Offset Compensation block computes the frequency offset and compensates the offset. The Noncoherent Demodulator stage utilizes the minimum shift keying (MSK) scheme to perform the demodulation process. The reason is that MSK is a special case of O-QPSK with sinusoidal symbol weighting, which can be noncoherently detected [4]. Hence, the proposed Rx adopts the MSK demodulation to implement a noncoherent receiver which possesses lower hardware complexity. The Preamble Removal stage acquires the preamble and removes it from PPDU packet. The Despreading stage despreads each 32-chip PN sequence to 4-bit symbols. The Confirm SFD stage acquires the length of the PSDU and notifies the MAC layer of receiving the PSDU from the receiver.

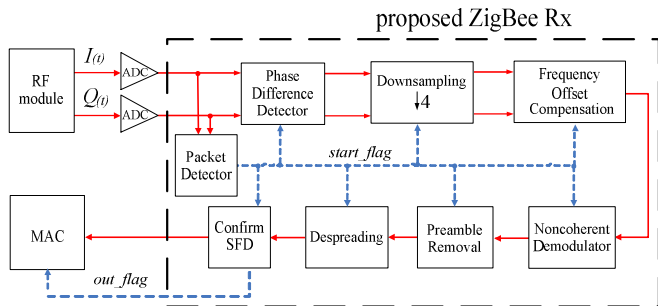


Fig. 5. Detailed block diagram of the proposed ZigBee Rx

In order to provide sufficient samples for phase error estimation in the receiver, the sampling rate of the ADC is set to be four times the frequency of the input signals. Hence, the sampling rate of the ADC is 8 MS/s. The requirement of the ADC resolution can be derived from the system simulation. According to [1], the packet error rate (PER) should be less than 1% when the E_b/N_0 is over 9 dB. 4-bit resolution for ADCs is sufficient to meet the requirement according to the system simulations. In summary, the ADCs are determined to be 4-bit, 8 MS/s ADCs.

III. IMPLEMENTATION AND SIMULATION RESULT

The proposed design is carried out on FPGA and then by 0.18 μm CMOS technology. All of the process corners : $[0^\circ\text{C}, +100^\circ\text{C}]$, and (SS, TT, FF) models, are simulated. Table I summarizes the overall characteristics. The comparison between the proposed ZigBee transceiver and a commercial product is summarized in Table II.

TABLE I
SPECIFICATIONS OF THE PROPOSED ZIGBEE TRANSCIVER

SPECIFICATIONS OF THE PROPOSED ZIGBEE TRANSCIVER	
Technology	0.18-μm CMOS Process
Power supply	1.8 V \pm 10 %
Clock rate	8 MHz
Core size	0.39 mm ²
Power consumption @ 8 MHz	Tx: 128 μW Rx: 143 μW

TABLE II
COMPARISON BETWEEN THE COMMERCIAL PRODUCT AND THE PROPOSED PROTOTYPE

Design	Mode	Power supply	Tx power	Rx power
Ours	2.45 GHz	1.8 V	128 μW	143 μW
Freescall-MC13192	2.45 GHz	2.7V	81 mW*	100mW*

(*Note: The power consumption contains the power of RF module and mixed-signal module.)

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