A High-Efficiency DC-DC Buck Converter for Sub-3×VDD Power Supply[§]

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***Abstract*— This paper presents a DC-DC step-down converter, which can accommodate the range of input voltage from VDD to sub-3×VDD voltage. By utilizing stacked power MOSFETs, a voltage level converter, a detector and a controller, the proposed design is realized by a typical 1P6M 0.18 μm CMOS process without using any high voltage process to resolve gate-oxide reliability and leakage current problems. The core area is less than 0.184 mm^2, while the VDD range is up to 5 V. Since the internal reference voltage is 1.0 V, it can increase the output regulation range. The proposed design attains very high conversion efficiency to prolong the life time of battery-based power supply. Therefore, it can be integrated in a system chip to provide multiple supply voltage sources.**

***Keywords*—DC-DC, step-down converter, sub-3×VDD, gate-oxide reliability.**

I. Introduction

Thanks to the fast evolution of semiconductor technology, the size of transistors are downsized constantly and rapidly. The operation voltage of transistors is dropped from 5 V to 3.3, 1.8 V, or even less. Nevertheless, the operation voltage of prior or existing systems might be still 12 V or 5 V, particulary car electronics. Therefore, we need a voltage converter to supply lower operation voltage for advanced transistors. The function of a voltage converter is to convert an input voltage into a regulable output voltage. Moreover, the output voltage should be independent with the variation of input voltage and output load. Nowadays, there are two popular types of voltage converters, the "Low Drop-Out Linear Regulator (LDO)" and the "Switching mode power supply (SMPS)". Table I shows the comparison between these two types of voltage converters.

The switching mode power supply can be applied on high efficiency voltage converter rather than the linear regulators, especially when the voltage difference between the input and the output of the voltage converter is significant. In addition to the previous advantage, the output voltage of the switching mode power supply can be boosted, dropped, or even converted into a negative voltage. Therefore, its application scope is larger than that of the linear regulators. However, the disadvantage of the switching mode power supply is that ripples will be coupled with the output voltage. The reason is that the switching mode power supply compares the divided voltage of the output with an internal reference voltage to generate digital control signals which then turn on/off the power MOS transistors. There are two common methods to implement the controller mechanism therein, "Pulse-Width Modulator (PWM)" and "Pulse-Frequency Modulator (PFM)" [1]. A general structure of the switching mode power supply is illustrated in Fig. 1.

	LDO	SMPS
Efficiency	Low (30% $\sim$ 50%)	High ($>$ 70%)
Structure	Simple	Complex
Output ripple	Small	Big
Weight & Volume	Big	Small
Input range	Small	Big

TABLE I
Comparison between LDO and SMPS

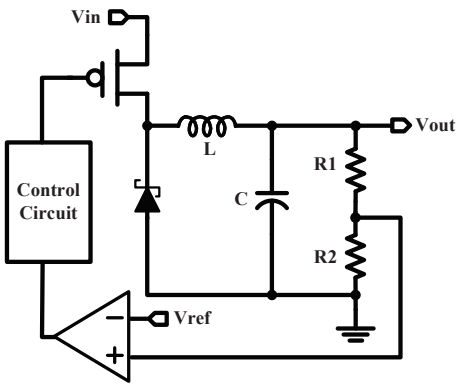

Fig. 1. Structure of switching mode power supply circuit.

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II. The High-Efficiency DC-DC Buck Converter Design

Fig. 2 shows the proposed buck converter structure. We utilize the pulse-width modulator to realize the feedback control. This structure includes a low drop-out linear regulator (LDO) as a voltage source to supply a 3.3 V for internal operation voltage. In this work, A 1.0 V through VREF as a reference voltage which is generated by Bandgap Reference circuit and compared with the output voltage which is divided by R1 and R2. EA (error amplifier) is used to amplify the difference between these two voltages. The output of EA, VEA, is compared with Vramp to generate a digital signal, Q. Dead-time circuit generates two non-overlap signals, QP and QN. Voltage Level Converter shifts the voltage level of QP and controls the power transistor (PMOS1).

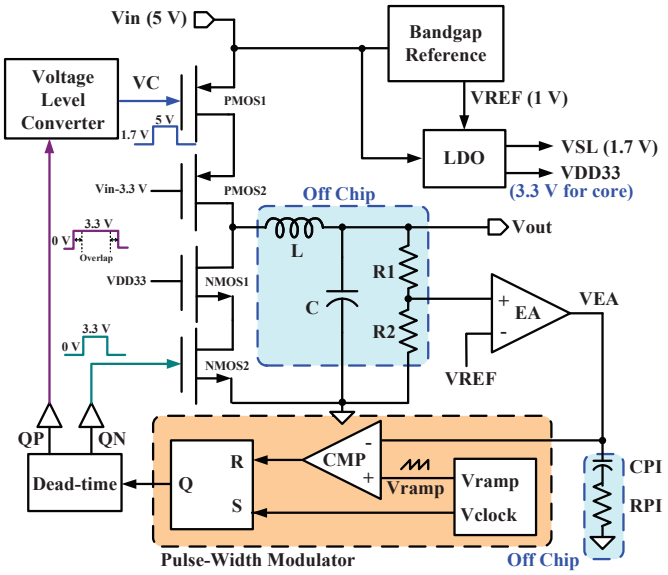

Fig. 2. The proposed DC-DC buck converter structure.

A. Design of the power transistor to resolve the gate-oxide reliability

Since the highest demanded input is 5 V, we should resolve the gate-oxide reliability and leakage current problems. In this work, we proposed two stacked MOSs in the output stage as shown in Fig. 3. In order to cut off the PMOS1 completely and prevent any leakage current, the control signal of PMOS1 should be boosted by 1.7 V. Therefore, a Voltage Level Converter is needed, which is shown in Fig. 4. QP and QP_Bar are a pair of differential voltages. When QP is "1", then the MN03 is turned on and the voltage of VC_Bar is dropped. Therefore, the voltage of VC is boosted as MP02 is turned on and MP01 is cut off. A positive feed-back loop is composed of MP01 and MP02 which can enhance the voltage transition speed. Finally, 5 V is passed through VC and the output voltage at VC_Bar becomes the summation of VSL and the threshold voltage of MP03, which is close to VSL.

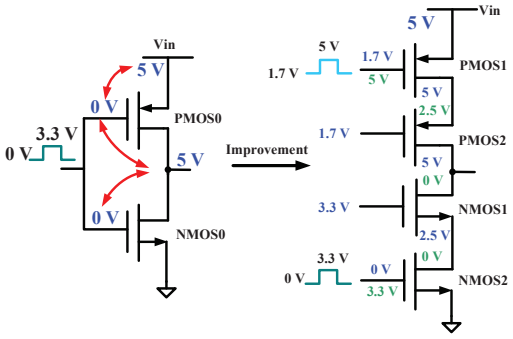

Fig. 3. Stacked output stage.

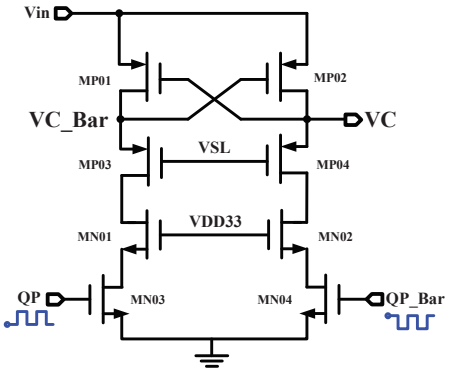

Fig. 4. Schematic of Voltage Level Converter.

B. Design of the Pulse-Width Modulator

The Pulse-Width Modulator compares the voltage VEA and a triangular voltage, Vramp. It generates a pulse train of which the duty cycle is determined by the difference between VEA and Vramp. The Pulse-Width Modulator is composed of a voltage comparator, a clock and ramp signal generator, and a latch, as shown in Fig. 2.

In this work, we use a high-speed comparator. The comparator circuit mainly consists of three blocks: Pre-amplification, Decision circuit, and Output buffer as shown in Fig. 5. A differential pair and active loads are used to achieve the Pre-amplification function. The Decision circuit needs to distinguish the difference in a few mV level between the input voltages to have a high precision. We use a positive feedback network to increase the gain of the decision circuit. The output buffer stage is used to slice the output signal of the Decision circuit into digital signals.

The schematic of clock and ramp signal generator is shown in Fig. 6. VH and VL are two reference voltages and VH is always larger than VL. When Vclk is "0", then MN7 is cut off such that I1 and Icg are identical. In the meantime, Ct is charged by Icg and Vramp is rising. When the Vramp is larger than VH, then CMP_H turns "0" and CMP_L turns "1". Meanwhile, Vclk turns "1" and MN7 is turned on. When MN7 is turned on, Vramp is discharged through MN7 until Vramp

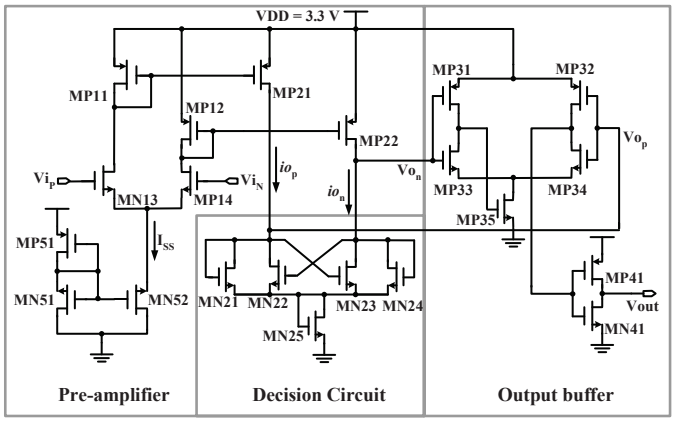

Fig. 5. The schematic of the comparator.

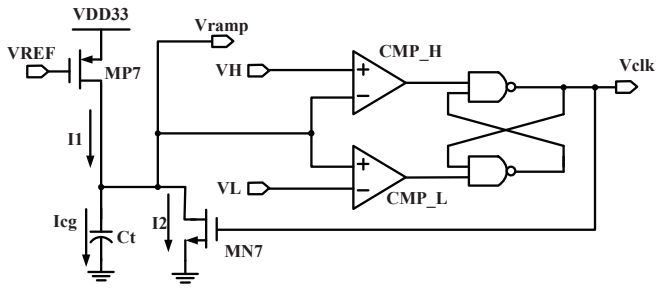

Fig. 6. The schematic of the clock and ramp signal generator.

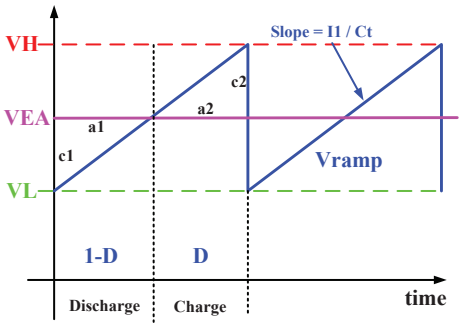

Fig. 7. Triangle voltage waveform.

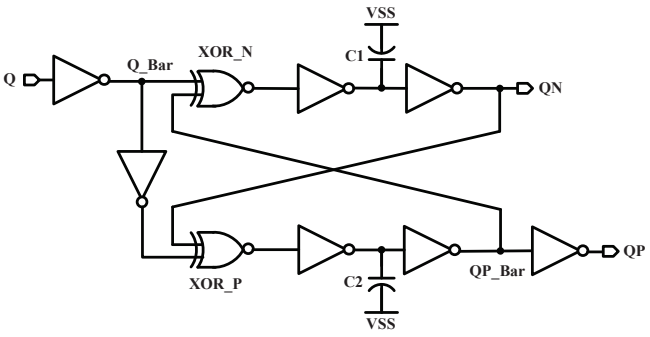

Fig. 8. Dead-time circuit.

is smaller than VL. Therefore, we can get a clock signal via Vclk and a ramp signal via Vramp.

The peak-to-peak value of the ramp signal is decided by VH and VL as illustrated in Fig. 7. A buck converter operated in the continuous-conduction mode (CCM) has conversion relationship given by Eqn. (1) [3], where VH and VL are upper and lower bounds of the ramp signal, D is the duty cycle pulse ratio of signal Q. The transition frequency of the ramp signal, f_{ramp}, is decided by Eqn. (2).

$$\mathrm{D} = \frac{\mathrm{VH} - \mathrm{VEA}}{\mathrm{VH} - \mathrm{VL}} = \frac{\mathrm{Vout}}{\mathrm{Vin}} \tag{1}$$

$$f_{ramp} \cong \frac{\mathrm{I1}}{(\mathrm{VH} - \mathrm{VL}) \cdot \mathrm{Ct}} \tag{2}$$

Dead-time circuit generates a pair of non-overlap control signals which can prevent any short current and improve the efficiency. Fig. 8 shows the schematic of Dead-time circuit design. When the input signal Q is "1", Q_Bar is "0". In the meantime, XOR_N equals to QP_Bar or the previous state, logic "0". Then XOR_P is flipped to "1", because QN is "1", and QP_Bar is changed to "1" by the C2 delay path. Therefore, QP leads QN on the rising edge of input signal Q. By contrast, QN leads QP on the falling edge of input signal Q. Consequently, QN and QP become a pair of non-overlap control signals for the power transistors.

C. Design of Internal Reference Voltage

The reference voltage circuit is critical to any analog circuit design, especially in the voltage converter design. Fig. 9 shows the schematic of Bandgap and LDO design. Left side of Fig. 9 is a bandgap bias circuit [2]. It generates a PVT-independent reference voltage, VREF. In this work, the reference voltage, VREF, is 1.0 V, which is also a reference voltage to the LDO circuit. The LDO circuit generates all the biases and a 3.3 V operation voltage for the internal circuits. The series resistors, RO0 and RO1, monitor the output voltage by a simple voltage division. A feedback voltage, Vf, is fed back and compared with the output voltage of the bandgap circuit by an error amplifier. The error amplifier then feeds a control voltage into the pass transistor, MPL11, to regulate the output voltage according to difference between feedback voltage and output voltage of the bandgap circuit. A faster speed of the feedback loop comes along with a more stable output voltage.

III. Simulation and Implementation

The proposed design is implemented by a typical TSMC 0.18 μm mixed-signal CMOS process. The external inductor and capacitor are 10 μH and 22 μF, respectively. The equivalent series resistance (ESR) of the capacitor is 0.1 Ω. The compensation resistor and capacitor is 100 KΩ and 1 nF, respectively. Fig. 10 shows the simulation waveform of line regulation and load regulation. The input voltage, Vin,

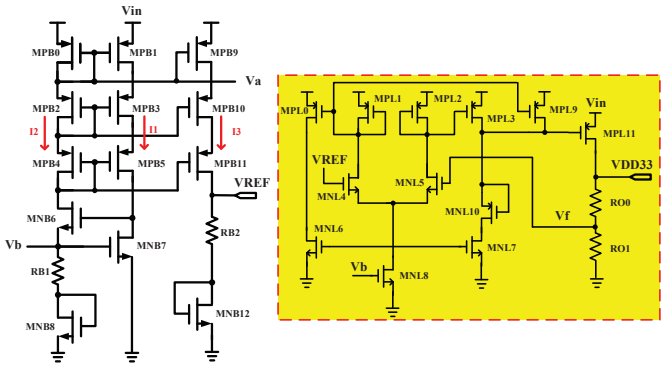

Fig. 9. Schematic of Bandgap and LDO.

vary from 5 V to 4 V, and the output current vary from 100 mA to 50 mA. VREF is a 1.0 V reference voltage. Fig. 11 shows the simulation with temperature variation which vary from -40 ^{o}C to $+125$ ^{o}C. According to the results of Fig. 10 and Fig. 11, the output voltage in this work can resist the variation of input voltage, output current and temperature. Fig. 12 shows the die photo of the DC-DC buck converter. The core area is less than 0.184 mm^2. The performance of the proposed design is tabulated in Table II. Table III shows a comparison between our work and prior works. The chip area, efficiency, and temperature tolerant of our design are better than those of prior works.

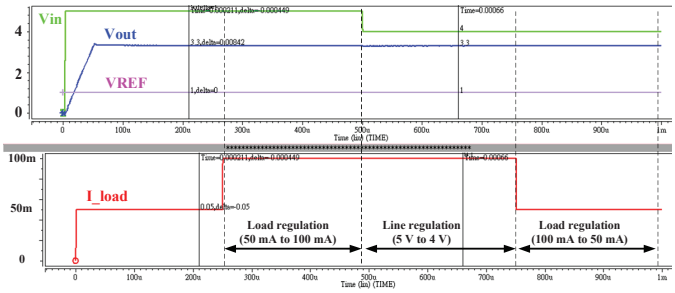

Fig. 10. Simulation waveform of line regulation and load regulation.

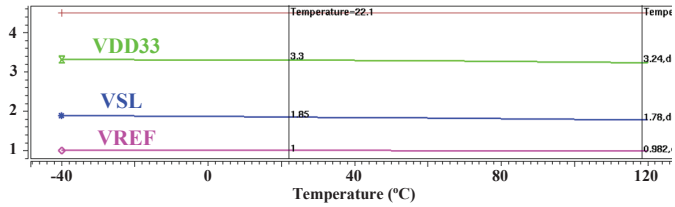

Fig. 11. Simulation with temperature variation.

IV. Conclusion

This paper presents a DC-DC step-down converter. The input voltage range can reach almost 3 times of VDD voltage through the proposed stacked power transistors without any high voltage techniques process to resolve the gate-oxide reliability and leakage current problems. The efficiency is higher than 91%. The temperature tolerant is wide enough to be used in a rugged environment, likes car electronics.

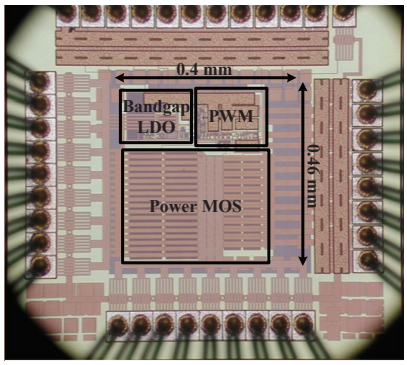

Fig. 12. Die photo of the DC-DC buck converter.

	Line regulation	Load regulation
Vout = 3.3 V	0.038%/V	0.343%/V
Vout = 1.8 V	0.055%/V	0.346%/V

TABLE II

Simulation result of line regulation and load regulation

	[4]	[5]	[6]	Ours
Year	2004	2005	2007	2009
Technology	0.25 μm	0.35 μm	0.6 μm	0.18 μm
Area (mm^2)	4.16	0.9	1.353	0.184
Vin (V)	2.8$\sim$5.5	2.4$\sim$4.2	2.2$\sim$6	3$\sim$5
Vout (V)	1$\sim$1.8	1.3$\sim$3.5	0.6$\sim$Vin-0.2	1$\sim$Vin-0.2
Efficiency (%)	90	65$\sim$95	88.5	91
Temperature (^{o}C)	N/A	0$\sim$75	0$\sim$75	-40$\sim$125

TABLE III

Comparison between prior works and ours

Acknowledgment

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