A Low Power Wake Up Detector for ECU Nodes in An Automobile FlexRay System[1]

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Abstract **– This investigation presents a low power wake-up detector design to monitor wakening signals in a FlexRay-based car network. The detector is required to wake up the bus driver that is operated in the idle low power mode provided that a wakening signal appears. The proposed detector utilities two low-power comparators with hysteresis function to carry out the required wake-up function and state recognition at the receiver end of the FlexRay bus.**

Key word: low power receiver, FlexRay, hysteresis, wake-up.

I. INTRODUCTION

The FlexRay standard is designed for an in-car network [1], Fig. 1 shows FlexRay application in-car networks, which can be used in the realization of X-by-wire systems.

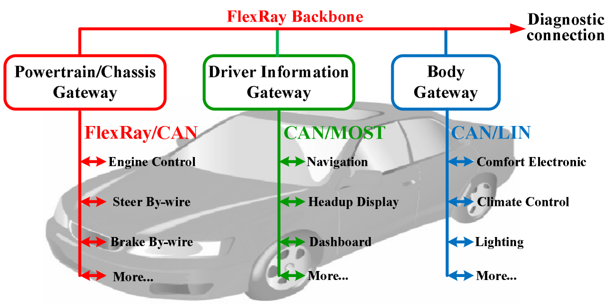

Fig. 1. FlexRay in X-by-wire usages.

Fig. 2 shows the FlexRay bus driver block diagram. According to Flexray standards, the bus driver needs a detector to monitor wake-up events. The wake-up detector is then deemed as a critical part of the FlexRay bus driver.

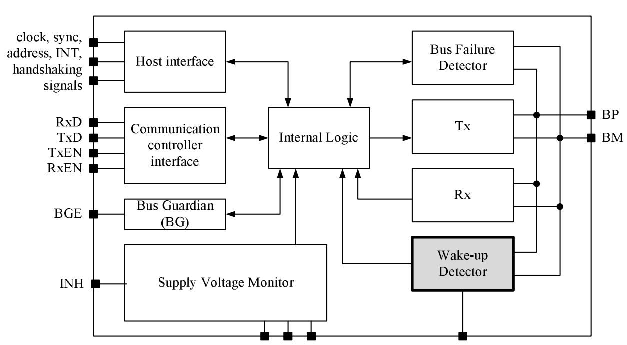

Fig. 2. FlexRay bus driver block diagram.

The power management is indispensable in automobile network for the sake of booming low power demand. When some ECU nodes are in the idle state, the bus driver in the FlexRay system might change into the low power mode. Therefore, the in-car network could save power and enhance the energy efficiency. Fig. 3 shows the operation mode transition of the bus driver in FlexRay systems.

II. WAKE-UP DETECTOR DESIGN FOR FLEXRAY SYSTEM

The low power wake-up detector, thus, is in charge of the power management function in FlexRay-based systems. Compared with normal receivers of FlexRay bus drivers, the wake-up detector consumes less power when bus drivers are operated in the idle low power mode. When the wake-up detector receives the signal that matches the length of the wake-up signal required by the FlexRay specification, the bus driver will be waken up and transited form the idle low power mode to the normal mode.

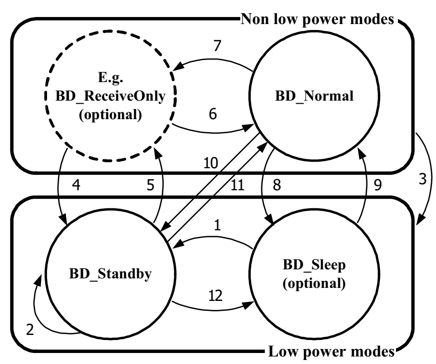

Fig. 3. Operation mode transitions.

In the FlexRay system bus, BP and BM are the solely pair of differential signals. Therefore, the wake-up detector must identify the BP and BM differential signals to deliver a digital signal to the communication controller of the bus driver. Thus, the time length and the pattern of the wake-up signal can be examined. Fig. 4 shows the signal for the wake-up pattern recognition in a FlexRay system.

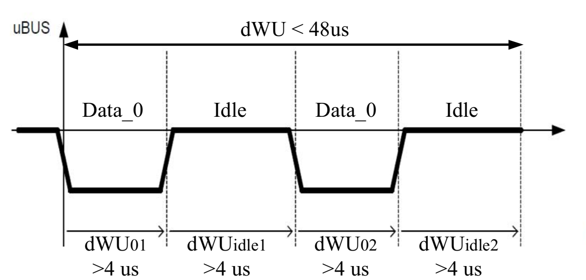

Fig. 4. Wake-up pattern recognition

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A. Design of the low power wake-up detector

The low power wake-up detector for FlexRay systems must recognize the idle state and the received bits. Meanwhile, the wake-up detector must retain the power saving feature. We propose a 2-comparator scheme with hysteresis to achieve the required functions. Referring to Fig. 5, Comparator2 is used to determine data_0 or data_1, Comparator1 and Comparator2 are used to detect whether the input signals on the bus is in the idle state or not. The Rdata and Ridle signals are generated and sent to the following communication controller of the bus driver to check the time length and the pattern of wake-up signal.

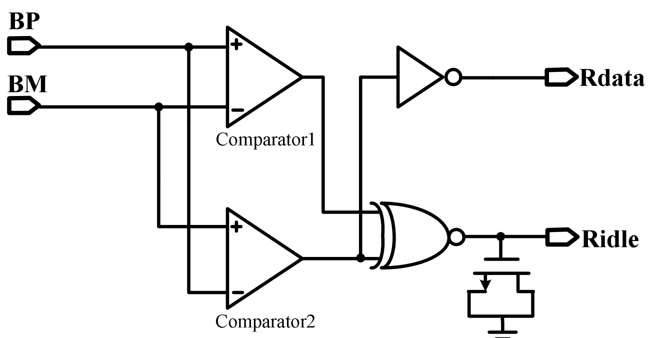

Fig. 5. The schematic of the wake-up detector.

B. Design of the comparator

The circuit of the comparator with a hysteresis function [2] can filter out the noise of the bus. Referring to Fig. 6, the input stage of the comparator is composed of a simple differential input circuit and an active current source. The gate drives of M1 and M2 can be adjusted to change the voltage threshold of comparator. The gate drives of M3、M4、M6 and M7 are consist of the determining circuit, which realizes the hysteresis function. Different hysteresis function can be carried out by tuning these gate drivers. The output stage of the comparator is a simple inverter.

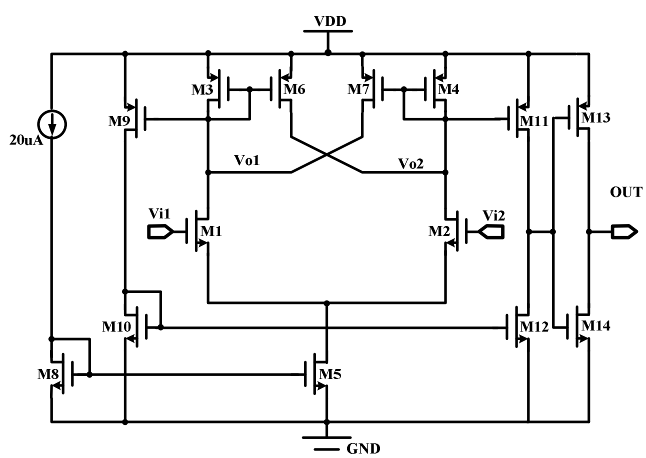

Fig. 6. The circuit of the comparator.

III. Implementation and Measurement Result

The proposed design is carried out by a typical 0.18 μm single-poly six-metal CMOS technology. Verified by all-PVT-corner post-layout simulations, the design of the low-power detector can meet 40 Mbps throughput requirement in a single channel. Fig. 7 shows the post-simulation waveforms that 40 Mbps data rate is received by Rx, where Rdata, Ridle are generated. Table I shows the comparison between FlexRay 2.1B specification and our design to prove that all of required receiver specifications are met. Table II shows the power consumption of the wake-up detector measured on-silicon.

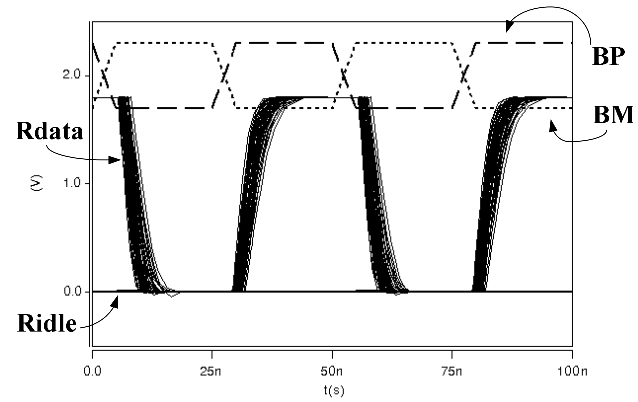

Fig. 7. Post-simulations of 40 Mbps data rate on Rx.

TABLE I
SPECIFICATIONS OF THE PROPOSED RECEIVER

RECEIVER SPECIFICATION		Simulation	Measurement
Receiver delay, negative edge	< 100 ns	< 4.4 ns	5.2 ns
Receiver delay, positive edge	< 100 ns	< 3.9 ns	4.2 ns
Receiver delay mismatch	< 5 ns	< 0.5 ns	<1 ns
Idle reaction time	50~400 ns	< 16 ns	17.2 ns
Activity reaction time	100~450 ns	<13 ns	15.6 ns

(NOTE: BUS DRIVER DELAY IS NOT INCLUDED)

TABLE II
POWER CONSUMPTION OF THE WAKE-UP DETECTOR

DIFFERENTIAL SIGNAL STATE ON BUS	Simulation	Measurement
40Mbps	3.80 mW	3.37 mW
Wake-up signal	2.01 mW	1.76 uW
Idle (2V)	742.9 uW	699.6 uW
Idle low power (0V)	251.6 uW	240.9 uW

(NOTE: PAD POWER IS NOT INCLUDED)

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