A High Voltage Battery Charger with Smooth Charge Mode Transition in BCD Process

Shang-Hsien Yang, Jen-Wei Liu, Yi-Hong Wu, Deng-Sian Wang, Chua-Chin Wang
Department of Electrical Engineering, National Sun Yat-Sen University
No. 70, Lienhai Rd., Kaohsiung, Taiwan
{ccwang}@ee.nsysu.edu.tw

***Abstract*—A 60 V battery charger implemented using TSMC 0.25 µm Bipolar-CMOS-DMOS (BCD) 60 V process is presented in this work. A novel transition method is proposed to ensure smooth transitions between constant current (CC) and constant voltage (CV) modes. Since the proposed approach would require only additional diodes, power consumption and chip area are conserved in comparison with other sophisticated methods proposed in prior works. The charger sources a current of 50 mA in CC mode and has an efficiency of 75% ~ 80% throughout the charging sequence. The supply voltage is kept at 3 volts higher than the battery voltage throughout the charging sequence to maintain charging efficiency. A thermal protection circuit is included in this design to prevent the charger from operating at a temperature over the maximum allowed temperature.**

I. INTRODUCTION

In the past, battery chargers fabricated in conventional integrated circuit processes was limited to operating voltages ranging from 3 to 5 volts. While such battery chargers can still find applications in handheld electronic devices such as cell phones, PDAs, and digital cameras, it is not feasible to design chargers in such processes to fulfill the demands of devices with higher voltages, such as laptop computers and electrically powered bicycles. However, with the availability of the recently developed Bipolar-CMOS-DMOS (BCD) process that covers voltage up to 60 V, it is now possible to realize high voltage battery chargers in integrated circuit technology instead of using discrete power electronic devices.

TSMC 0.25 µm BCD 60 V process provides a variety of devices, including 0.25 µm (2.5 V) CMOS, 0.5 µm (5 V) CMOS, 0.8 µm (60 V) lateral diffused MOS (LDMOS), high voltage bipolar npn transistors, diodes, Zener diodes, and Schottky diodes for high voltage circuit designs. Controller circuits, both analog and digital, are implemented using 0.25 µm/0.5 µm CMOS. By contrast, the high voltage output drivers are carried out by the 0.8 µm LDMOS as the output drivers [1]. Thus, in this design, the 0.8 µm LDMOS transistors serve as Power MOS to charge the battery while other analog circuits are implemented using 0.5 µm CMOS.

In this paper, a 60 V battery charger with constant-current (CC) /constant-voltage (CV) control and over-temperature protection is presented. The charging strategy, advantages, and limitations of the proposed charger using TSMC 0.25 µm BCD 60 V process thereof are discussed in Section II. Section III covers the characteristics and analysis of this charger in the CC or the CV modes, along with the thermal-protection mechanism which protects this charger from overheating. The measured current, voltage, and thermal results are shown in Section IV.

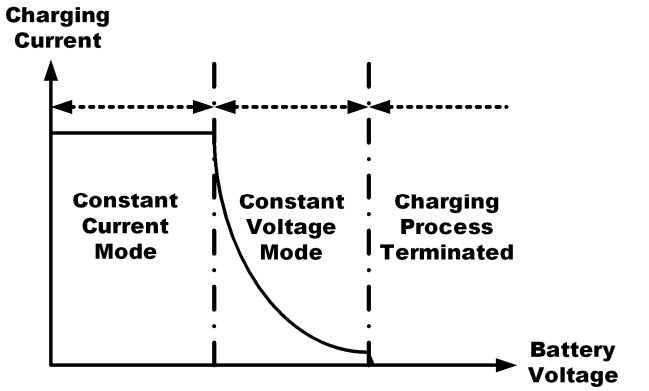

Fig. 1. Typical charging sequence consisting of constant current (CC) and constant voltage (CV) modes.

II. CIRCUIT DESCRIPTION

A. Charging Strategy

Generally speaking, a battery charger starts the charging sequence by sourcing a constant regulated current (CC) instead of a regulated voltage to the battery, since its internal equivalent series resistance (ESR) is low. Forcing the battery to be charged with a constant voltage will result in excessive charging current, which might bring destruction upon both the battery and the charger. However, as the battery voltage rises, its internal ESR also increases. If the battery charger continues to source the same regulated current into the battery, it is likely the battery would become overheated and eventually melt. Hence, it is necessary to switch the battery charger into the constant voltage (CV) mode and sourcing a decreasing current into the battery. When the battery voltage reaches the designated voltage level, the charging sequence is terminated. This charging strategy, well-known as the constant-current /constant-voltage (CC/CV) technique, has been widely used in prior literatures [2] - [4].

B. Circuit Structure

As shown in Fig. 2, the structure of the proposed battery charger includes an error amplifier, EA_1, Level Shifter, LD_{N1}, and Power MOS, LD_{Power}. EA_1 compares the shunt-feedback battery voltage, V_{bf} with reference voltage, V_{ref} and drives the gate of LD_{N1} with a gate drive voltage V_{drive}. Since 0.5 µm CMOS transistors can allow a maximum voltage of only 5 V, the level shifter is used to shift the voltage level from 0 - 5 V to a higher level in order to drive Power MOS LD_{Power}. An external power supply is used to provide the Level Shifter and Power MOS LD_{Power} with a variable voltage. To maintain efficiency, the variable voltage is maintained at 3 V higher than the battery until it reaches 60 V and the battery voltage reaches 57 V. After that specific operating point, the power supply maintains its output at 60 V.

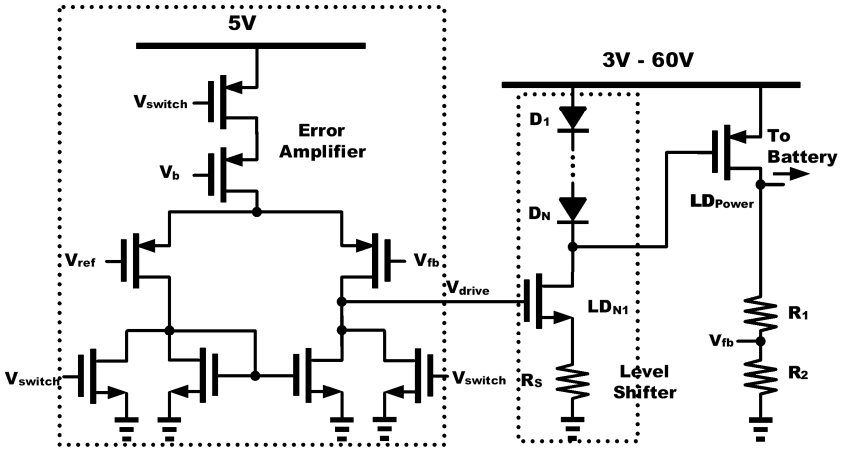

Fig. 2. The proposed CC/CV loop.

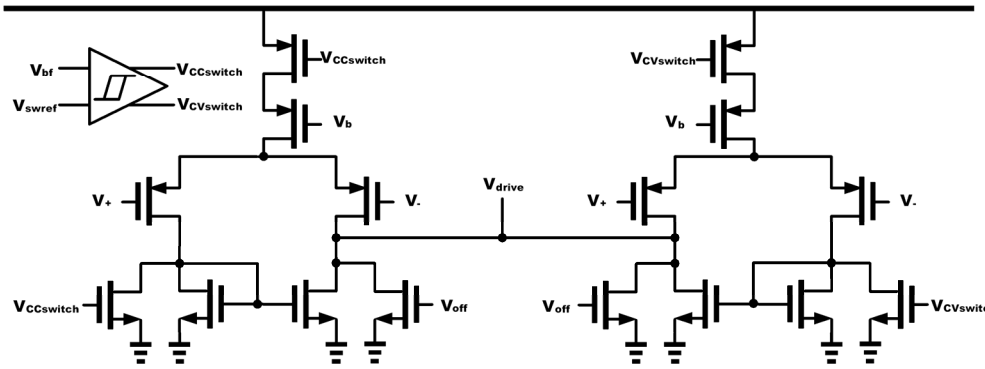

Fig. 3. One possible implementation of CC/CV dual loops.

Although TSMC 0.25 μm BCD 60 V process offers good overall performance such as high transconductance parameters (K_n and K_P) and low R_{DSon}, this advanced process has its restrictions. Firstly, the maximum sustainable voltage across the gate and source of the 0.8 μm LDMOS is limited to 5 V such that P-type LDMOS transistors are hard to be driven directly with an analog/digital controller circuit realized in 0.5 μm CMOS. Worse yet, the maximum voltage across the two plates of a MIM capacitor is 10 V according to the measurements of several test-keys. Therefore, conventional frequency compensation methods such as the schemes using Miller capacitors and pole-splitting are very inconvenient. As a consequence, the overall closed-loop stability becomes an issue if any circuit block is not designed carefully. It is worth noting that small Miller capacitors can still be realized by using dummy LDMOS transistors, which is carried out by coupling the gate and source of the dummy N-type LDMOS together with a lower voltage node, and with a higher voltage node coupling to the drain. It is also possible to realize the Miller capacitor using P-type LDMOS by coupling the source and gate together to a higher voltage node, and its drain to a lower voltage node. Unfortunately, the capacitance attained by these methods is considerably small with respect to size.
The schematic of the error amplifier is shown in Fig. 2. V_{switch} is used to turn on or off the error amplifier with transistor $M_{switch1}$, depending on the charger temperature, the battery voltage, and the charging sequence. Transistor $M_{switch2,3}$ are used to discharge the accumulated charge in the parasitic capacitors at the drain node of $M_{switch2,3}$, so that V_{drive} is grounded and LD_{N1} of the cascaded level shifter can be fully turned off.

III. Modes of Charger Operation

A. Prior CC/CV Charge Modes

As depicted in Fig. 3, conventional chargers with CC/CV charge modes include one differential amplifier for CC operation mode and the other one for CV operation mode. A comparator is used to compare the shunt-feedback battery voltage V_{bf} with a predefined voltage V_{swref} to determine which differential amplifier will be turned on. Notably, extra glue logic is added to the control to switch both differential amplifiers off when the charging sequence is terminated or under the situation when the charger is overheated. A truth table is given in Table I which tabulates the modes of the entire charger operation.

Table I
Four Operation Modes
(0 Represents 0V and 1 Represents 5 V)

	$V_{CCswitch}$	$V_{CVswitch}$	V_{off}
CC mode	0	1	0
CV mode	1	0	0
Charging Terminated	1	1	1
Overheat	1	1	1

The charger rapidly transits between CC and CV mode before it can stably settle in CV mode as shown in Fig. 4. This can be an issue hindering the battery from being charged properly. When V_{bf} is higher than the predefined voltage V_{swref}, the charger leaves the CC mode and enters the CV mode. The abrupt change in operation voltage may cause a drastic change of the output current, which in turn may cause the battery voltage to drop.

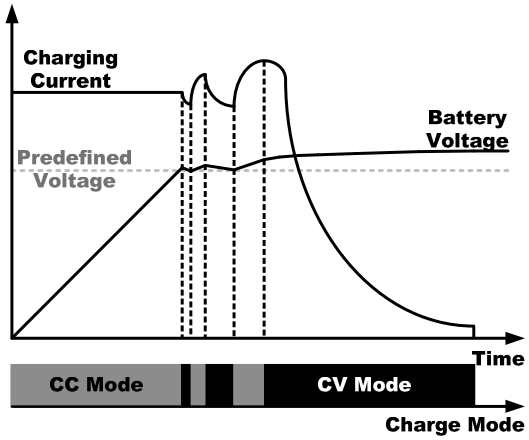

Fig. 4. The transition from CC to CV mode.

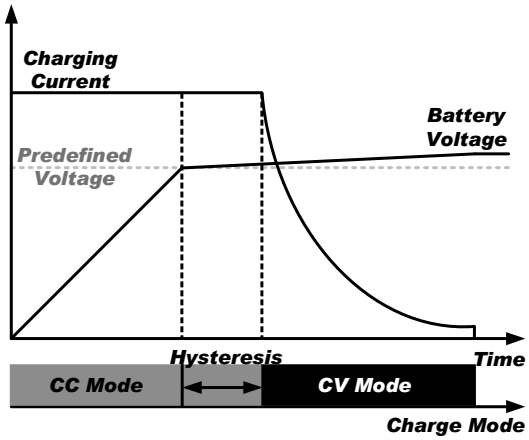

Fig. 5. The transition from CC to CV mode using a hysteresis comparator

Consequently, V_{bf} drops below the predefined voltage V_{swref}, and the charger is switched back to CC mode. As observed in [4], the oscillation may continue until the battery is fully charged. One apparent solution is to add hysteresis to the comparator to filter out the rapid oscillation. As demonstrated in Fig. 5, hysteresis is required if a comparator is used to determine the CC/CV modes. However, some drawbacks still exist in the aforesaid structure. If the hysteresis range is made too large, the entrance to CV mode might be over delayed, causing excessive heat. By contrast, if the hysteresis range is made too small, the rapid oscillation may still occur [4]. To conclude, the use of a comparator to determine between CC and CV mode is not an ideal solution.

Several sophisticated alternative solutions have been proposed in previous literature, [2], [4]. However, all the reported additional circuits further complicate stability analysis and deteriorate the overall battery charger robustness. Furthermore, the inclusion of these additional circuits requires additional power consumption, reducing the efficiency of the battery charger.

B. Proposed CC/CV Charge Mode Selection

To overcome these tradeoffs, a novel implementation of the CC/CV loop is proposed in this work by combining two loops into one, as shown in Fig. 2. The new scheme consists of a linear dropout regulator (LDO)-like CV loop and a series of diodes D_1 to D_N, where N is the number of diodes. Similar to the operation of a typical LDO, the error amplifier drives the cascaded level shifter with the error voltage of the shunt-feedback battery voltage V_{bf} and reference voltage V_{ref}. The level shifter shifts the error signal to an appropriate level to drive the Power MOS LD_{Power}. Resistor R_s is used to reduce the power consumption of the level shifter, which can be quite high when its DC path is biased at 60 V.

Diodes D_1 to D_N are then turned on and the V_{gs} of LD_{N1} and LD_{Power} are clamped at a voltage V_{Clamp}. As a result, constant charging current is maintained regardless of the battery voltage. This current is in fact the maximum current allowed by the charger, defined as:

$$I_{CC} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{Clamp} - V_{thp})^2$$
$$= \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(N \times V_{Don} - V_{thp})^2 \qquad (1)$$

where V_{Don} is the turn on voltage of the diodes and V_{thp} is the threshold voltage of the Power PMOS. Notably, with a proper selection of R_S, the drifting of I_{CC} caused by temperature variation of V_{Don} can be reduced.

As the battery voltage rises, the required charging current falls below I_{CC}, such that V_{drive} becomes lower and diodes D_1 to D_N are turned off. The charger returns to its LDO-like operation, and will continue to charge the battery in CV mode until the charging sequence is terminated. The proposed charger, unlike conventional chargers, depends on a current quantity, I_{CC}, instead of a voltage quantity, V_{swref}, to transit from the CC mode to the CV mode. Since the charging current is decreased smoothly, the possibilities of a rapid change between the CC and the CV modes are eliminated. Furthermore, fewer circuits are required in comparison with the conventional CC/CV chargers. This means lower power consumption and a higher charging efficiency.

C. Thermal Protection

With insufficient cooling, the chip temperature may exceed the maximum allowed operating temperature of the charger [5]. Therefore, a mechanism is needed to prevent the charger from overheating and damaging. The thermal protection circuit utilizes the bandgap voltage reference generator which drives two additional DC paths, where one path provides a proportional to absolute temperature (PTAT) voltage and the other one generates a complementary to absolute temperature (CTAT) voltage. These two generated voltages are compared with a hysteresis comparator, as shown in Fig. 8. To prevent the charger from turning on and off rapidly, a hysteresis of 20 °C is added in our design. According to the simulations, the charger turns off at approximately 110 °C and turns back on when the temperature drops below 88 °C.

IV. Experimental Results

The proposed charger has been fabricated using TSMC 0.25 μm BCD 60 V technology. The chip micrograph is shown in Fig. 10, where the total silicon area is 448 × 631 μm^2 (core) and 586 × 879 μm^2 (with pads). The battery load is emulated with Prodigi 3311D Programmable DC Electronic Load. The variable voltage is supplied by a Chroma 62012p-600-8 Programmable Power Supply. As shown in Fig. 6, the charger begins with a charging current of 50 mA, which slowly rises to 52 mA, since the V_{Don} of diodes D_1 to D_N is also raised slightly as the supply voltage of the level shifter rises from 3 V to 40 V. These diodes are gradually turned off as the battery voltage rises from 40 V to 45 V, and the charger begins to operate in the CV mode, sourcing a decreasing current into the battery. When the battery voltage reaches the designated voltage level of 58 V, the charging process is terminated. Throughout the charging process, the variable supply voltage is kept at 3 V higher than the battery until it reaches 60 V, which is the maximum voltage allowed for TSMC 0.25 μm BCD 60 V process.

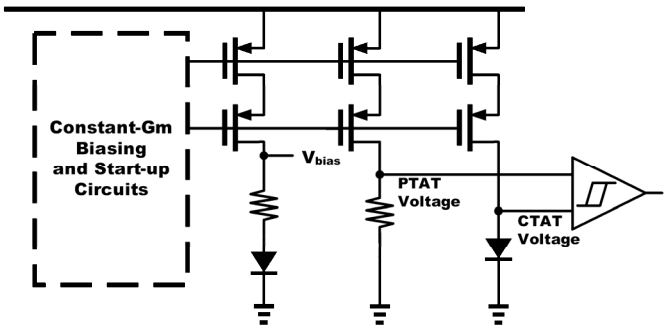

Fig. 6. The schematic of the bandgap reference generator, a CTAT, and a PTAT voltage generator.

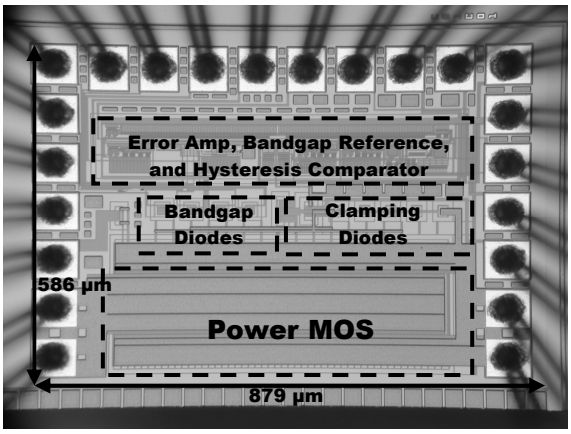

Fig. 7. Chip micrograph.

The relationship between the battery voltage and the charger efficiency is depicted in Fig. 9. Since the power consumed by the level shifter is proportional to the charging current, the efficiency of the charger increases significantly as the charging current drops.

V. CONCLUSION

This paper presents a high voltage battery charger implemented using TSMC 0.25 µm BCD 60 V process with 50 mA of CC mode charging current. The method of realizing Miller compensation capacitors using the BCD process is briefly mentioned. The proposed method of clamping the gate-source voltage of the Power PMOS with diodes allows smooth transition from the CC mode to the CV mode without the requirement of hysteresis comparators or any other complicated circuits. This prevents an early entrance of the CV mode, which would occur only after the charging current has decreased below a predefined value. The predefined value is determined by the number of diodes in series that clamps the gate-source of the Power PMOS. A thermal protection circuit is also included, which can stop the charging sequence when the charger is overheated.

VI. ACKNOWLEDGMENT

This study has been partially supported by the Chip Implementation Center (CIC), National Science Council under grant NSC98-2220-E- 110-009, Ministry of Economic Affair under grant 98-EC-17-A-01- S1-104, 98-EC-17-A-02-S2-001, 98-EC-17-A-02-S2-0017, and 98- EC-17-A-19-S1-133.

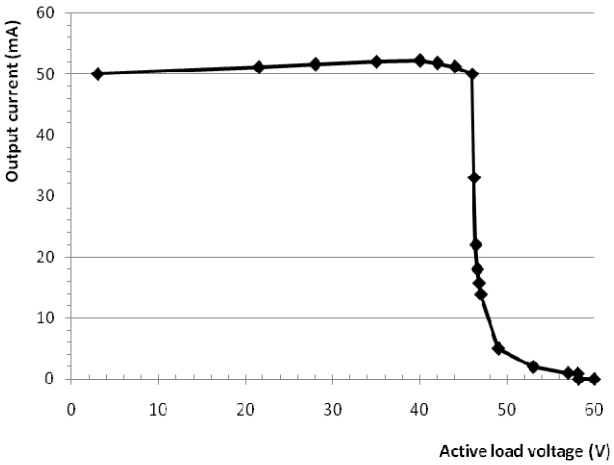

Fig. 8. Measured output current vs. active load voltage.

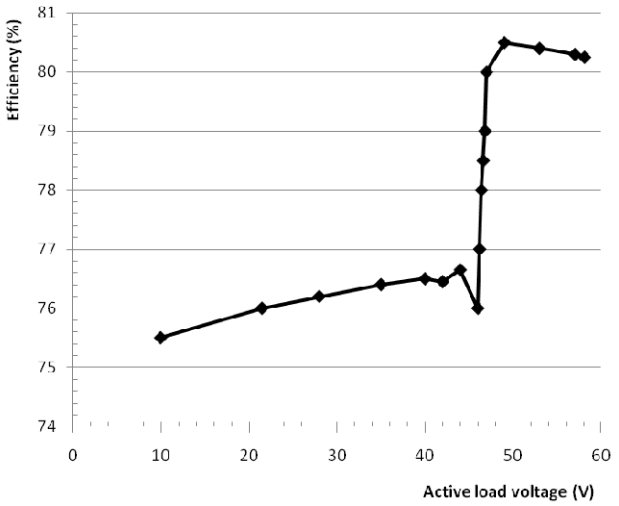

Fig. 9. Measured efficiency vs. active load voltage.

References

[1] "TSMC high voltage technology brochure 2007," Available: http://www.tsmc.com/download/english/a05_literature/12_High_Volt Vol_Brochure_2007.pdf

[2] M. Chen and G. A. Rincón-Mora, "Accurate, compact, and power-efficient Li-ion battery charger circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1180–1184, Nov. 2006.

[3] J. -J. Chen, F. -C. Yang, C. -C. Lai, Y. -S. Hwang, and R. -G. Lee, "A high-efficiency multimode Li–ion battery charger with variable current source and controlling previous-stage supply voltage," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2469–2478, July 2009.

[4] C. -H. Lin, C. -Y. Hsieh, and K. -H. Chen "A Li-ion battery charger with smooth control circuit and built-in resistance compensator for achieving stable and fast charging," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 2, pp. 506–517, Feb. 2010.

[5] J. Qian, "Enhanced-safety, linear Li-ion battery charger with thermal regulation and input overvoltage protection," Available: http://focus.ti.com/lit/an/slyt269/slyt269.pdf

[6] F. Lima, J. N. Ramalho, D. Tavares, J. Duarte, C. Albuquerque, T. Marques, A. Geraldes, A. P. Casimiro, G. Renkema, J. Been, and W. Groeneveld, "A novel universal battery charger for NiCd, NiMH, Li-ion and Li-Polymer," in *Proc. Eur. Solid-State Circuits Conf.*, pp. 209–212, Sep. 2003.