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Feed-forward Output Swing Prediction AGC design with Parallel-Detect Singular-Store Peak Detector

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ABSTRACT

This paper presents an Automatic Gain Control (AGC) circuit design with 200–530 μW average power consumption given a 1 V supply. The Variable Gain Amplifier (VGA) therein comes with 0.9 V input range and output stages with a swing of 0.9 V and a minimum bandwidth of 100 MHz. Feed-forward Output Swing Prediction is used to adjust the gain of the VGA corresponding to the signal envelope detected by a Parallel-Detect Singular-Store Peak Detector. At a maximum refresh-rate of 4 MHz, the AGC is capable of adjusting the gain of the VGA within less than 250 ns when the input signal envelope is reduced by 20 dB, and 100 ns when raised by 20 dB. The circuit design is carried out using a 0.18 μm standard CMOS process with a core area of 0.0024 mm^2.

1. Introduction

Automatic Gain Control (AGC) plays an essential role in modern wireless transceivers for analog/digital radio systems, GPS, WLAN, Bluetooth, ZigBee, and many other applications. They are in charge of adjusting the gain of the associated Variable Gain Amplifiers (VGA) so that constant amplitude of the demodulated signal is provided to downstream circuits under various conditions. Meanwhile, Peak Detectors (PD) in AGCs are responsible for detecting the amplitude of such signals. Notably, data recovery from the input signal can begin only after the AGC circuit has been adjusted to provide the appropriate gain. Such an amplitude adjustment must be faster than the preamble of the transmitted data. For the efficiency of channel bandwidth, the adjustment time should be as short as possible [1].

Traditionally, VGAs designed to provide gain adjustment in a constant period of time offer exponential gain characteristics, which were often implemented using BJTs or emulated with CMOS circuits. However, when the output of the VGA has already saturated, which is usually the case for low power receivers, the actual AGC characteristics deviate from the small signal model intended for constant settling time adjustment. In other words, there would be no constant settling time adjustment even if the VGA has the exponential gain characteristics. Furthermore, the emulation of the exponential gain characteristics in a standard CMOS process [2] usually comes with a high overhead in hardware and degraded performance in bandwidth and power compared with VGAs that are not intentionally designed to attain the exponential gain characteristics [3].

In this study, a 100 MHz AGC operating at 1 V supply voltage is presented. The Feed-forward Output Swing Prediction architecture capable of adjusting the gain of the VGA to the desired value is discussed in Section 2. This section also covers the characteristics and analysis of the Parallel-Detect Singular-Store Peak Detector along with the VGA with high swing input and output stages. The simulation results indicating gain, bandwidth, and response time performances are shown in Section 3.

2. AGC circuit architecture

2.1. Feed-forward Output Swing Prediction

In a Feed-forward Output Swing Prediction AGC loops, a Parallel-Detect Singular-Store Peak Detector is used to detect the input signal envelope, V_{peak}, as shown in Fig. 1. The feed-forward mechanism is accomplished by feeding V_{peak} to the Auxiliary VGA of the Gain Adjustment Loop. $V_{predict}$, the predicted envelope of the actual amplified signal at V_{out} is generated depending on the gain of the Auxiliary VGA. This voltage is regulated by the error amplifier of the Gain Adjustment Loop to a pre-defined value V_{ref} by adjusting the gain control signal V_{err} of the Auxiliary VGA. The Master-Slave configuration of the Gain Adjustment Loop and the Main VGA results in simultaneous gain

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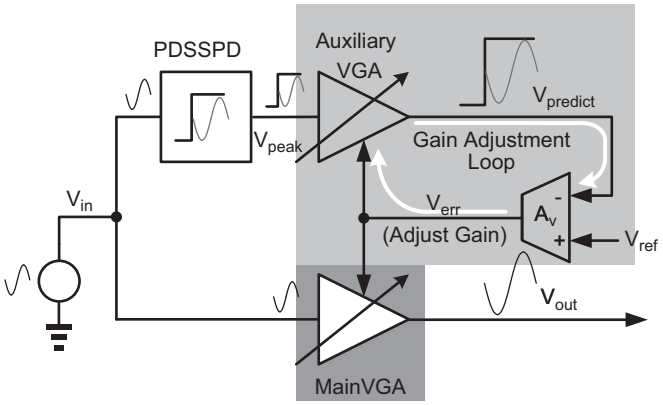

Fig. 1. The proposed AGC with Feed-forward Output Swing Prediction.

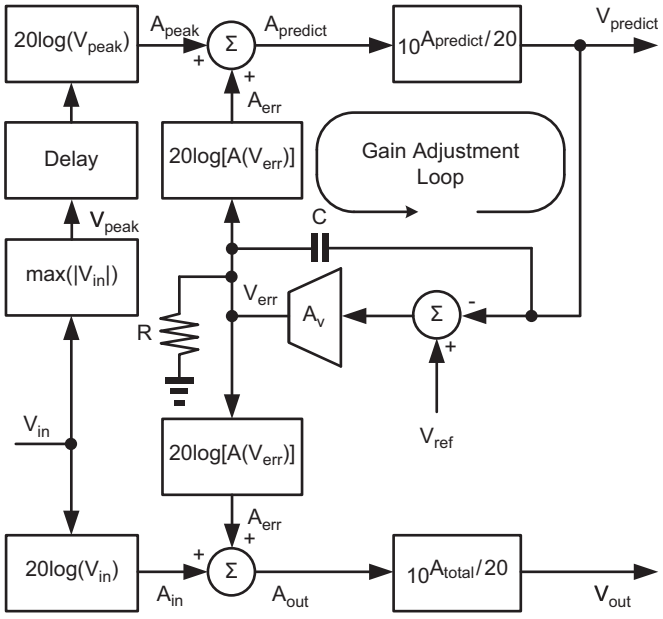

Fig. 2. Model of the Feed-forward Output Swing Prediction AGC.

adjustment between the Auxiliary VGA and the Main VGA. Hence, the gain of the Main VGA can be adjusted to an appropriate value as long as the incoming signal is within the dynamic gain range of the VGAs.

The model of a Feed-forward Output Swing Prediction AGC loop is more comprehensively demonstrated in Fig. 2. V_{peak} is the peak value of the input signal acquired by the peak detector and expressed with $\max(|V_{in}|)$. A variable delay, denoted as Delay block in Fig. 2, is contributed by the peak detector. The delay contributed by this block is nonlinear and dependent on the previously stored V_{peak} value and the present V_{peak} value. The delay becomes significantly longer when V_{peak} changes from a larger value to a smaller value, because the peak detector is required to be discharged. While an actual AGC processes the input signal directly using a voltage value and generates an appropriate gain using a linear scale, the decibels of gain that an AGC system can provide is of interest from a system perspective. For this specific reason, voltage values V_{peak} and V_{in} are converted into A_{peak} and A_{in}, which are expressed in dB in this model. Depending on the gain adjustment voltage V_{err} of the Gain Adjustment Loop, A_{peak} is summed with a corresponding amount of A_{err} to generate $A_{predict}$. As the error amplifier of the Gain Adjustment Loop compares not decibels but voltages, the expression of $A_{predict}$ is converted back into $V_{predict}$, which in turn is used to deduct the predefined V_{ref} such that the gain adjustment voltage of the Gain Adjustment Loop, V_{err}, is generated. With V_{err}, the same amount of A_{err} added to A_{peak} is also applied to A_{in} so that an appropriate A_{out}, which corresponds to a desired V_{out} output signal envelope is generated.

In a feedback AGC system, an integrator-based controller must be used to produce a very low frequency dominant pole such that the phase lag contributed by the peak detector will not jeopardize the stability of the AGC. Unlike the integrator-based controller of a conventional AGC, the bandwidth of the Feed-forward Output Swing Prediction AGC is determined by the frequency response of the Gain Adjustment Loop. Since the VGAs are built to operate at a frequency of 100 MHz, the dominant pole of the Gain Adjustment Loop is determined by the output resistance of the error amplifier, R, the capacitance value of the Miller capacitor C, and the gain of the error amplifier, A_v, which can be expressed as

$$\omega_p = \frac{1}{(1+A_v)RC} \tag{1}$$

Given a constant input signal envelope A_{in}, the relationship between the predefined V_{ref} and A_{out}, the output signal envelope of V_{out} can be modeled as a first-order open loop system shown in Fig. 3. The voltage (not expressed in decibels) transfer function of this system becomes

$$T_{OL}(j\omega) = \frac{A_v S^A_{V_{err}}}{\left(1+j\frac{\omega}{\omega_p}\right)\left(1+j\frac{\omega}{\omega_{VGA}}\right)} \approx \frac{A_v S^A_{V_{err}}}{\left(1+j\frac{\omega}{\omega_p}\right)} \tag{2}$$

where A is the amount of gain provided by the VGA, the S term is the sensitivity of A to the variation of V_{err}, and ω_{VGA} is the high frequency parasitic pole introduced by the VGA, which can be neglected. As long as the frequency components of the variation of A_{in} is within the bandwidth imposed by ω_p, the disturbance on A_{out} caused by this variation can be regulated. Besides, since ω_{VGA} is at a high frequency, the settling time can be solely estimated with ω_p. Both ω_p and ω_{VGA} are sensitive to process variation, and ω_p is also sensitive to the deviation of capacitance value of C in Fig. 2. Hence, the parameters of this AGC system are made conservative such that stability is ensured regardless of process variation and the deviation of capacitance value. Notably, even in the worst case situation, ω_p is increased to 30 MHz while ω_{VGA} is pushed to more than 400 MHz at the FF corner. Hence, the relationship that $\omega_{VGA} \gg \omega_p$ is maintained.

One of the key advantages over traditional feedback AGCs lies in the ability of preventing the output of the VGA to be saturated. First of all, with an appropriate placement of ω_p, the frequency response of the Gain Adjustment Loop is inherently faster than an integrator-based AGC loop. Furthermore, as soon as the Parallel-Detect Singular-Store Peak Detector detects a variation in the envelope of V_{in}, a corresponding A_{in} is generated. Based on this input, the Gain Adjustment Loop immediately adjusts the gain of the VGA to regulate the value of $V_{predict}$ to V_{ref}. Under the assumption that the preceding stages of the AGC are operating correctly and the input waveform is not distorted due to saturation close to the supply rails, the waveform of V_{out} will never saturate. For this reason, the A_{peak} generated by the Parallel-Detect Singular-Store Peak Detector and consequently the V_{err} and

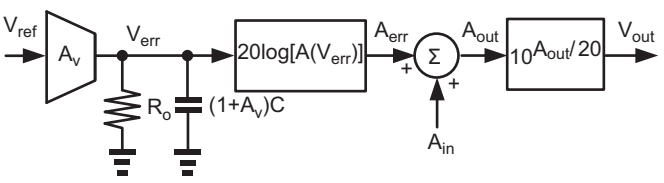

Fig. 3. Reference-to-amplitude open-looped model of the Feed-forward Output Swing Prediction AGC.

$A_{predict}$ generated by the Gain Adjustment Loop will immediately reflect the actual envelope of the signals both at the input and the output. Finally, since the delay contributed by the Parallel-Detect Singular-Store Peak Detector does not appear on the Gain Adjustment Loop, no phase margin is lost by this delay. On the other hand, a traditional feedback AGC needs to wait for the peak detector monitoring the output of the VGA to be discharged before gain adjustment begins, and the output of the VGA remains saturated. In addition, during this period, a traditional AGC will have no idea how "saturated" the VGA is. This results in a significant delay before the gain control voltage can reflect to the amplitude of the output signal. Such a delay can be interpreted as a phase lag to the system. Consequently, the dominant pole has to be placed at a very low frequency such that the frequency response of the AGC behaves like an integrator for the system to be stable.

Finally, the previous assumption requires that the VGA has equal gain for both sine waves and pulse train. Hence, it will be necessary for the VGA used in the Feed-forward Output Swing Prediction AGC to have a wide voltage input range even when operating under a low voltage supply.

2.2. Parallel-Detect Singular-Store Peak Detector

Traditional peak detectors typically consist of an error amplifier, a MOS diode, and a capacitor. The error amplifier serves as a voltage follower charging the capacitor corresponding to the input signal. The MOS diode prevents the capacitor from being discharged. This type of peak detector is often modified by replacing the MOS diode with a current mirror [4], as shown in Fig. 4.

Theoretically, the peak voltage, PD_{out}, stored in the capacitor directly reflects to the envelope of the input signal, V_{in}. However, when the amplitude of the input signal has dropped drastically, the voltage at the output terminal of the capacitor does not discharge spontaneously unless a reset signal is issued. Thus, without an appropriate control of the reset signal, the peak detector will create an invalid voltage for the AGC loop, and the gain of the VGA will not be raised to an appropriate value corresponding to the amplitude drop of the input. In addition, an abrupt reset signal discharges PD_{out} all the way to ground, causing a spurious disturbance to the AGC.

To resolve all these issues, the proposed Parallel-Detect Singular-Store Peak Detector shown in Fig. 5 includes two parallel traditional peak detectors, which independently acquire the amplitude of the incoming signal, V_{in}. The peak values generated by the peak detectors, $PD_{out,0}$ and $PD_{out,1}$, are compared by a comparator, which stores the resulting value in DFF1. Thus, the output value, Q, of DFF1 is determined corresponding to the peak detector number, 0 or 1, which stores the lower peak value. When a pulse generated by either a digital logic or a periodic signal appears at the Refresh terminal, Q masks the Refresh pulse for one of the two reset signals, $reset_0$ or $reset_1$, with the NAND gate.

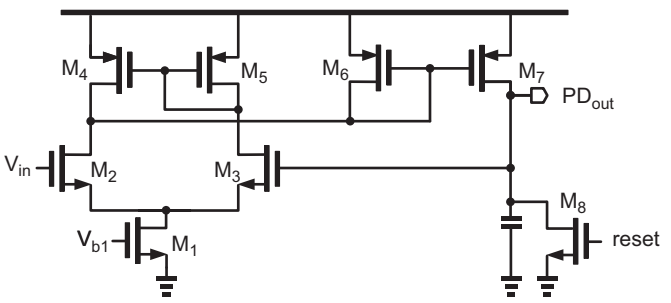

Fig. 4. A traditional peak detector using current mirror.

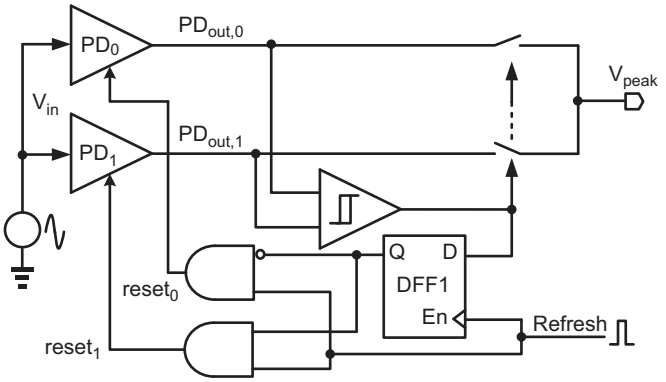

Fig. 5. Parallel-Detect Singular-Store Peak Detector.

As a result, the capacitor of the peak detector with the higher voltage is discharged while the voltage value of the other peak detector remains in its own capacitor. The comparator also controls the analog MUX consisting of two transmission gates so that the appropriate voltage value is passed down to $V_{predict}$. Subsequently, when the amplitude of the input signal becomes smaller, Parallel-Detect Singular-Store Peak Detector can refresh its stored voltage immediately when a pulse is triggered at the Refresh terminal. However, when the amplitude of the input signal remains constant or becomes larger, the input amplitude acquired by both PD_0 and PD_1 remains constant or becomes larger simultaneously. Hence, triggering a pulse at the Refresh terminal will not affect V_{peak}. This idea is further illustrated in Fig. 6(a) and (b). The voltage value of the input envelope appearing at V_{peak} will not be discharged completely by the reset pulse as $PD_{out,0}$ and $PD_{out,1}$. Instead, it is switched between $PD_{out,0}$ and $PD_{out,1}$ with the correct voltage value.

When the input signal amplitude is dropped significantly, a spurious increase of the peak detector voltage could occur as a result of unwanted charge-injection. To avoid misjudgment of gain tuning, the comparator of the Parallel-Detect Singular-Store Peak Detector automatically switches back to the other peak detector to squelch the problem, as depicted in Fig. 6(a), removing the spurious voltage after 1.24 μs.

2.3. Wide input and output voltage swing variable gain amplifier

To allow a wide input swing, both PMOS (M_{10}) and NMOS (M_{11}) transistors are used as the input transconductor, which are depicted in Fig. 7. To avoid the dependence upon the input stage transconductance to the input voltage, the total transconductance of g_{m10} and g_{m11} is a regulated value, G_m, such that

$$G_m = g_{m10} + g_{m11} = \beta(V_{SG10} + V_{GS11} - |V_{thp}| V_{thn}) \tag{3}$$

where $\beta = 1/2\mu_n C_{ox}(W/L)_n = 1/2\mu_p C_{ox}(W/L)_p$.

Apparently, this requirement can be achieved if the voltage across source terminals of M_{10} and M_{11}, $V_{SG10}+V_{GS11}$, is fixed [5]. In order to do so, an electronic Zener diode consisting of transistors M_{13} to M_{17} is placed between the source terminals. This yields a total transconductance of [5]

$$G_m = \frac{g_{m15} g_{m14}}{g_{m15} + g_{m14}} \left[\frac{g_{m16} g_{m17}}{g_{m15}} (r_{o16} \| r_{o13}) + 1 \right] \tag{4}$$

Simulation results shown in Fig. 9 suggest that this voltage varies around only 10 mV when a rail-to-rail sine wave is applied. The currents are mirrored and summed at the drain nodes of M_{19} and M_{21}. Since tuning G_m directly degrades the capability of the electronic Zener diode to regulate the voltage across source terminals of M_{10} and M_{11}, the gain is adjusted by increasing or

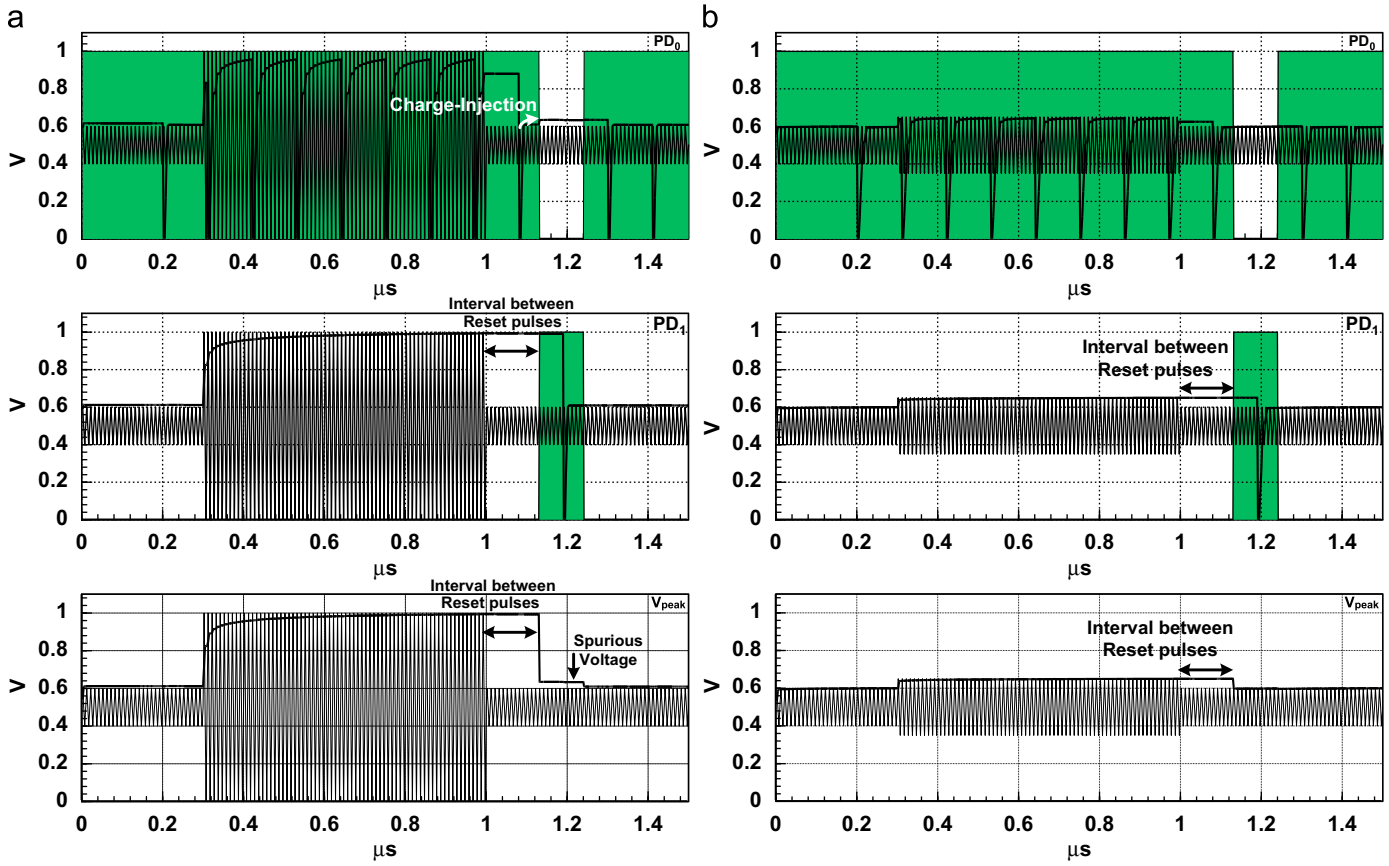

Fig. 6. Waveform of $PD_{out,0}$, $PD_{out,1}$, and V_{peak} when the input signal amplitude is dropped (a) significantly and (b) slightly. The Refresh pulse appears every 0.1 μs.

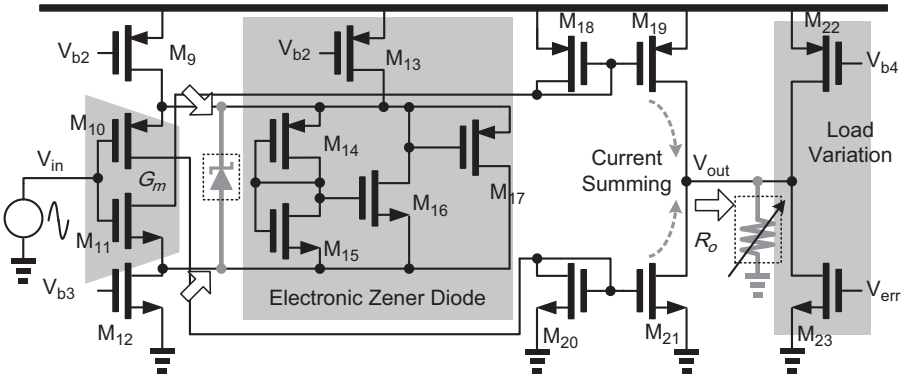

Fig. 7. The proposed rail-to-rail VGA.

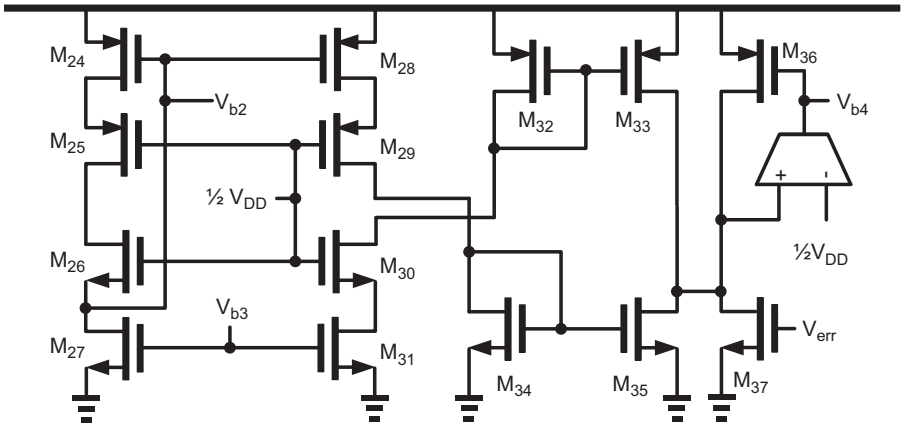

Fig. 8. Bias circuit for the proposed VGA.

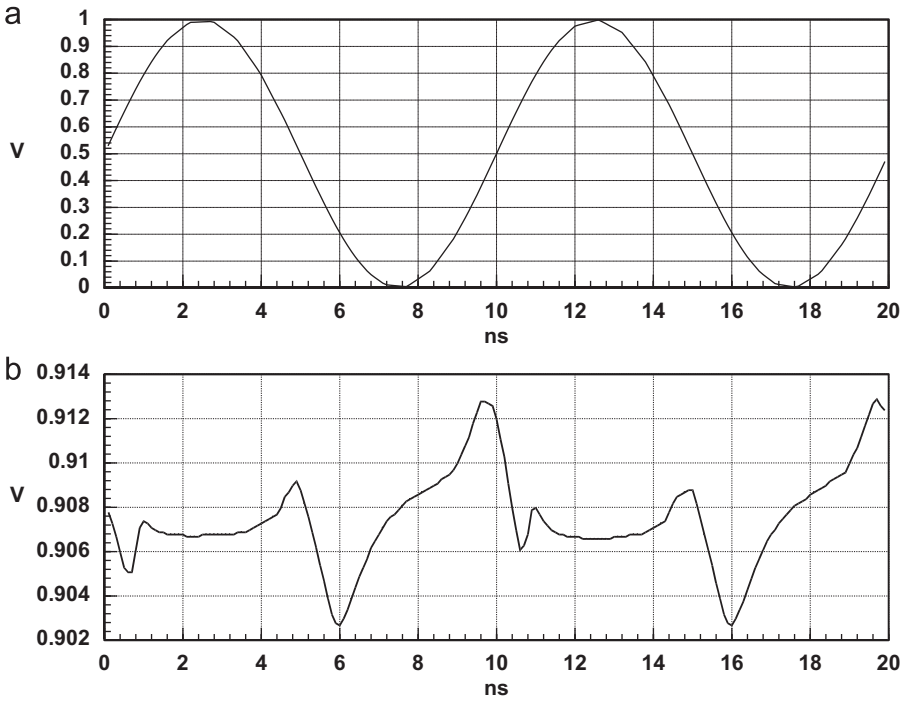

Fig. 9. The (a) input voltage vs. (b) variation of voltage across sources of PMOS M_{10} and NMOS M_{11} when a rail-to-rail sine wave is applied.

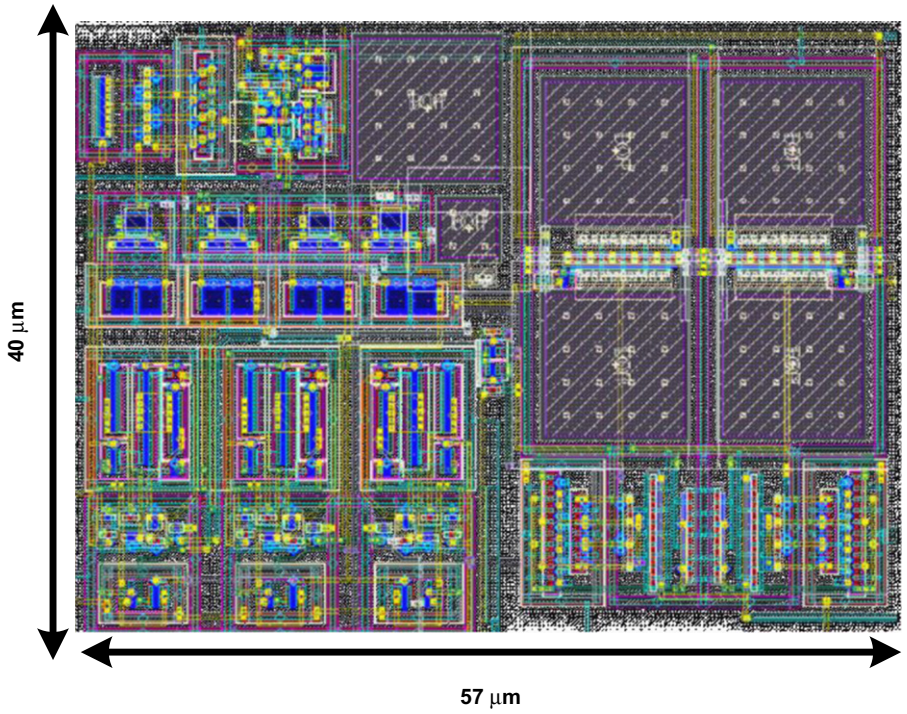

Fig. 10. Layout of the proposed AGC.

decreasing the current of M_{22} and M_{23} using V_{err} to attain varying values of r_{o22} and r_{o23}. As such, the overall variable output resistance of the VGA can be expressed as

$$R_o(V_{err}) = r_{o19} \| r_{o21} \| r_{o22}(V_{err}) \| r_{o23}(V_{err}) \tag{5}$$

If we express r_o as $1/g_o$, the overall gain, A, of the VGA becomes

$$A = \frac{g_{m15}g_{m14}}{g_{m15}+g_{m14}} \left\{ \frac{g_{m16}g_{m17}+g_{m15}(g_{o13}+g_{o16})}{g_{m4}(g_{o13}+g_{o16})[g_{o19}+g_{o21}+g_{o22}+g_{o23}]} \right\} \tag{6}$$

A bias circuit shown in Fig. 8 is used to balance the current of M_{22} and M_{23} to ensure that the DC value of V_{out} is half of the supply voltage, $1/2V_{DD,}$ to allow the maximum possible swing. Transistors M_{24} to M_{31} are used as replicas of transistors M_9 to M_{12} of the VGA to produce V_{b2}. However, since there is no Zener diode used in the bias circuit and the current sourced by M_{13} does not apply here, M_{27} and M_{31} are proportionally smaller than M_{12}. $1/2V_{DD}$ and V_{b3} are provided externally. In a practical realization of systems using an AGC such as the proposed circuit, a voltage regulator should be included, and $1/2V_{DD}$ and V_{b3} can be attained

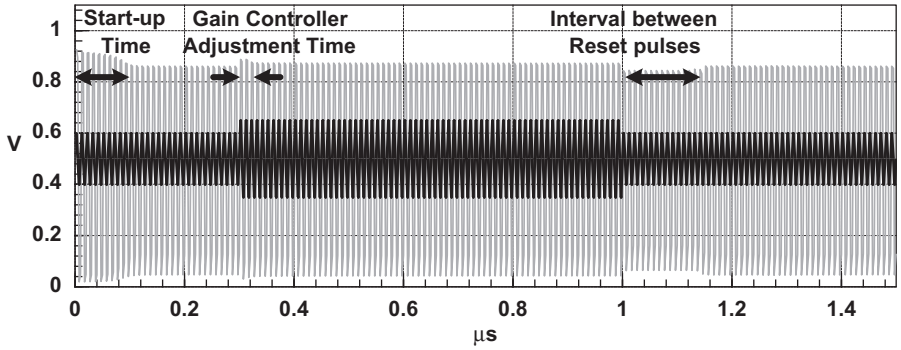

Fig. 11. The input signal (black) vs. the output signal of the AGC (gray).

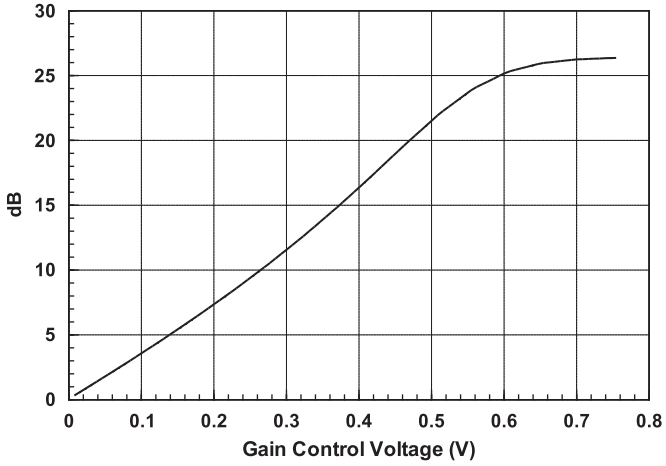

Fig. 12. Gain control voltage vs. gain (in dB).

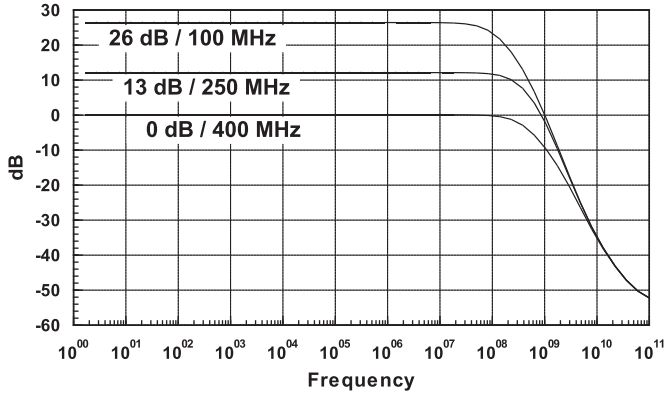

Fig. 13. Bode plot of the VGA.

from the feedback resistor used by the voltage regulator without additional cost to the implementation. M_{32} to M_{35} are used as replicas of transistors M_{18} to M_{21}, and M_{37} is used to sink a variable current identical to M_{23}. With the help of an error amplifier, V_{b4} is generated to bias M_{22} and M_{36} such that the drain node of M_{19} to M_{23} (V_{out}) and the drain node of M_{33} to M_{37} is regulated at $1/2V_{DD}$.

3. Simulation results

This design has been carried out using a 0.18 μm standard CMOS process with a layout occupying an area of 0.0024 mm^2 shown in Fig. 10. Simulations are carried out under all process, voltage, and temperature (PVT) corners with consideration of parasitic (resistances and capacitances) extracted using Calibre PEX. To prove the robustness of the AGC circuit, the worst case simulation result is summarized in the following text.

The AGC has a response time of 250 ns and is capable of detecting input signal amplitude and adjust the desired corresponding gain to provide constant signal amplitude within the range of 0–26.4 dB, as depicted in Fig. 11. The response time of 250 ns can be made even shorter by increasing the frequency of the Reset signal shown in Fig. 5 at the expense of extra power consumption. On the other hand, if the input signal amplitude does not vary in a fast fashion, the Reset signal can be made slower, or be event-driven by downstream digital circuits to conserve additional power.

The gain vs. gain control voltage relationship of the proposed Main and Auxiliary VGAs is plotted in Fig. 12. These VGAs consume a total of 77 μW when they are working at a gain of 26.4 dB and a bandwidth of 100 MHz. When the VGAs drop to a gain of 0 dB, their bandwidth is increased to 400 MHz, their total power consumption soars up to 400 μW. The Bode plot of the VGA at 0 dB, 12 dB, and 26.4 dB is shown in Fig. 13. The simulated THD of the VGA with its output targeted to be $0.95V_{p-p}$ at 1 MHz is −6.8 dB when a $1V_{p-p}$ input is applied, and −23 dB when a $0.1V_{p-p}$ input is applied. The in-band RMS noise is $62\mu V\sqrt{Hz}$ at 0 dB gain, and $441\mu V\sqrt{Hz}$ at 26 dB gain. It is apparent that the VGA is less noisy when consuming more current.

A tabulated comparison of this VGA along with other prior works is shown in Table 1. This table indicates that the proposed AGC has the largest output swing, the largest gain per stage, large input swing, fast response time, and wide bandwidth. To fairly compare the performance of the proposed AGC with those of other prior works in Table 2, the following figures of merit (FOM) are used for comparison:

$$\mathrm{FOM1} = \frac{\text{Tunable Gain} \times \text{Bandwidth}}{\text{Power Consumption} \times \text{Area}} (\mathrm{dB\,MHz/mW\,mm^2}) \quad (7)$$

$$\mathrm{FOM2} = \frac{\text{Tunable Gain} \times \text{Bandwidth} \times \text{Output Swing}}{\text{Power Consumption} \times \text{Area} \times V_{DD}} (\mathrm{dB\,MHz/mW\,mm^2}) \quad (8)$$

$$\mathrm{FOM3} = \frac{\text{Tunable Gain} \times \text{Bandwidth} \times \text{Output Swing} \times \text{Input Swing}}{\text{Power Consumption} \times \text{Area} \times V_{DD} \times V_{DD} \times \text{Response Time}} (\mathrm{dB/\mu s^2\,mW\,mm^2}) \quad (9)$$

Notably, the proposed design outperforms all prior works using every abovementioned FOMs.

Table 1
Transistor sizes.

Peak detector							
M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
2.2/0.18 μm	0.66/0.18 μm	0.66/0.18 μm	0.33/0.18 μm	0.66/0.18 μm	0.33/0.18 μm	0.22/0.18 μm	2.2/0.18 μm
Proposed VGA							
M_9	M_{10}	M_{11}	M_{12}	M_{13}	M_{14}	M_{15}	M_{16}
6.6/0.18 μm	1.76/0.18 μm	0.22/0.18 μm	3.52/0.18 μm	0.44/0.18 μm	4.4/0.18 μm	0.22/0.18 μm	1.1/0.18 μm
M_{17}	M_{18}	M_{19}	M_{20}	M_{21}	M_{22}	M_{23}	
4.4/0.18 μm	0.66/0.18 μm	0.66/0.18 μm	0.22/0.18 μm	0.22/0.18 μm	1.32/0.18 μm	0.44/0.18 μm	
Bias circuit for the VGA							
M_{24}	M_{25}	M_{26}	M_{27}	M_{28}	M_{29}	M_{30}	M_{31}
6.6/0.18 μm	1.76/0.18 μm	0.22/0.18 μm	3.3/0.18 μm	6.6/0.18 μm	1.76/0.18 μm	0.22/0.18 μm	3.3/0.18 μm
M_{32}	M_{33}	M_{34}	M_{35}	M_{36}	M_{37}		
0.66/0.18 μm	0.66/0.18 μm	0.22/0.18 μm	0.22/0.18 μm	1.32/0.18 μm	0.44/0.18 μm		

Table 2
Comparison with prior works.

	Proposed[a]	[2]	[6]	[7]	[8]	[9]
Gain (dB)	0–26	−8 to 32	2–24	−10 to 50	−10 to 17	0–22
Stages	1	2	3	2+1 CGA[b]	2	1
Bandwidth	100 MHz min	18 MHz	4 GHz	18 MHz min	1.25 GHz	100 MHz
Response time	250 ns	5.6 μs	200 ns	20 μs	1.6 μs	2.4 μs
Input swing	$\sim 1V_{p-p}$	N/A	60 mV V_{p-p}	1.8 V	550 mV V_{p-p}	N/A
Output swing	$1V_{p-p}$	500 mV V_{p-p}	400 mV V_{p-p}	0.75 V	160 mV V_{p-p}	N/A
Core area (mm^2)	0.0024	0.563	0.3844	0.45	0.0887	N/A
Supply voltage (V)	1	1.8	1.8	1.8	1.8	1.8
Power	530 μW	11.6 mW	84 mW	2.178 mW	43.2 mW	2.4 mW
Noise[a]	$62\mu V\sqrt{Hz}$	$77.5nV\sqrt{Hz}$	–	$21nV\sqrt{Hz}$	–	$44nV\sqrt{Hz}$
FOM1	2044025	110.2468	2725.336	612.1824	8807.779	N/A
FOM2	2044025	30.62412	605.6302	255.076	782.9137	N/A
FOM3	8176101	N/A	100.9384	12.7538	149.5148	N/A
Process (μm)	0.18	0.18	0.18	0.18	0.18	0.35
Year	2011	2008	2009	2010	2008	2010

[a] Simulated.
[b] Variable gain stage+1 constant gain stage.

4. Conclusion

In this study, we have presented a 1 V AGC circuit that features both an innovative AGC and peak detector design. A low voltage VGA with rail-to-rail input stage has also been proposed. The maximum power consumption of this AGC is 0.53 mW, with a minimum bandwidth of 100 MHz and with a dynamic range of 26.4 dB. By using the novel Parallel-Detect Singular-Store Peak Detector, the maximum response time of this AGC can be as short as 250 ns. Therefore, this AGC can be found to be very practical in many power-aware applications.

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