Temperature and Process Compensated Clock Generator Using Feedback TPC Bias

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***Abstract*—This paper proposes a temperature and process compensated clock generator using a feedback TPC (temperature and process compensation) bias circuit. With the proposed feedback TPC bias based on the OPA, MOS transistors and resistors, the BJT required in traditional bandgap bias circuit could be avoided. Thus, it is easy to be integrated with less area penalty. The proposed design is implemented using 0.25μm BCD process. According to the all-corners simulation results, the proposed clock generator processes the frequency diffusion error of 2.10% in the worst cases. Besides, the worst case duty cycle is simulated to be 48.93.%. The area of the chip is 0.1356 mm^2.**

Keywords— Clock generator, process, temperature, compensation

I. Introduction

A stable clock generator is critical in lots of systems, e.g., microprocessor [1], digital radio [2], biomedical device [3], [4]. In order to attain the stable clock signal, the clock generator must be immunity to the unideal environment parameters variation, e.g. the temperature variation and the process diffusion [5]- [7].

Kurit *et al.* presented a PLL-based clock generator to obtain a stable clock by removing the noise with the loop filter [1]. However, it requires an external clock source and it possesses the stable problem. Besides, it is sensitive to the process variation because of the analog components. Zhang *et al.* modified the PLL-based clock generator by an improved control loop to compensate the process variation [2]. However, it is sensitive to the temperature variation. Sundaresan *et al.* presented a process and temperature compensated clock generator based on a differential ring oscillator. However, it requires BJT transistors for temperature compensation such that it is difficult to be integrated using the CMOS process.

This paper proposed a feedback TPC (temperature and process compensation) circuit to compensate the temperature and process variation. It generates a voltage signal which is adjusted according to the temperature and process variation for the differential ring oscillator such that the output frequency is stable.

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II. Temperature and Process Compensation Clock Generator

Referring to Fig. 1, the proposed temperature and process compensated clock generator is composed of a Voltage regulator, a feedback TPC (temperature and process compensation) circuit, a replica bias circuit, a differential ring oscillator and a differential-to-single-end converter. The voltage regulator provides a regulated power signal, Vref, for other components to obtain a better PSRR. The feedback TPC circuit generates the required compensation voltage, Vcomp, for the differential ring oscillator. Vcomp is adjusted according to the temperature variation and the process diffusion such that a stable output frequency could be generated. The replica bias circuit receives Vcomp and generates a control signal, Vctrl, which follows the the variation of Vcomp. Thus, the differential ring oscillator is indirectly biased by Vcomp (= Vctrl) and the feedback TPC circuit is isolated from the noisy oscillator. Besides, Vcs is a bias voltage to generate an appropriate bias current for the differential ring oscillator. The differential-to-single-end converter receives the differential oscillated signal, Vop and Von, and output the single-end signal, Vout.

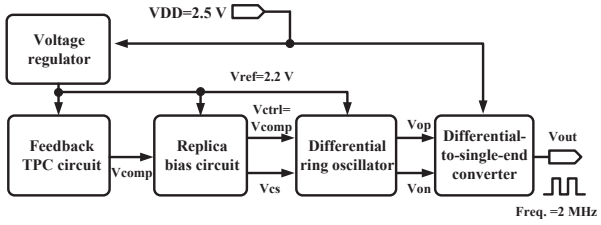

Fig. 1. Block diagram of the proposed temperature and process compensation clock generator.

A. Differential Ring Oscillator

Fig. 2 (a) shows the block diagram of the differential ring oscillator, which is composed of three delay stages, two dummy stages, and a buffer stage. The delay stage is a differential structure to reject the noise from the power lines and the substrate. The buffer stage provides the driving ability for the large capacitive load. The dummy stage is used to match the loads of stage1 and stage2 to the load of stage3,

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such that the linearity of the differential ring oscillator can be improved.

Fig. 2 (b) shows the schematic of the delay stage. M302 and M303 behave as the active loads of the delay stage to provide the large small-signal gain and the wide oscillation swing. M301 and M304 are the passive loads of the delay stage. They can provide great large-signal gain and a better PSRR (Power supply rejection ratio).

By simplifying the delay stage to be a RC model, the delay time of each delay stage can be given as

$$t_d \approx \frac{C_o \cdot (V_H - V_L)}{I_{ref}}, \tag{1}$$

where C_o is the equivalent capacitance at the output of each delay stage. V_H and V_L refer to the peak voltage of the oscillation signals, which is equal to the voltage, Vref and Vctrl, respectively. I_{ref} is the tail current in each delay stage.

Moreover, the frequency of the output signal is determined by the number of the delay stages. Thus, the frequency of the output signal, f, can be derived to be

$$f = \frac{1}{N \cdot t_d}, \tag{2}$$

where N refers to the number of the delay stages, which is 3 in this design.

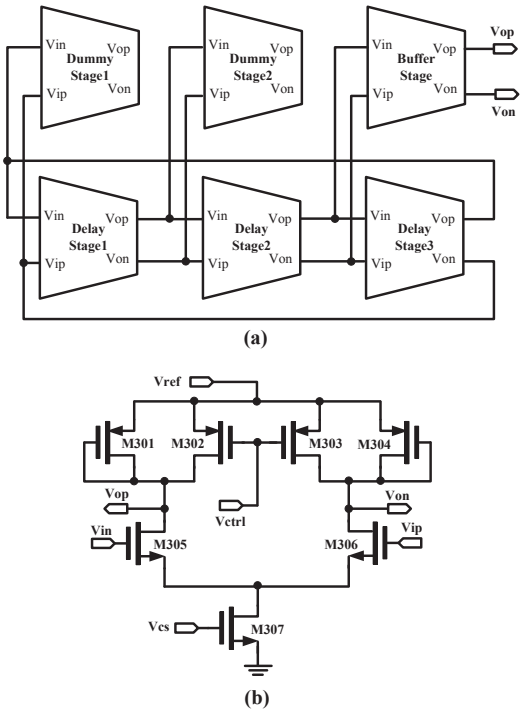

Fig. 2. Schematic of (a) the differential ring oscillator and (b) the delay stage.

B. Replica Bias Circuit

Fig. 3 shows the schematic of the replica bias circuit. M401, M402, M405, and M407 behaves as the half circuit of the delay stage. The compensation signal, Vcomp, is biased at the gate of the active load transistor, M401. With the negative feedback of the operational amplifier, OPA1, a bias signal, Vcs, is generated. Vcs is coupled to the gate of M407 to provide a bias current I_{ref} for M407 and M408. It results in that the bias current of M403 and M404 is the same with that of M401 and M402. Thus, the control signal, Vctrl, can trace the compensation signal, Vcomp.

According to the saturation current equation of the MOS transistor, the bias current, I_{ref}, could be given as

$$I_{ref} = K_{402}\frac{W_{402}}{L_{402}}(V_{ref} - V_{comp} - V_{T402})^2, \tag{3}$$

where $K_{402} = \mu_0 C_{ox}$. W_{402} and L_{402} are the width and length of the transistor M402. V_{T402} is the threshold voltage of M402.

By replacing Eqn. (1) and (2) into Eqn. (3), the frequency of the output signal can derived to be

$$f = K_{402}\frac{(W/L)(V_{ref} - V_{comp} - V_{T402})^2}{N \cdot C_o \cdot (V_{ref} - V_{ctrl})}, \tag{4}$$

According to Eqn. (4), the output frequency can be adjusted by the control signal, V_{ctrl}.

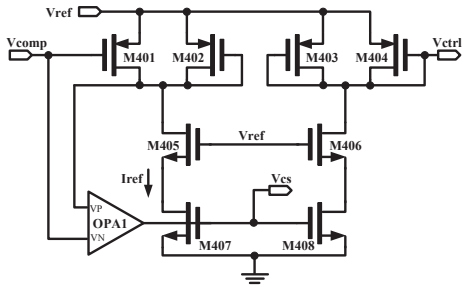

Fig. 3. Schematic of the replica circuit.

C. Feedback TPC Circuit

Fig. 4 shows the feedback TPC (temperature and process compensation) bias circuit. M501 $\sim$ M505 are the process sensor. M506 $\sim$ M512 construct to a single stage operational amplifier (OPA2). R501, R502 and M513 are the feedback circuit, which can compensate the process and temperature variation.

M501, M503, and M504 act as the current source generator, which provide the operating current for the feedback TPC circuit. M502 is a diode connected MOS transistor, which acts as a V_{T} sensor. The sensed voltage, V_{TP}, can be denoted as

$$V_{TP} = V_{ref} - |V_{SG502}|, \tag{5}$$

where V_{SG502} is the source-gate voltage of M502. When the process diffuses from the fast to the slow corner, the threshold voltage, V_{T502}, is increased such that the source-gate voltage, V_{SG502}, is increased. Thus, the voltage of V_{TP} is pulled down.

The decreased V_{TP} is coupled to the positive input node of OPA2. With the negative feedback loop, Vcomp can trace the variation of V_{TP}. As mentioned previously, Vctrl could trace Vcomp, which results in that Vctrl can traces V_{TP}. Thus, the

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effect of K_{402} and V_{T402} caused by the process diffusion in Eqn. (4) can be compensated.

When the temperature rises, the voltage of V_{T502} and V_{SG502} decrease. It results in that V_{TP} increases. Similarly, Vcomp and Vctrl increase with the risen temperature. Thus, the effect of the increased K_{402} and decreased V_{T402} is compensated by the increased Vctrl in Eqn. (4). Hence, the temperature variation is compensated.

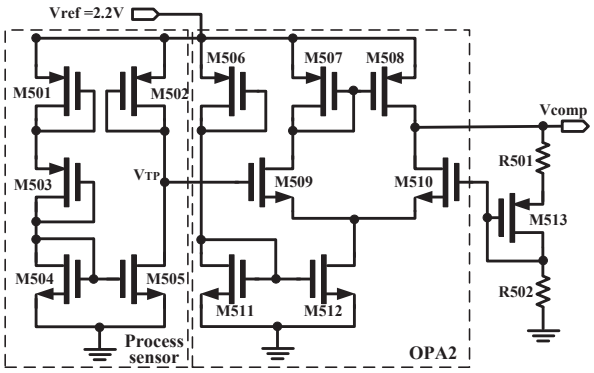

Fig. 4. Schematic of the proposed feedback TPC circuit.

D. Differential-to-single-end Converter

Fig. 5 shows the schematic of the differential-to-single-end converter. M601 $\sim$ M605 and M606 $\sim$ M607 behave as two single stage voltage comparators CMP1 and CMP2, respectively. The input differential oscillation signals, VIP and VIN, are coupled to the negative node and the positive node of CMP1, respectively. Moreover, VIP and VIN are coupled to the positive node and the negative node of CMP2, respectively. The outputs of CMP1 and CMP2 are connected to the gate of M611 and M613, respectively. With the comparison of CMP1 and CMP2, and the current mirror of M612 and M614, a single-end signal, Vsingle, is generated. Besides, by adjusting the size of M611 $\sim$ M614, the duty cycle of Vsingle is close to 50%. Vsingle is then buffered and the output signal Vout is obtained.

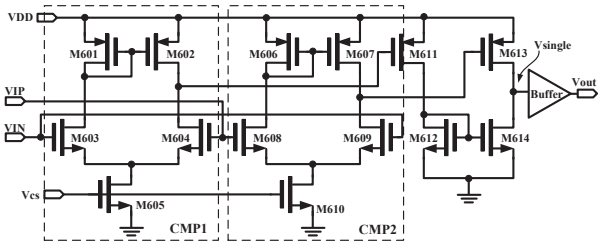

Fig. 5. Schematic of the differential-to-single-end converter.

E. Voltage Regulator

Fig. 6 shows the schematic of the voltage regulator, which is composed of a start-up circuit, a cascoded beta-multiplier bias circuit, an error amplifier, the pass transistor M720, the compensated capacitor C701, and the feedback resistors R702 and R703. With the large voltage gain of the error amplifier, the PSRR can be increased. With the compensation capacitor, the bandwidth of the voltage regulator can be improved. Besides, the feature size of the pass transistor is large to reduce the dropout voltage.

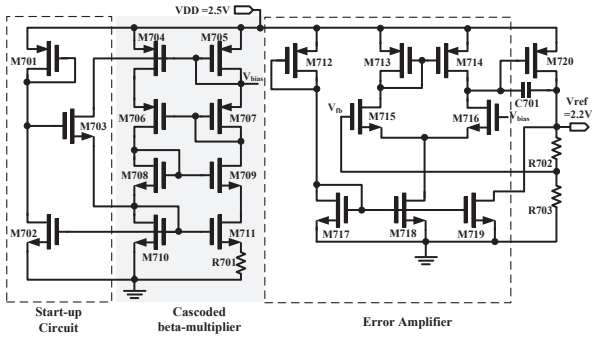

Fig. 6. Schematic of the regulator circuit.

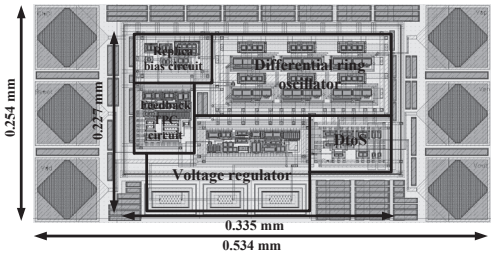

Fig. 7. Layout of the proposed temperature and process compensated clock generator.

III. Implementation and Simulation

The proposed temperature and process compensation clock generator is carried out using 0.25μm BCD process. Fig. 7 shows the layout of the proposed design. The chip area is 0.254×0.534 mm^2. Fig. 8 (a) shows the simulated waveform of Vout at the corner of [TT, 35^{o}C]. The frequency of Vout is 2.036 MHz and the duty cycle is 50.24%. Fig. 8 (b) shows the simulated voltage of Vcomp in different process corners. Vcomp increases with the risen temperature. Referring to Fig. 9, the output frequency error is reduced from -24% to -1.95% by using the compensation circuit. Fig. 10 shows the frequency error simulated in all corners. The worst case of the frequency error is 2.10% at the corner of [SS, 100^{o}C]. Fig. 11 shows the duty cycle of Vout in different corners. The worst case of the duty cycle is 48.93.% at the corner of [TT, 80^{o}C]. Table I reveals the specification comparison with prior works. The proposed design possesses the best performance on the frequency error. Besides, a FOM (Figure-of-merit) = $\frac{\text{Temp. Range}}{\text{Frequency error}}$ is given, which reveals that the proposed design possesses the best result by considering the temperature range and the frequency error.

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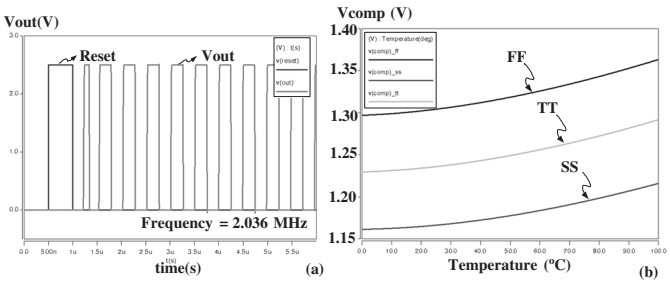

Fig. 8. Simulated waveform of (a) the output signal Vout at the corner of TT, 35^{o}C and (b) the compensation voltage, Vcomp, at TT, FF and SS corners with temperature varied from 0^{o}C to 100^{o}C.

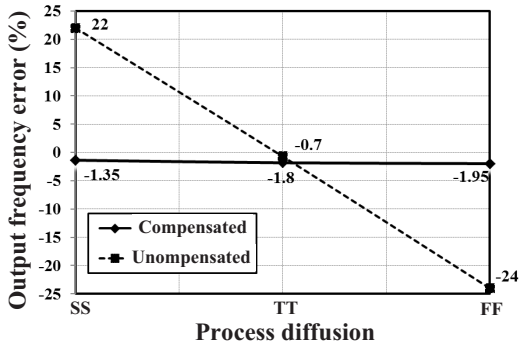

Fig. 9. Compensated and uncompensated output frequency error in TT, FF and SS corners.

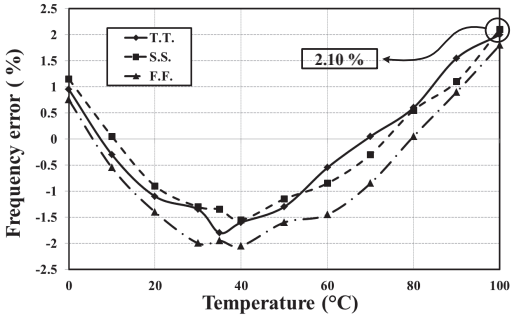

Fig. 10. Simulated frequency error in TT, FF, and SS corner with temperature from 0^{o}C to 100^{o}C.

IV. Conclusion

A temperature and process compensation clock generator is proposed in this paper. By using the feedback TPC circuit and the replica bias circuit, the frequency error is simulated to be 2.10% in the worst case of [SS, 100^{o}C] corner. With the differential-to-single-end converter, the duty cycle is simulated to be 48.93% in the worst case.

Acknowledgment

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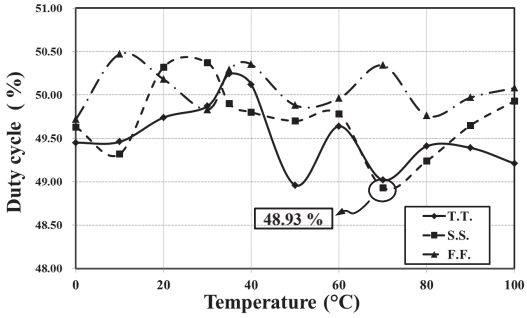

Fig. 11. Schematic of the regulator circuit.

	This work	[2]	[6]
Process	0.25μm BCD	90nm CMOS	0.18μm CMOS
Supply voltage (V)	2.5	1.0	1.8
Output frequency	2.0 MHz	3000 MHz	130 MHz
Frequency error	$\pm$2.10%	$\pm$11.14%	$\pm$4.99%
Temp. Range (^{o}C)	0$\sim$100	-50$\sim$100	0$\sim$100
Duty cycle	50% $\pm$1.07%	N/A	50.23%¶
Chip Area (mm^2)	0.1356	N/A	0.1521
Core Area (mm^2)	0.076	N/A	0.0042
Power (mW)	0.64	2.55	2.74
Publication	ICICDT	ISCAS	ISNE
Year	2012	2009	2010
FOM†	47.62	13.46	20.04

Note: ¶ The duty cycle is simulated at the typical corner.
† FOM = $\frac{\text{Temp. Range}}{\text{Frequency error}}$.

TABLE I
Comparison with several prior works

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