A Reconfigurable 16-channel HV Stimulator ASIC for Spinal Cord Stimulation Systems

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***Abstract*—A 16-channel stimulation waveform generator ASIC using high voltage CMOS technology to generate high voltage stimulation signals for Spinal Cord Stimulation (SCS) systems is presented in this study. To enlarge the voltage swing on high-impedance electrodes, the output stage of the proposed for the SCS systems is implemented on silicon using a 0.25 μm high-voltage (60 V) devices. Particularly, a charge pump composed of 5 cascaded voltage doublers is used to boost the core voltage (2.5 V) to higher than 10 V required by the SCS systems to execute electrical stimulation therapy [1]. A total of 16 stimulation waveform generators are included to drive 16 sets of electrodes, where each generator is composed of an HV operational amplifier and an HV analog switch. Compared with existing commercial products, the proposed SCS system attains better flexibility to meet the spinal cord stimulation high voltage demand in addition to the reduction of cost and PCB size.**

***Index Terms*—spinal cord stimulation (SCS), 16-channel stimulation waveform generator, high-voltage process**

I. Introduction

MANY implantable electronic devices intended for restoring deficient functions of human have been reported in recent years. Particularly, implantable stimulators are used for pain relief or even pain killing, e.g., SCS. Statistically, more than 14,000 people per year have implanted SCS devices to stop or at least reduce pain caused by different problems. The number has been found to grow significantly every year [1]. Compared with the conventional medicine-based approach, SCS attains the following main advantages: 1. no side effects; 2. mobile and convenient; 3. low cost; 4. no need to carry pain-killing medicine all the time; 5. very effective. However, currently available SCS devices still have many problems, including large size, short operating time, etc. Moreover, SCS systems require at least 10 V to drive the electrodes as well as the nerve trunks, logic-based semiconductor technologies can not provide such a high voltage swing. Thus, many off-chip power devices must be used such that the PCB size of the SCS systems can not be reduced significantly to a comfortable size for human. Considering the above factors, this study presents a 16-channel HV stimulation waveform generator with the programmable control mechanism carried out by a HV CMOS process to resolve the mentioned difficulties and meet the SCS demand.

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II. HV ASIC for implantable electrical stimulation system

Fig. 1 shows the basic operation of an SCS system, where the electrode array is installed in the epidural space of the spinal cord, while a pulse generator (PG) is installed in the abdominal by surgery. This paper proposes an HV Application-Specific Integrated Circuit (ASIC) in the PG to carry out the generation of high voltage stimulation signals. Typically, the stimulating pulses generated by the PG must at least have three kinds of stimulation modes, mono-, bi-, and tripolar [2]. Besides, the PG usually has four adjustable settings for these three modes as follows.

1) Pulse amplitude: Setting the threshold voltage of the stimulation signal.
2) Pulse width: Setting the stimulated coverage size of the pain area.
3) Stimulation rate: Setting the stimulation impulse time per second.
4) Channel selection: Selecting the output channels of electrodes.

The pulse generator surgically placed under skin delivers an electrical current or voltage via a lead to electrodes coupled with the spinal. When the pulse generator is turned on, it feels like a mild tingling in the pain area. All of the circuits, decoder, PG and peripheral circuits, are expected to be realized on silicon to reduce the size and volume of the implant [3].

TABLE I
Specifications of the stimulation waveform parameters

Field	Range	Bit width
Amplitude	0.0 V $\sim$ 10.5 V	8 bits
Rate	2 Hz $\sim$ 1200 Hz	7 bits
Pulse width	60 μs $\sim$ 1000 μs	7 bits
Stimulation type	4	2 bits
Dose time	0.1 sec $\sim$ 30 min	7 bits
Dose lockout time	0.5 sec $\sim$ 15 sec	5 bits

HV ASIC: As depicted in Fig. 2, the proposed HV ASIC is include 4 subcircuits, i.e., a Charge pump, an 8-bit DAC (Digital to Analog Converter), a 16-channel Sample and Hold circuit (S/H), and Stimulation waveform generators (0$\sim$15). The details of each function block is described as follows.

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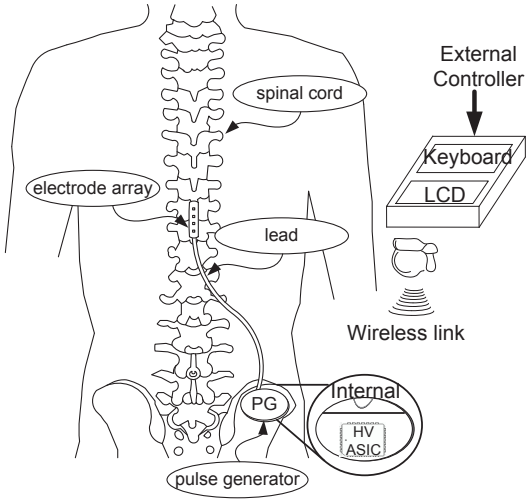

Fig. 1. The spinal cord stimulation scenario [1]

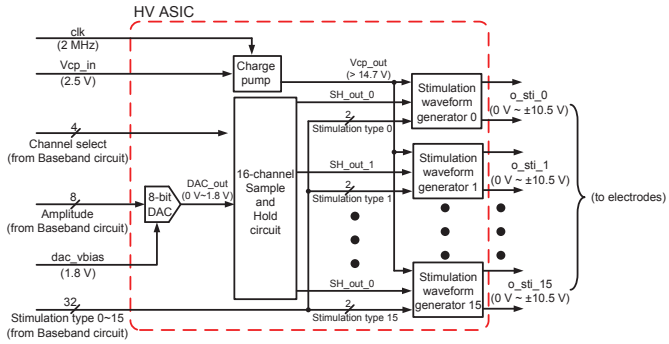

Fig. 2. Block diagram of the proposed 16-channel stimulator.

A. Charge pump circuit

Charge pump in Fig. 2 takes advantage of the well-known Dickson architecture to generate a voltage large than VDD [4]. It is composed of 5 cascaded voltage doublers, as shown in Fig. 3 (a), where the 2.5 V input voltage is elevated to be over 14.7 V theoretically. The voltage doubler schematic is then shown in Fig. 3 (b). The output voltage of the first voltage doubler is as follows.

$$(\text{Vcp\_cell}(1)\text{\_out}) = (\text{Vcp\_cell}(1)\text{\_in}) + (\text{V\_clk}) \qquad (1)$$

If the input signal voltage (Vcp_cell(1)_in), equals to the signal voltage (V_clk) of Clock Generator (not shown), the maximum output voltage of the first cell will be ideally boosted to the following voltage provided that the threshold voltage drop is ignored.

$$(\text{Vcp\_cell}(1)\text{\_out}) = 2 \times (\text{Vcp\_cell}(1)\text{\_in}) \qquad (2)$$

By a similar derivation, the 5 cascaded voltage doublers will theoretically boost the stimulation voltage larger than 14.7 V.

B. Digital to Analog Convertor(DAC)

The binary-weighted current steering DAC in Fig. 4 generates a current, which is converted into a reference

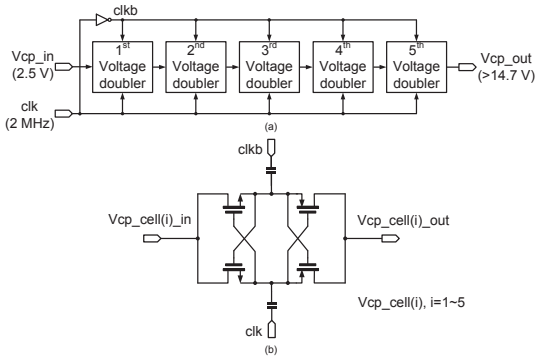

Fig. 3. Schematic of (a) five cascaded voltage doublers; (b) a voltage doubler.

voltage by a resistor and a unit-gain buffer. The unit-gain buffer will then deliver a voltage level proportional to its own input current for the following S/H. Notably, the DAC design is composed of a set of 8 current sources activated by a binary word sent from Baseband circuit (not shown). Meanwhile, we can tune the voltage biasing (dac_vbias) through an off-chip device setup.

C. 16-channel Sample and Hold circuit (S/H)

As soon as the Baseband circuit provides 4-bit channel select signals to select one of the 16-channel S/H circuits as shown as in Fig. 5, where a 4-to-16 decoder is needed. Notably, one dummy switch transistor is employed to avoid the problem of charge injection [5]. This 4-to-16 decoder also generates true and complementary pair for each channel to enable the selected one. There are 16 S/H circuits, each of which corresponds to one channel. Notably, the selected channel utilizes the corresponding S/H circuit to store the voltage from DAC_out, which will then be fed into the corresponding Stimulation waveform generator.

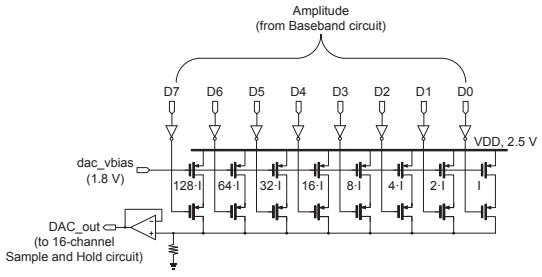

Fig. 4. Schematic of the 8-bit current-steering DAC.

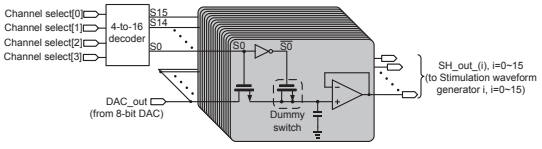

Fig. 5. 16-channel Sample and Hold circuit.

D. Stimulation waveform generators

The proposed stimulation waveform generator which is composed of HV Operational Amplifier and HV analog switch circuit as shown in Fig. 6. It is in charge of generating high voltage stimulation signals to meet the spinal cord stimulation demand. When the channel is enabled, the S/H circuit send a voltage of 0 $\sim$ 1.8 V (SH_out) to HV OPA which will proportionally raise to 0 $\sim$ 10.5 V. To cope with different demands of clinical usage or experiments, the stimulating pulses including different stimulation types must be able to be provided by the PG. We take advantage of the HV devices provided by HV CMOS process to carry out High Voltage Operational Amplifier (HV OPA) and High Voltage analog switch for the required stimulation function. The details of each subcircuits are described as follows.

1) HV Operational Amplifier: The HV OPA is a multiple-voltage level-converting amplification stage capable of converting an analog voltage signal from the circuits in the low voltage device domain and amplifying it into the high voltage device domain, as shown in Fig. 7 [6]. The HV OPA includes two parts: an amplifier based on low voltage device and an output stage consisting of high voltage devices. The P- and N- different pair, and Bias circuit on the left hand side of Fig. 7 are low voltage devices to generate a voltage Vx, while the output with a stage is a Common Source amplifier to provide an output with a swing as high as Vcp_out. Notably, HP1, HP2, HN1, HN2 are HV PMOS and NMOS, respectively, while Rz and Cc are used for a better step response of the HV OPA.

2) HV analog switch circuit: Fig. 8 shows the High Voltage analog switch circuit. An illustration of the stimulation is demonstrated in Fig. 9 (a), where a positive stimulation is shown. When Stimulation type i[0] is from low to high, the low voltage transistor LN1 and high voltage transistor HN22 are turned on. Thus, the gate drive of HP21 is dropped and turned on. Then, HV OPA output delivers a stimulation current from HP21 through the electrodes on spinal cord to HN22. This stimulation current from o_sti_i[0] node flowing through the spinal cord to o_sti_i[1] is defined as positive stimulation. By contrast, when Stimulation type i[1] changes from low to high, the low voltage transistor LN2 and high voltage transistor HN21 are on to trigger a reverse current as shown in Fig. 9 (b). That is, the HV OPA delivers a current from HP22 through o_sti_i[1] to o_sti_i[0]. Hence, this scenario is defined as the negative stimulation, where o_sti_i[0] is the lower voltage, and o_sti_i[1] is the higher voltage.

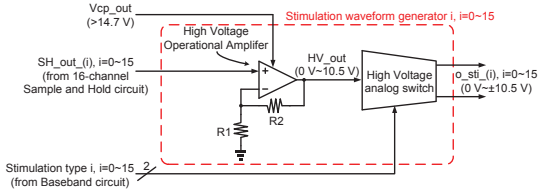

Fig. 6. Schematic of Stimulation waveform generators.

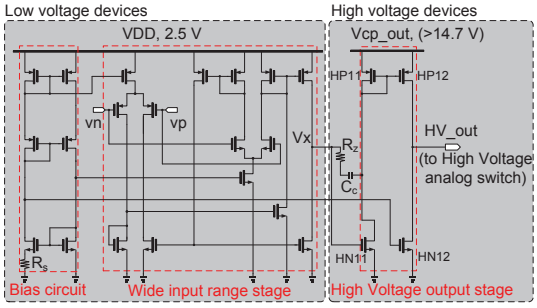

Fig. 7. Schematic of High Voltage Output stage Operational amplifier.

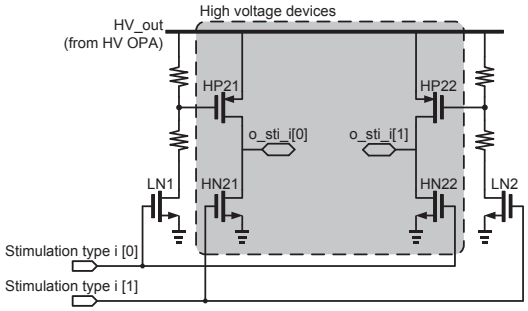

Fig. 8. Schematic of High Voltage analog switch.

III. Simulation and Verification

The proposed ASIC is carried out using the TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 μm high-voltage (60 V) CMOS process. Fig. 10 shows the layout view of proposed 16-channel HV stimulator HV ASIC design, where the area is 2862×1900 (μm^2). Fig. 11 demonstrates the worst-case simulation of the output voltage, when all 16 channels are turned on at the operation frequency = 1200 Hz. Notably, 1200 Hz is the highest stimulation frequency required by SCS system [1]. The Vcp_out voltage drops slightly from the expected 14.7 V to 13.08 V due to the charge pump loading effect [7]. Such a voltage drop will be proportional to the total number of selected channels. Notably, the expected

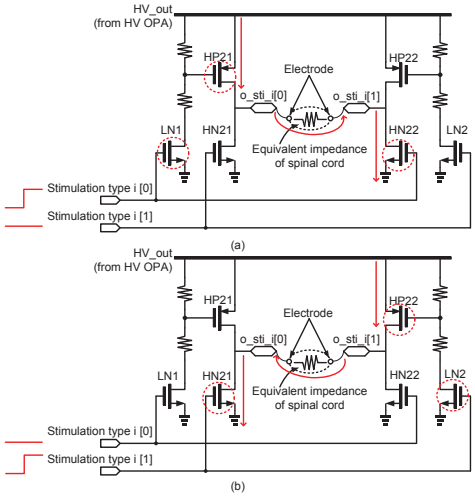

Fig. 9. Analog switch circuit with negative stimulation waves generators.

stimulation at the first channel in such a worst case, o_sti_0, is as high as 10.5 V regardless the positive (stimulation type 0[1]) or negative(stimulation type 0[0]). Table II reveals the specification comparison with prior works. Particularly, compared with our previous work [9], which used the discretes to provide SCS stimulation high voltage as shown in Fig. 12, where the area of the PCB is 5.8×5.5 (cm^2). The proposed design totally eliminates these discretes by integrating all HV analog circuits into one chip. In other words, the proposed HV ASIC integrated on silicon without any discrete significantly reduces the size of SCS implants.

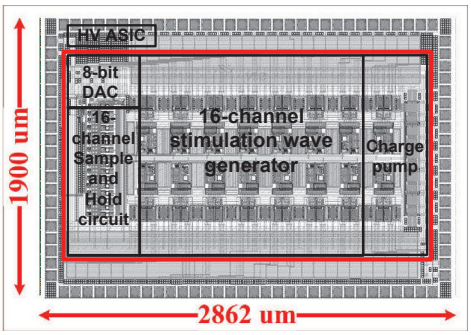

Fig. 10. Layout view of 16-channel HV stimulator HV ASIC for SCS circuit.

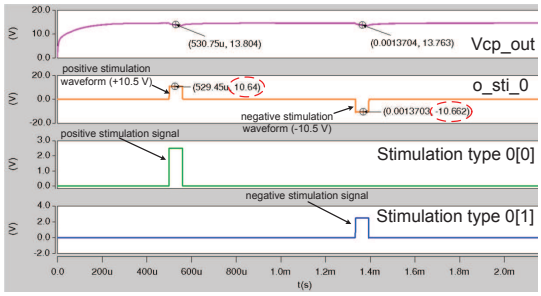

Fig. 11. Output voltage 16-channel HV stimulation wave generators.

IV. Conclusion

A multiple-stage operational amplifier dedicated for voltage level converting and amplification with HV analog switches is designed and proved to provide 16-channel HV stimulations in this HV ASIC design for SCS systems. The proposed HV ASIC is considered as a total solution for any SCS implant to be the HV frontend in charge of HV stimulation voltage generation.

Acknowledgement

This investigation is partially supported by National Science Council under grant NSC 99-2221-E-110-081-MY3, NSC 99-2923-E-110-002-MY2, and EZ-10-09-44-98. It is also partially supported by Metal Industries Research Development Centre (MIRDC) and Ministry of Economic Affairs, Taiwan, under grant 100-EC-17-A-01-1010. The authors would like to express their gratefulness to Chip Implementation Center of National Applied Research Laboratories, Taiwan, for their thoughtful chip fabrication service.

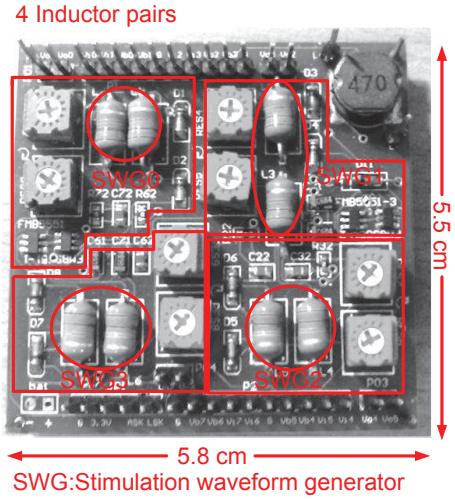

Fig. 12. SCS implant frontend using off-chip discretes. [9]

TABLE II
Comparison of the commercial SCS systems

Device	proposed	[8]	[9]
Process	0.25 μm	0.18 μm	0.18 μm
Amplitude (V)	0.0 $\sim$ 10.5	0.0 $\sim$ 2.98	0.0 $\sim$ 10.5
Number of channels	16	16	4
Stimulation type	voltage	voltage	voltage
Stimulation current	525μA	136μA	200μA
Power/channel	5.4 mW	0.06 mW	2.13 mW
Programmable mode	Yes	No	Yes
Stimulation Freq. (Hz)	2 $\sim$ 1200	N/A	2 $\sim$ 150
Number of discretes	0	N/A	$>$ 30
Die size	5.43 (mm^2)	8.96 (mm^2)	32 (cm^2)(on PCB)
Year	2012	2009	2011

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