Linear Programmable Gain Amplifier Using Reconfiguration Local-Feedback Transconductors

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***Abstract*—This paper proposes a linear PGA (programmable gain amplifier) using reconfiguration local-feedback transconductors for a FPW (flexural plate-wave) allergy biosensor. By using the LFT (local-feedback transconductors), the transconductance of the proposed PGA is linear against the input voltage. By using the proposed reconfiguration methods, the transconductance behaves as the pseudo-exponential approximation function of the digital control bits. Thus, the gain error of the linear PGA is simulated to be 0.25 LSB with dynamic gain range of 45.13 dB (-24.17∼20.96 dB). The proposed linear PGA is implemented by using a typical 0.18 μm CMOS process. The power consumption is 9.59 mW for 20 pF capacitive load at 20 MHz. The core area of the proposed design is 0.838×0.838 mm^2.**

***Index Terms*—FPW, biosensor, programmable gain amplifier, linear, gain error, and gain range.**

I. INTRODUCTION

Programmable gain amplifier (PGA) is an important component in lots of systems, e.g., hearing aids [1], wireless communication systems [2]-[4] to obtain a large dynamic range. In a FPW (flexural plate ware) allergy biosensor system, the PGA is to amplify the output of the FPW allergy biosensor, which generates a 20 MHz sinusoidal signal with its amplitude dependent on the concentration of the immunoglobulin E (IgE), as shown in Fig. 1 [5], [6]. The amplified signal is detected by a voltage peak detector and then converted to digital word by an ADC. In order to increase the precision of the FPW allergy biosensor system, it requires a linear PGA with the gain error less than 0.5 LSB.

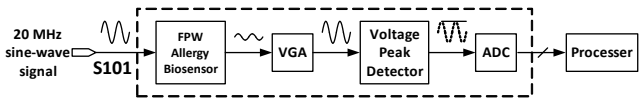

Fig. 1. FPW allergy biosensor system.

There were several methods presented for the implementation of the PGA. The first method is to use the OPA and the variable resistor feedback network, which results in the voltage gain insensitive to process variation [7]. After that, the CDN (Current division network) is then introduced to avoid the loading effect caused by the resistor feedback network [8]. Variable G_m [9] and variable output loads [10] are another popular structures for PGA. However, the voltage gain suffers from the unwanted effects due to the process and temperature variation. Local-Feedback transconductor (LFT) is then presented to obtain a process and temperature immunity variable gain without the loading effect [11]. In order to improve the linearity of the PGA, the reconfiguration structure is presented [2], [3]. However, these prior works can not provide a gain error less then 0.5 LSB, such that they can not be applied to the FPW allergy biosensor system.

Therefore, this paper proposes a linear programmable gain amplifier for the FPW allergy biosensor system. By using the local-feedback transconductors in a modified reconfiguration structure, the gain error of the linear PGA is simulated to be 0.25 LSB. Besides, the dynamic gain range is 45.13 dB (-24.17 $\sim$ 20.96 dB).

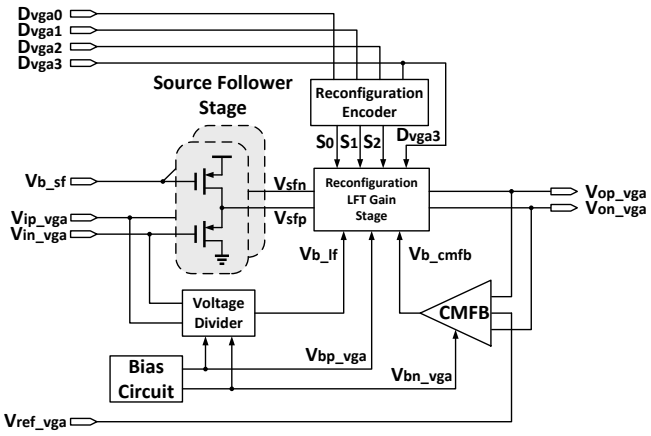

Fig. 2. Schematic of the proposed linear PGA.

II. LINEAR PGA USING RECONFIGURATION LFT

Fig. 2 shows the schematic of the proposed linear PGA, which is composed of a Source Follower Stage, a Reconfiguration Encoder, a Reconfiguration LFT Gain Stage, a Voltage Divider, a Common-Mode Feedback (CMFB) Circuit, and a Bias Circuit.

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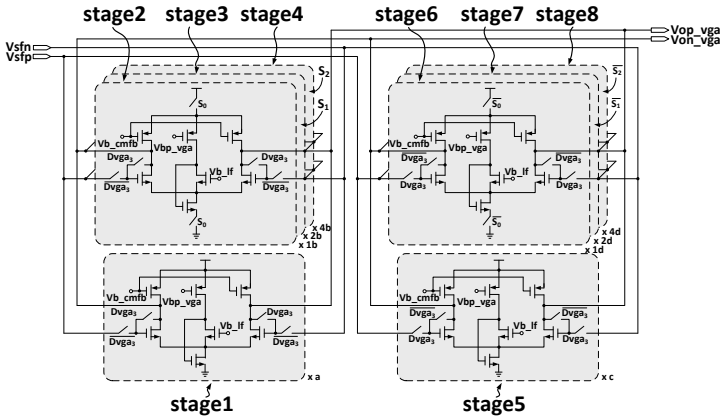

Fig. 3. Schematic of the reconfiguration LFT (local-feedback transconductors) gain stage.

A. Reconfiguration LFT Gain Stage

Fig. 3 reveals the schematic of the reconfiguration LFT gain stage. It is composed of 8 LFT stages (stage1 $\sim$ stage8) enclosed in the dashed line. According to the digital control signals, D_{vga3}, S_2, S_1, and S_0, the LFT stages change their configuration to accomplish a pseudo-exponential approximation function, $e^{2x} \cong (1+x)/(1-x)$ for the system transconductance, G_m. When D_{vga3} = logic 1 (= 3.3 V), stage1 $\sim$ stage4 become the gain stages and stage5 $\sim$ stage6 behave as the load stages, as shown in Fig. 4 (a). By setting the aspect ratio (W/L) for stage1 to stage8 to be the values of a, 1b, 2b, 4b, c, 1d, 2d, and 4d, respectively, the system G_m can be derived to be

$$G_m = \frac{G_{m,\text{gain stage}}}{G_{m,\text{load stage}}} = \frac{G_{ma}+G_{mb}}{G_{mc}+G_{md}}$$

$$= \frac{a+b\left(2^0\times S_0+2^1\times S_1+2^2\times S_2\right)}{c+d\left(2^0\times \overline{S_0}+2^1\times \overline{S_1}+2^2\times \overline{S_2}\right)}, \quad (1)$$

where G_{ma} and G_{mc} are the transconductances of stage1 and stage5, respectively. G_{mb} refers to the equivalent transconductance for stage2 $\sim$ stage4. G_{md} is the equivalent transconductance of stage6 $\sim$ stage8. $S_0 \sim S_2$ are the digital control signals to adjust the tail current of stage2 $\sim$ stage4 and stage6 $\sim$ stage8.

When D_{vga3} = logic 0 (= 0 V), stage1 $\sim$ stage4 become the load stages and stage5 $\sim$ stage6 become the gain stages. Thus, the system transconductance G_m is given by (2)

$$G_m = \frac{G_{m,\text{gain stage}}}{G_{m,\text{load stage}}} = \frac{G_{mc}+G_{md}}{G_{ma}+G_{mb}}$$

$$= \frac{c+d\left(2^0\times \overline{S_0}+2^1\times \overline{s_1}+2^2\times \overline{S_2}\right)}{a+b\left(2^0\times S_0+2^1\times S_1+2^2\times S_2\right)}. \quad (2)$$

According to equation (1) and (2), the variation of the system transconductance has better linearity against the control bits, $D_{vga3} \sim D_{vga0}$, as shown in Fig. 4 (b).

Besides, by setting V_{b_lf} to be (V_{sfp}+V_{sfn})/2, the transconductance of each reconfiguration LFT gain stage (G_{m_lft}) can be adjusted by the drain current I_{D247}, which is expressed as

$$G_{m\_lft} = 2\sqrt{I_{D247}\times\beta}, \quad (3)$$

where β denotes the transconductance parameter of the MOS transistor. Equation (3) reveals that the transfer charactenstic of G_{m_lft} is linear against the input voltage [11].

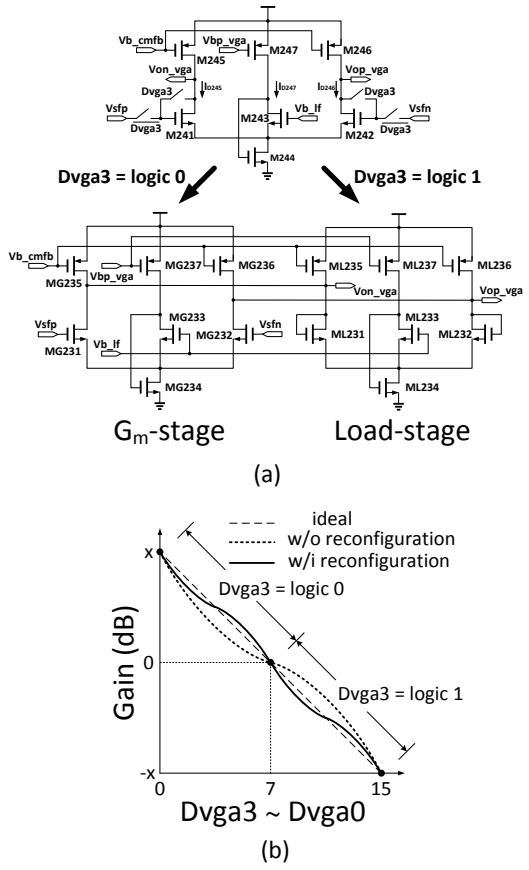

Fig. 4. (a) Operation reconfiguration LFT stage, and (b) the transition curves.

B. Reconfiguration Encoder

In order to obtain the linearity mentioned in subsection A, it needs a reconfiguration encoder for the digital signals ($D_{vga3} \sim D_{vga0}$). The reconfiguration encoder is composed of three exclusive OR gates, which generate the required control signals

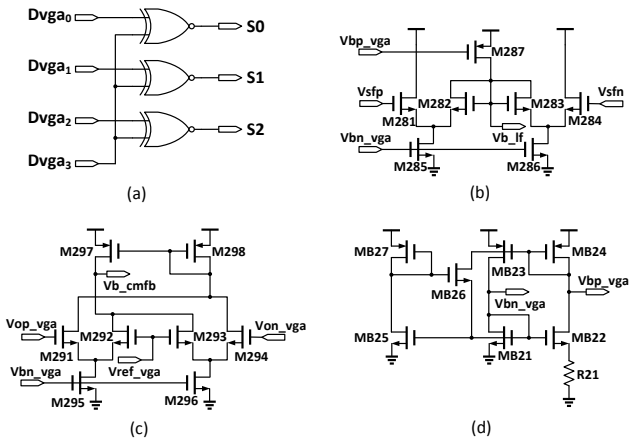

Fig. 5. Schematics of (a) the reconfiguration encoder, (b) the voltage divider, (c) the CMFB, and (d) the bias circuit.

$S_0 \sim S_2$ for the reconfiguration LFT stages, as shown in Fig. 5 (a).

C. Active Voltage Divider

The reconfiguration LFT stages require a bias voltage, V_{b_lf}, equivalent to $(V_{sfp}+V_{sfn})/2$, to provide the required DC operation voltage. It can be obtained by using an active voltage divider, as shown in Fig. 5 (b)

D. Common-Mode Feedback (CMFB) Circuit

The reconfiguration LFT stage requires a CMFB (Common-Mode Feedback) circuit to sense the output signals, V_{op_vga} and V_{on_vga}, and provide a bias voltage, V_{b_cmfb}, as shown in Fig. 5 (c). With the CMFB circuit, V_{op_vga} and V_{on_vga} are clamped at a stable bias voltage, V_{ref_vga}, as shown in Fig. 5 (b).

E. Bias Circuit and Source Follower Stage

Fig. 5 (d) reveals the schematic of the Bias Circuit. MB21 $\sim$ MB24 and R21 are the Beta-multiplier bias, which generates two bias voltages, V_{bp_vga} and V_{bn_vga} for the reconfiguration LFT stages. MB25 $\sim$ MB27 are the start-up circuit. Besides, the proposed design requires two source follower stages, which receive the input signals V_{ip_vga} and V_{in_vga}, respectively. Two level shifted output signals, V_{sfp} and V_{sfn}, are then generated. Thus, the input signals with zero DC voltage components, V_{ip_vga} and V_{in_vga}, generated by the FPW allergy sensor, could be received successfully.

III. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The proposed PGA is fabricated using a typical 0.18 μm standard CMOS process. The layout is shown in Fig. 6. The chip area is 0.838×0.838 mm^2 and the core area is 0.198×0.163 mm^2 where the area of the Buffers is not included. Fig. 7 shows the simulated transconductance of the local-feedback transconductors and the conventional transconductors, which is composed of the transistors M241, M242, and M244 in Fig. 4 (a). It reveals that the G_m of the local-feedback transconductor is less susceptible to the amplitude of the input voltage. Thus, the transconductance of the LFT stage has better linearity against the input voltage than the conventional transconductor. Fig. 8 shows the simulated frequency response for the proposed linear PGA. The voltage gain is varied from -24.17 dB to 20.96 dB, according to the digital control signals $D_{vga3} \sim D_{vga0}$ varied from 1111 to 0000. The -3 dB bandwidths is 66.28 MHz for the worst case (D_{vga3} - D_{vga0} = 0000). Fig. 9 shows the simulated voltage gain and gain error against the control bits. The dynamic gain range is 45.13 dB (-24.17 $\sim$ 20.96 dB). The worst gain error is less than -0.74 dB.

Table I reveals the specifications of the proposed linear PGA compared to the prior works. In order to compare the linearity, the gain error could be normalized to be the LSB by dividing by the gain step. The gain error of the proposed PGA is only 0.25 LSB, which is the smallest value in Table I. Besides, a FOM (Figure of Merit) is provided to reveal the performance compared to the prior works. It shows that the proposed design possesses the best performance by considering the gain range, the stage number and the gain error, simultaneously.

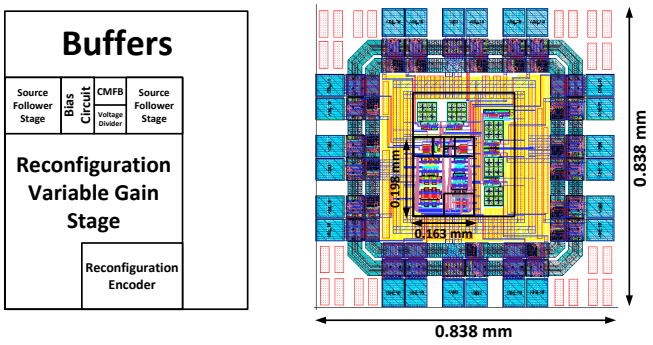

Fig. 6. Layout of the proposed linear PGA.

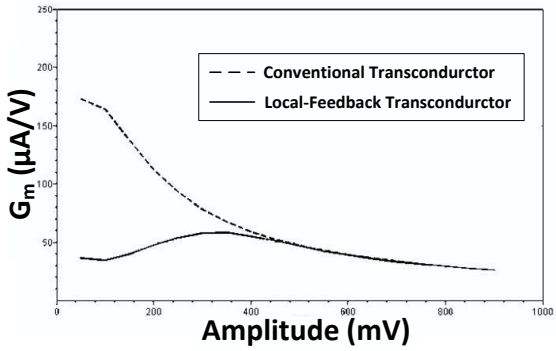

Fig. 7. Simulated transconductance of the local-feedback transconductors and the conventional transconductors.

IV. CONCLUSION

In this paper, a linear PGA is proposed. By using the local-feedback transconductors reconfiguration, the transconductance of the proposed PGA is linear against the input voltage and the control signals. The worst gain error is simulated to be 0.25 LSB. Besides, the -3 dB bandwidth is 66.28 MHz. Moreover, the gain range is 45.13 dB (-24.17 $\sim$ 20.96 dB).

TABLE I
COMPARISON BETWEEN THE PROPOSED DESIGN AND PRIOR WORKS

	This work	[1]	[2]	[3]	[4]
Year	2012	2008	2009	2010	2010
Process (μm)	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Power Supply (V)	1.8	1.8	1.5	1.8	1.8
Gain Range (dB)	45.13	42	42	21	53
Gain Step (dB)	3.01	1.31	1.31	1.3125	1
Bandwidth (MHz)	66.28	84	60	270	65
Gain Error (dB)	<0.74 (0.25 LSB)	<0.55 (0.42 LSB)	<0.54 (0.41 LSB)	<0.33 (0.23 LSB)	<0.5 (0.50 LSB)
Power Dissipation (mW)	9.59¶	1.4	3.2	2.34	2.16
Core Area (mm^2)	0.032	0.05	0.078	0.04	0.385
Chip Area (mm^2)	0.702	N/A	N/A	N/A	N/A
Stages	1	1	1	1	3
FOM §	183.57	100.03	101.89	90.58	35.33

Note: ¶ The power dissipation is simulated including the buffer for a 20 pF capacitance load. It is only 4.96 mW if the buffer is not included.

§ $\text{FOM} = \frac{\text{Gain Range}}{(\text{Stage number})[\text{Gain Error(LSB)}]}$

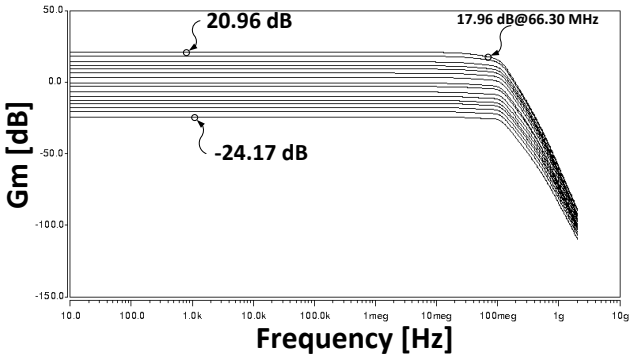

Fig. 8. Simulated frequency response of the system G_m with different digital control signals, $D_{vga3} \sim D_{vga0}$.

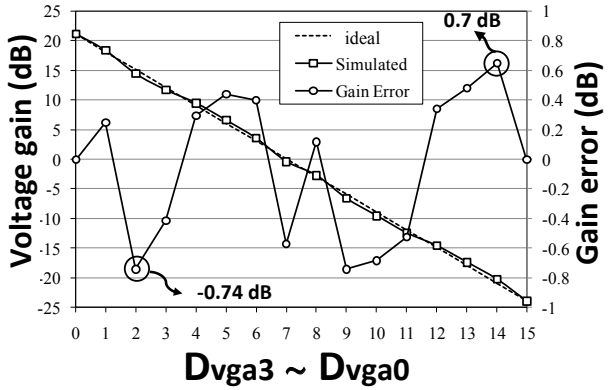

Fig. 9. Simulated gain and gain error versus the digital control word.

V. ACKNOWLEDGEMENT

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