A Delay-based Transceiver with Over-current Protection for ECU Nodes in Automobile FlexRay Systems[1]

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***Abstract* –This work presents a FlexRay Transceiver (FRT) used in an in-vehicle network compliant with the latest FlexRay physical layer standards. The proposed FRT utilizes a delay-based mechanism to reduce glitches. Besides, an Over-current Protection (OCP) circuit is included to avoid short-circuit hazard. The proposed is implemented on silicon using a typical 0.18 μm CMOS process. The total core area is 0.774 × 0.565 mm^2 and the power consumption is 158.4 mW at 10 Mbps data rate.**

Key word: FlexRay, transceiver, Over-current Protection.

I. INTRODUCTION

FlexRay V3.0.1 is the latest communication protocol [1] proposed by several automobile power houses, including BMW, Daimler-Chrysler, General Motors, Freescale, Philips, Bosch, Volkswagen, etc., in 2010. Recently, many researches regarding the FlexRay transceiver have been publicized [2]-[3]. According to FlexRay specification, a robust FlexRay transceiver is required to include a Bus Failure Detector (BFD) and short-circuit protection. A BFD is in charge of detecting whether buses are shorted to VDD or GND, which usually utilizes a voltage comparison method to distinguish bus status. However, BFD could generate a wrong warning signal if a glitch or large over-shoot voltage caused by the power MOS or switches' transitions accidently appear on bus [2]. Therefore, we propose a delay-based method in FlexRay transceivers to prevent such a situation. Besides, according to FlexRay specifications, the maximum output current limit of the transceivers is 60 mA no matter the buses are shorted to VDD, GND, or other buses. Thus, an Over-current Protection is needed in the transceivers. After the bus current is scaled down by a current mirror, we utilize a Current Bias Circuit, which generates a 60 μA current, and a current comparator to realize the required Over-current Protection on silicon.

II. DELAY-BASED TRANSCEIVER WITH OVER-CURRENT PROTECTION FOR FLEXRAY STSTEMS

Fig. 1 shows the proposed FlexRay Transceiver (FRT) design, including a Transmitter (Tx), a Receiver (Rx), Bus Failure Detector, a Current Bias Circuit (CBC), and a Voltage Bias Circuit (VBC). Tx is in charge of transmitting data on bus (BP/BM), where an Over-current Protection (OCP) is needed to avoid short-circuit hazard. Rx and Bus Failure Detector (BFD) are used to receive data and monitor bus status, respectively. Whenever BFD detects any short-circuit alarm on bus, BFD sends a warning to upper level as well as the controller (not shown). Notably, VBC and CBC generate a reference voltage, Bias_2V=2 V, and a reference current, Bias_60μA=60 μA, to Tx and Over-current Protection, respectively.

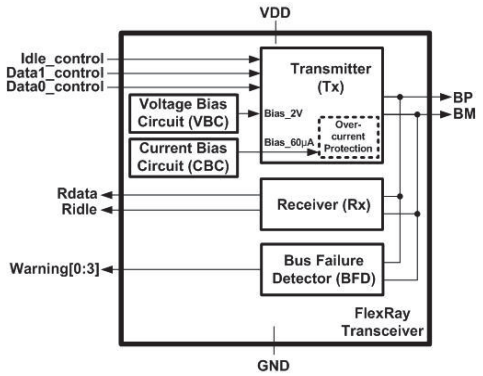

Fig. 1. Explosive view of FlexRay Transceiver (FRT).

The proposed delay-based Transmitter and Over-current Protection are shown in Fig. 2. The transitions of power PMOS transistors (e.g., LH0~LH3) and power NMOS transistors (e.g., LL0~LL3) can not be synchronized perfectly. A large current will be generated on BP and BM if they are accidently turned on at the same time. That is, a "glitch" is generated. A delay switch design (i.e., RH, RL, LH, and LL) are added to reduce the glitch. Besides, the power PMOS and NMOS transistors are equally divided into many transistors, i.e., M102 ~ M117. Because the size of each transistor is small and the transition time of gate drive thereof also is equally delayed, no large current will be resulted in BP and BM. Take M110 ~ M113 as an example. Buffer_N1, Buffer_N2, and Buffer_N3 provide different delays to drive the gate of M111, M112, and M113, respectively. The power transistors, M110~M113, are turned on step by step. An illustration in Fig. 3 shows the timing waveform of Buff_N1~ Buff_N3, and the without (prior work) and with (this work) glitch reduction. The glitch will be apparently eliminated by properly delaying the transition time of each power MOS.

As mentioned, the absolute maximum output current limit is 60 mA when the bus is shorted. Fig. 2 shows Over-current Protection (OCP) circuit to detect such a current limit. We use M119 as a current-mirror to scale down M118's tail current (≤60 mA) to 1/1000, which is supposed to be 60 μA at most. A Current Bias Circuit without BJTs based on [4] generating a reference 60 μA current (Bias_60μA) is included in FRT. When the $I_{tail,M119}$ is equal to or over Bias_60μA, OCP sends a signal, "Over-Current" to turn off Tx.

III. IMPLEMENTATION AND MEASUREMENT RESULT

The proposed FRT, including Tx/Rx, Bus Failure Detector, Voltage Bias Circuit, and Current Bias Circuit, is carried out

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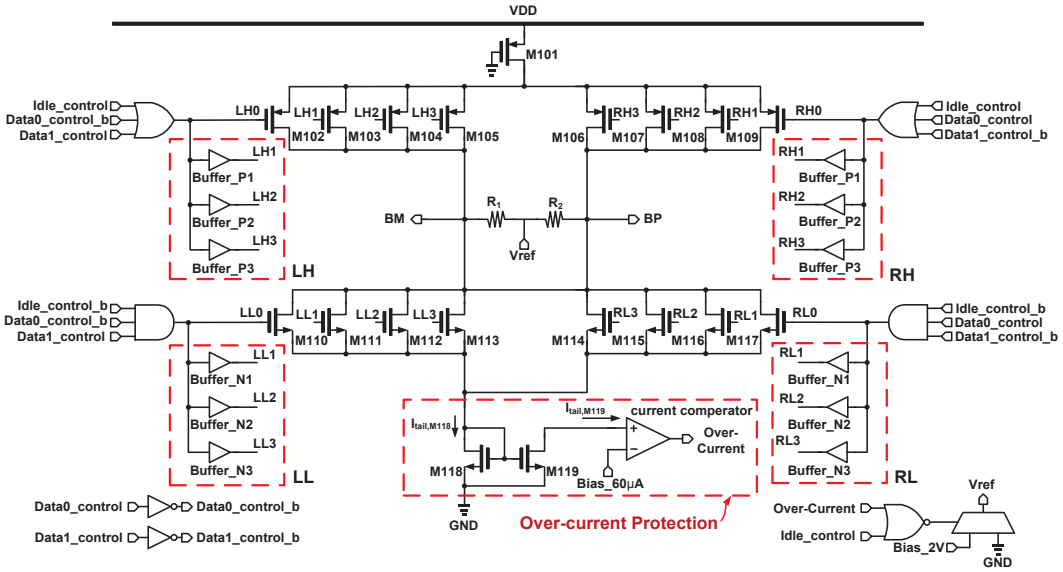

Fig. 2. The schematic of delay-based transceiver with over-current protection.

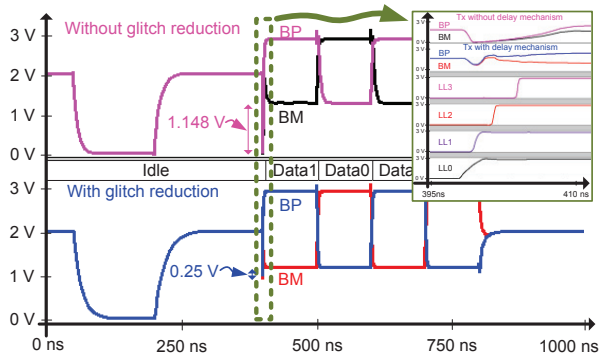

Fig. 3. The waveforms of Buffer_N1~ Buffer_N3 and glitch reduction (without and with).

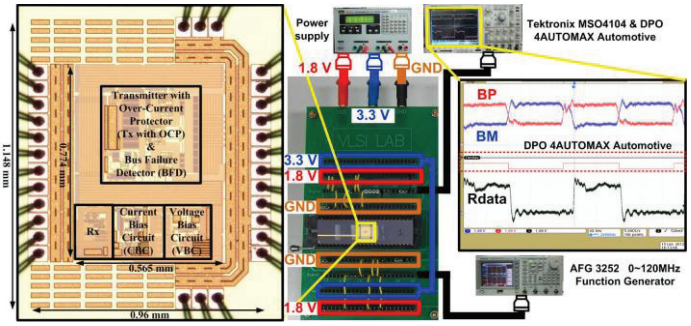

Fig. 4. The measurement set-up, die photo, and measured waveform of the proposed system.

using a typical 0.18 μm CMOS process. Fig. 4 shows the measurement set-up and readings, including all instruments, die photo, and measured waveforms. The total core area on silicon is 0.774 x 0.565 mm^2. The function generator, AFG 3252, generates a pair of Data0_control and Data1_control to FRT. The oscilloscope shows the BP and BM signals decoded by DPO 4AUTOMAX Automotive, which match the decoded Rdata by Rx. Therefore, the functionality of our proposed design is proved. Table I shows the comparison between the required FlexRay V3.0.1 specification and the measurement results of our FRT to prove that all of required transceiver specifications are met. Table II shows the performance comparison of the proposed FRT with our previous FlexRay transceiver design [2].

TABLE I
SPECIFICATION OF THE PROPOSED FRT

FLEXRAY TX SPECIFICATIONS V3.0.1		MEAS. RESULTS
Absolute value of uBus while sending	600 ~ 2000 mV	1520 mV
Absolute value of uBus while Idle (mV)	0 ~ 30 mV	13.1 mV
Transmitter delay negative edge (ns)	< 75 ns	5.18 ns
Transmitter delay positive edge (ns)	< 75 ns	4.35 ns
Transmitter delay Mismatch (ns)	< 4 ns	0.73 ns
Receiver delay, negative edge (ns)	75 ns	6.95 ns
Receiver delay, positive edge (ns)	75 ns	6.30 ns
Receiver delay mismatch (ns)	5 ns	0.65 ns
Throughput (Mbps)	10 Mbps	10 Mbps

TABLE II
COMPARISON TABLE OF THE PROPOSED FRT AND PRIOR WORK

	This work	[2]
Technology	Typical 0.18 μm CMOS process	Typical 0.18 μm CMOS process
FlexRay version	V3.0.1	V2.1B
Core area	0.43731 mm^2	0.117 mm^2
Data rate	10 Mbps	10 Mbps
Input voltage	1.8 V DC & 3.3 V DC	1.8 V DC & 3.3 V DC
Bus Failure Detection (BFD)	Yes	No
Over-current Protection (OCP)	Yes	No
Glitch reduction	Yes	No
Power consumption (each FRT)	158.4 mW	43.01 mW

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