# Bus Driver Controller with Hazard Detection for FlexRay Protocol 3.0.1

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Abstract—A Bus Driver (BD) controller design is presented in this investigation, where all of the hazard detection and protection required by FlexRay 3.0.1 are integrated and realized, including under-voltage (UV), bus failure, wake-up detection, etc. The required 4-state transition for FlexRay BD control is also carried out to coordinate the interfacing and signaling among the ECU (electronic control unit) Host and the analog BD frontend. The entire proposed design is implemented on silicon using 0.18  $\mu$ m 60 V BCD CMOS process. The area is 819x612  $\mu$ m<sup>2</sup>, and the system clock is 80 MHz based on the all-PVT-corner post-layout simulation. The proposed BD controller design is the first reported controller meet the requirements of FlexRay 3.0.1 protocol.

*Keywords*—FlexRay, Bus Driver (BD), Bus Guardian (BD), state transition, hazard detection

## I. INTRODUCTION

The car electronics cover power train, chassis safety, peripheral electronics control system, telematics communication system, in-vehicle networking, etc. For the sake of safety, entertainment, and comfortness in a vehicle, the speed and quality of data communication among ECUs (electronic control unit) must be enhanced. FlexRay V3.0.1 is the latest in-car communication protocol [1] proposed by several automobile power houses, including BMW, Daimler-Chrysler, General Motors, Bosch, Volkswagen, etc., in 2010. It was designed for data exchange among ECUs installed in a vehicle. Besides the 10-20 Mbps high bandwidth demand, FelxRay specifications also emphasize the security such that under-votlage, over-temperature detection, bus failure, and wake-up detection are all required.

Regarding the total solution for FlexRay transceiver design, only a few reports were found in the literature. However, they are high power consumption and not easily to be integrated with digital signal processors, which is usually implemented using a low-voltage process. FlexRay transceiver revealed in [4] and [5], did not cover BG (bus

<sup>†</sup>Prof. C.-C. Wang is with Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 80424. (e-mail: ccwang@ee.nsysu.edu.tw). guadian). By contrast, [6] did not include BD (bus driver). [2], [3], and [7], however, only managed to demonstrate the digital functionality using FPGA or development board. Most important of all, these mentioned prior works almost ignore the security-related mechanisims required by FlexRay specifications, including under-votlage, over-temperature detection, bus failure, wake-up detection, etc. Therefore, we demonstrate a BD controller design with hazard detection using 60V BCD technology. All of the required security functions are carried out to meet the standard of FlexRay 3.0.1.

# II. FLEXRAY ECU BD WITH HAZARD DETECTION

Fig. 1 shows the explosive view of an ECU composed of Host, Communication Controllers (CC), and FlexRay Transceivers (FRT), where CC supervises the signals from BG (Bus Guardian) and generates an error interrupt to Host if the scheduling of BG is misaligned. FRTs are used to transmit and receive data into/form the bus via two channels, i.e., Channel 1 and Channel 2.

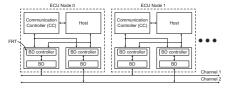


Fig. 1. ECU nodes on the FlexRay bus

#### A. Bus driver (BD) controller

Referring to Fig. 2, BD controller, in fact, is the master of the entire BD, which is in charge of monitoring the statuses of the bus, the temperature, the power supply, and the messages from the Host. On the other hand, it also takes actions as soon as any hazard is detected. A total of 4 blocks are included in the BD controller shown in Fig. 2, namely, Host Interface, CC Interface, BG Interface, and Power Supply Interface, which are respectively in charge of communication with Host, CC (communication control), BG (Bus Guardian), and power supply. Since the Tx/Rx design has been reported in [4], and BG design has also been reported [6], there is no reason to rephrase in this investigation. All of the other sub-circuits will be detailedly described in the following text.

Fig. 4 shows the flow chart for BD to detect the required 7 different types of harzards, which are LOCAL WAKEUP (S0), REMOTE WAKEUP (S1), BUS ERROR@(S2), TEMP HIGH (S3), TEMP MEDIUM (S4), UVVBAT (S5), and UVVCC (S6). Notably, any one hazard from S2 to S6 needs to assert ERRN logic low such that a warning message will be issued.

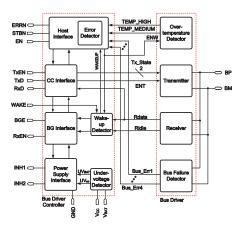


Fig. 2. Block diagram of BD with hazard detection

A total of 4 states are required by FlexRay 3.0.1 for the BD, which are Normal, Standby, Sleep, and Receive Only modes. Referring to Fig. 3, they are, respectively, described as follows.

• **BD\_Normal Mode :** BD is able to transmit and receive in this mode provided that the bus is biased appropriately.

BD\_Standby Mode : This is one of the two low-power modes. BD is not able to either transmit or recieve signals over the bus, since the bus is shorted to a pre-defined voltage.
BD\_Sleep Mode : This is the other low-power mode when the bus is shorted to GND. Certainly, BD is not functional in this mode. This mode is specifically for abnormal power voltage or low battery scenarios. Notably, this mode is entered by a command issued via Host Interface only.

• **BD\_Receive\_Only Mode :** In this mode, BD is forced to "listen" to the signals on the bus only. Any signal transmission is prohibited.

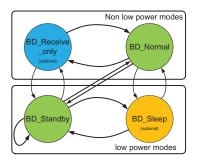


Fig. 3. State transistion of BD controller

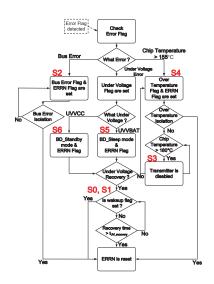


Fig. 4. Hazard detection flowchart

#### B. Wake-up detector

The wake-up function for FlexRay protocol is required to carry two different detections : local wake-up and remote wake-up.

(i). local wake-up detector (LWD) : Referring to Fig. 5, FlexRay protocols demand that ECUs should stay in low power modes provided that UVVCC (under-voltage VCC) or UVVBAT (under-voltage battery) is set. Usually, WAKE also stays low. However, BG or Host can wake up this ECU via this WAKE signal. As soon as WAKE is pulled up by either BG or Host, LWD will monitor if it lasts over  $t_{wake}$ . If yes, LOCAL\_WAKEUP will be asserted low to start the ECU. Simultaneously, UVVCC and UVVBAT will be pulled high to leave the low power modes.

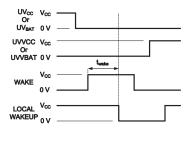


Fig. 5. Timing of LWD

(ii). remote wake-up detector (RWD) : By contrast, an ECU can be waked up by another ECU via the transistions over the bus, it is called "remote wake-up." Again, the ECU stays in the low power modes as long as UVVCC (under-voltage VCC) or UVVBAT (under-voltage battery) is set. RWD in the ECU keeps monitoring the variations of the differential signals of the bus, namely BP and BM. Referring to Fig. 6, as soon as two consecutive (BP-PM) pulses with duration over  $t_{det_DATA0}$  interleaved with two mark-level bits with duration over  $t_{det_idle}$  are detected, RWD will pull down REMOTE\_WAKEUP to signal BG and the rest of the ECU.

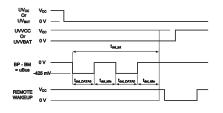


Fig. 6. Timing of RWD

## C. Under-voltage detector

FlexRay protocol require detection of two particular voltages, i.e.,  $V_{CC}$  (system voltage) and  $V_{BAT}$  (battery voltage). Either one of them drops below a pre-defined voltage level, warning signals and corresponding actions should be taken. Take the battery low as an example. Referring to Fig. 7,  $V_{BAT}$ is scaled down to  $V_{cp}$  by the voltage divider consisting of  $R_1$  and  $R_2$ . Similarly, a reference voltage,  $V_{uvdBAT}$  is also scaled down to  $V_{uvd\_cp}$  by the voltage divider consisting of  $R_3$  and  $R_4$ .  $UV_{BAT}$  is then generated by the voltage comparator with  $V_{uvd\_cp}$  and  $V_{cp}$  as inputs. If  $V_{cp}$  is lower than  $V_{uvd\_cp}$ ,  $UV_{BAT}$  is asserted high to pull up the UVVBAT (under-voltage battery) signal. The entire ECU is forced into BD\_Sleep state.

The  $V_{CC}$  (system voltage) detection is the same as  $V_{BAT}$ , which means the circuit is identical. However, the only difference is that the ECU will be forced into BD\_Standby state if  $V_{CC}$  (system voltage) is lower than the corresponding pre-defined voltage, which also pulls up the UVVCC (undervoltage VCC).

#### D. Bus failure detector

One of the most frequent faults in communication networks is the bus line (BP or BM) short-circuit [6]. A bus shortcircuit failure detector is then required in the receiver design, as shown in Fig. 8. The MOS string, M101 to M105, is used to generate one reference voltage, VrefA ( $\approx 4.5$  V), which is close to system supply voltage. By contrast, M106 and M107 consists of a voltage divider to generate VrefB ( $\approx 0.7$ V), which is close to GND. The 4 comparators, respectively,

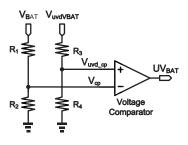


Fig. 7. Under-voltage detectors

generated 4 digital codes, namely Bus\_Err1 to Bus\_Err4. These codes are classified into 4 scenarios as follows.

- Bus\_Err1 = 1 : BP is short-circuited to VCC.
- Bus\_Err2 = 1 : BP is short-circuited to GND and BM is not GND.
- Bus\_Err3 = 1 : BM is short-circuited to VCC.
- Bus\_Err4 = 1 : BM is short-circuited to GND and BP is not GND.

Any of the above signals is pulled high, they will be notified to Host, as shown in Fig. 2. Then, appropriate corresponding actions should be taken to respond.

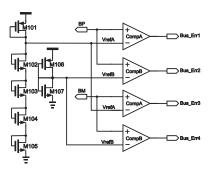


Fig. 8. Bus failure detector

### **III. IMPLEMENTATION AND SIMULATIONS**

The proposed FlexRay BD controller is carried out using the cell library of a typical 0.18  $\mu$ m 60V BCD CMOS process. Fig. 9 shows the layout, where the area is 0.819  $\times$  0.612 mm<sup>2</sup>. Fig. 10, 11, 12, 13, and 14, are the postlayout simulation results of normal networking Tx/Rx, local wake-up, remote wake-up, under voltage detection (battery low), and bus failure detection, repetively, using EDA tools, namely Encounter.

Table I shows the comparison of this work and several prior BD controller works. The proposed controller is the only solution to meet the speed and hazard detection requirements of the FlexRay protocol.

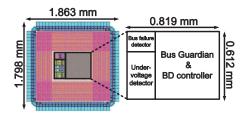


Fig. 9. Layout of the proposed BD controller



Fig. 10. Normal BD controller operation

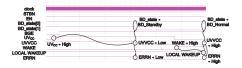


Fig. 11. Local wake-up scenario

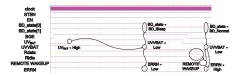


Fig. 12. Remote wake-up scenario

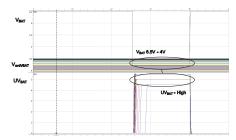


Fig. 13. Battery low detection



Fig. 14. Bus failure detection

TABLE I Comparison with prior works

	[8]	[6]	this work
Process	0.35 $\mu$ m Samsung	0.18 µm CMOS	0.18 $\mu$ m HV CMOS
Gate Count	58,691	4,550	5,833
Clock	77 MHz	80 MHz	80 MHz
Hazard Det.	No	No	Yes
Year	2012	2009	2013

# IV. CONCLUSION

This paper presents a FlexRay BD controller with hazard detection functionality. By the proposed hazard detectors, the BD controller meets all of the required security functions demanded by FlexRay protocols without any loss of system operation performance, namely speed.

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