A High-Speed 2×VDD Output Buffer With PVT Detection Using 40-nm CMOS Technology

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***Abstract*—A high-speed compensation technique is proposed to automatically adjust the slew rate of a 2×VDD output buffer. Based on the detected PVT (Process, Voltage, Temperature) corner, the output buffer will turn on different current paths correspondingly to either increase or decrease the output driving current such that the slew rate of the output can be adjusted as well. The proposed design is implemented using a typical 40 nm CMOS process to justify the slew rate compensation performance. By on-silicon measurements, the data rate is 500/460 MHz given 0.9/1.8 V supply voltage with a 20 pF load, the maximum slew rate is 0.53 (V/ns), and the core area of the proposed design is 0.052 × 0.254 mm^2.**

***Index Terms*—PVT variation, threshold voltage detection, mixed-voltage tolerant, I/O buffer, floating N-well circuit, gate-oxide reliability, slew rate compensation.**

I. Introduction

It is well known that more transistors can be integrated in a chip by using advanced CMOS technology. Another big advantage is that the circuits consisting of these advanced transistor operate faster than before. The nanometer CMOS technology undoubtfully provides these advantages, e.g., high circuit operating speed, low power supply voltage, and small area in system-on-chip (SoC) integration. However, in a PCB-based system, not every chip is fabricated by using the same advanced process. That is, some of the chips or discretes on a PCB-based system were fabricated by a not-so-advanced process, e.g., 5V or 3V CMOS process. Therefore, the output buffer fabricated by advanced processes needs to accommodate high or low voltage swings to communicate with older circuits. Therefore, a mixed voltage output buffer is needed in such a scenario [1]-[4].

Besides, I/O interfaces must be designed to prevent problems of leakage current, and electrical overstress on the gate oxide, and offset caused by the PVT variations, which are very serious in the nanomerer CMOS technology [5], [6]. However, most of the prior designs did not consider the slew rate offset caused by the PVT variations [1]-[3]. By contrast, PVT variations have been proved to affect the slew rate of the output buffer severely [7]. Thus, many recent works have been proposed to enhance the capability against PVT variation and enlarge the acceptable envelope as much as possible to enhance the yield. Though the logic delay method has been widely utilized to the detect PVT variation [7]-[8], it can only recognize three corners, i.e., TT, FF, and SS. The FS and SF corners were left unsolved in these works. Therefore, this work proposes a novel corner detection technique to detect all process corners, i.e., TT, FF, SS, SF, and FS. Another problem of the prior works is that the transmitting and receiving speeds were not fast enough to meet certain specifications, e.g., PCI-express, which is up to 266 MHz. Thus, high speed operation is another requirement for mixed voltage output buffers besides the PVT detection and the slew rate compensation.

In this study, we propose a hight-speed 2×VDD output buffer with PVT detection using 40-nm CMOS Technology. By using the compensation mechanism and the NMOS and PMOS process corner detectors, the slew rate of the output buffer is self-adjusted in a 500 MHz date rate.

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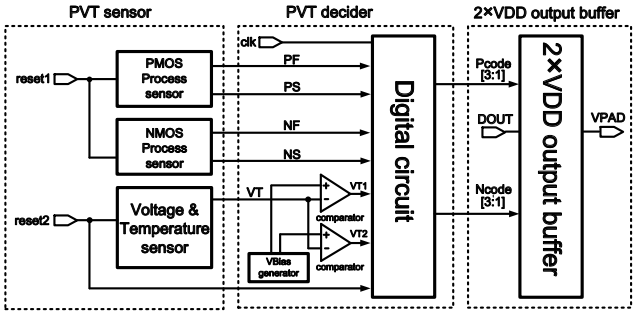

Fig. 1. The block diagram of the proposed output buffer.

II. 2 × VDD Output Buffer Circuit Design

Fig. 1 shows the block diagram of the proposed output buffer, which is composed of 3 major blocks, i.e., PVT sensor, PVT decider, and a 2×VDD output buffer. The details of these function blocks are given in the following text.

A. The PMOS Process sensor

Fig. 2 (a) and (b) show the schematics of the PMOS F and S corner sensors, which are composed of 4 cascaded inverters, respectively. The major difference is that inv1 ∼ inv3 and inv4 ∼ inv6 sizes are designed as high skew : low skew : low skew and high skew : high skew : low skew, respectively. The theory

of such a design is that the threshold voltage difference of PMOS at S and F corners will be magnified by skew-inverters.

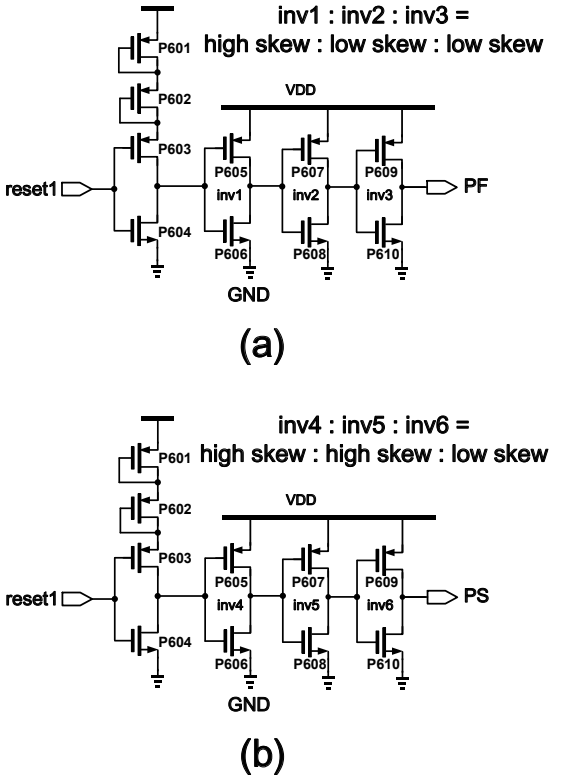

Fig. 2. Schematics of the PMOS process sensor detecting (a) F corner and (b) S corner.

B. The NMOS Process sensor

By a similar thought, the schematics of the NMOS F and S corner sensor are shown in Fig. 3 (a) and (b), which are composed of 1 NMOS source follower and 4 inverters, respectively. The major difference is that inv7 $\sim$ inv9 and inv10 $\sim$ inv12 sizes are designed as high skew : low skew : low skew and high skew : high skew : low skew, respectively.

C. The Voltage & Temperature sensor

Fig. 4 shows the schematic of the Voltage & Temperature sensor, comprising 2 cascaded PMOS source followers and an inverter. The PMOS source follower is composed of MP905 $\sim$ MP908. Notably, MP905 $\sim$ MP906 and MP907 $\sim$ MP908, which are without the body effect and with body effect, respectively. The function description of this sensor circuit is given as follows.

- step 1 : When the reset2 is activated, V_vthp2 and pout are pulled high to VDD (= 0.9 V).
- step 2 : When the reset2 is pulled low, V_vthp2 is discharged till Vthp, which is the threshold voltage of MP905.
- step 3 : By a similar operation, VT will be discharged till 2$\times$Vthp in the next repeated cycle the same as the previous step 1 and step 2.

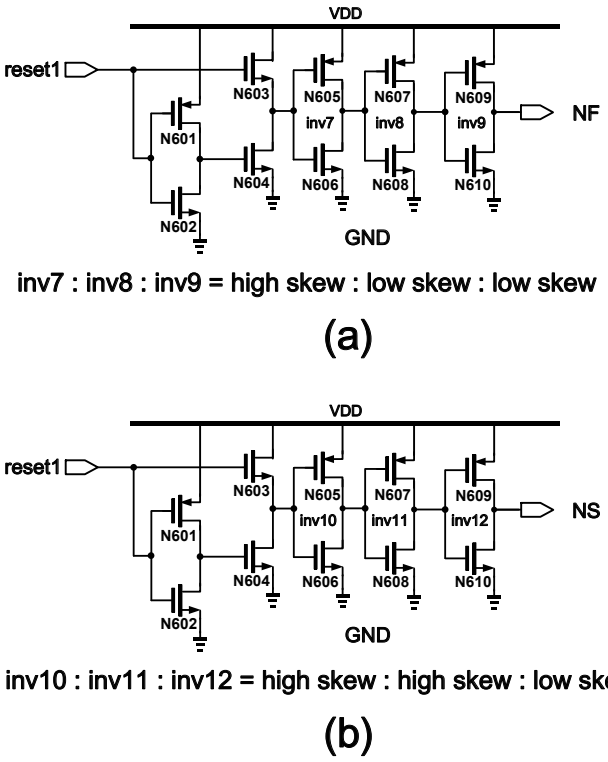

Fig. 3. Schematics of the NMOS process sensor detecting (a) F corner and (b) S corner.

According to Eqn. (1), the Vthp of MOS with body effect will drift at different Vbs, which is the voltage difference between VDD and source voltage of MOS. Notably, $\mathrm{Vthp0}$ is the no body effect threshold voltage, γ_p is the body effect coefficient, Vfn is the bulk surface potential, Vbs is the voltage difference between bulk and source of MOS.

$$\mathrm{Vthp} = \mathrm{Vthp0} + \gamma_{\mathrm{p}}(\sqrt{2|\mathrm{Vfn}| + \mathrm{Vbs}} - \sqrt{2|\mathrm{Vfn}|}) \qquad (1)$$

where γ_p can be written as $\gamma_p = \frac{\sqrt{2q\varepsilon_s N_A}}{C_{ox}}$, q is electronic charge, ε_s is silicon dielectric constant, N_A is doping concentration, and C_{ox} is oxide capacitance. Since γ_p of the Vthp comprises temperature factors, the 2 cascaded source followers generate a 2$\times$Vthp voltage, namely VT, with VDD and temperature variation.

D. The PVT decider

The PVT decider in Fig. 1 consists of a $\mathrm{V_{Bias}}$ generator, two comparators, and a Digital circuit. Fig. 5 shows the block diagram of Digital circuits composed of a 6-bit counter, an Encoder, and D flip-flops. According to the outputs of PMOS Process sensor, NMOS Process sensor, and Voltage & Temperature sensor, the PVT decider derives two digital codes, Pcode [3:1] and Ncode [3:1], to notify the following 2$\times$VDD output buffer what the sensed PVT status is. The codes indicates the required compensation status so as to control the output currents in the 2$\times$VDD output buffer.

E. 2$\times$VDD Output Buffer

Fig. 6 shows the 2$\times$VDD output buffer, which is composed of a Pre-driver, a Vg1 generator, a VDDIO detector, and an

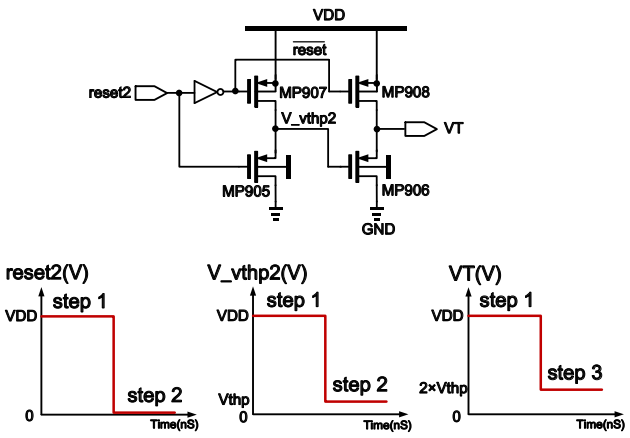

Fig. 4. Schematic of the Voltage & Temperature sensor.

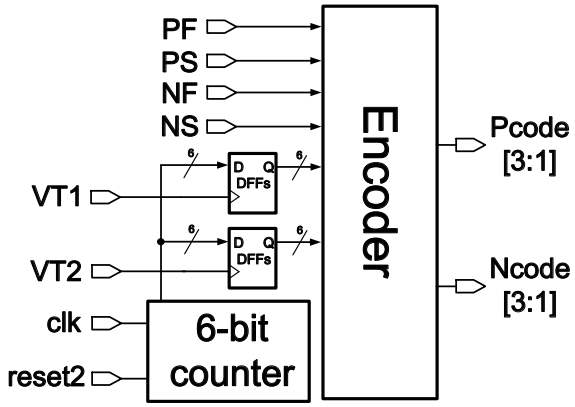

Fig. 5. Schematic of Digital circuit.

Output stage. The Pre-driver is used to encode three control signals, DOUT, Pcode [3:1], and Ncode [3:1], to compensate output currents for slew rate adjustment. The VDDIO detector and Vg1 generator will generate appropriate gate drive voltages in different voltage modes without leakage currents and overstress problems.

F. Output Stage

Fig. 6 shows the Output stage in the proposed 2 × VDD output buffer. The supply voltage (VDD) of the core circuits using 40 nm CMOS process is 0.9 V. Thus, the output stage must be realized using two groups of stacked PMOS and NMOS transistors, respectively, for transmitting 2×VDD signals. PMOSs M1a ∼ M1c are in parallel such that the slew rate of the output signal can be compensated by turning on or off the current paths flowing through M1a ∼ M1c individually. The switching status of M4a ∼ M4c are corresponding to PMOSs mentioned in the above.

III. Implementation and Measurement Results

This work is implemented using 40 nm CMOS technology without any thick-oxide device. Fig. 7 shows the die photo of this work, where the overall chip size is only 0.687 × 0.525 mm^2 and the compensation circuit is only 0.052 × 0.254 mm^2.

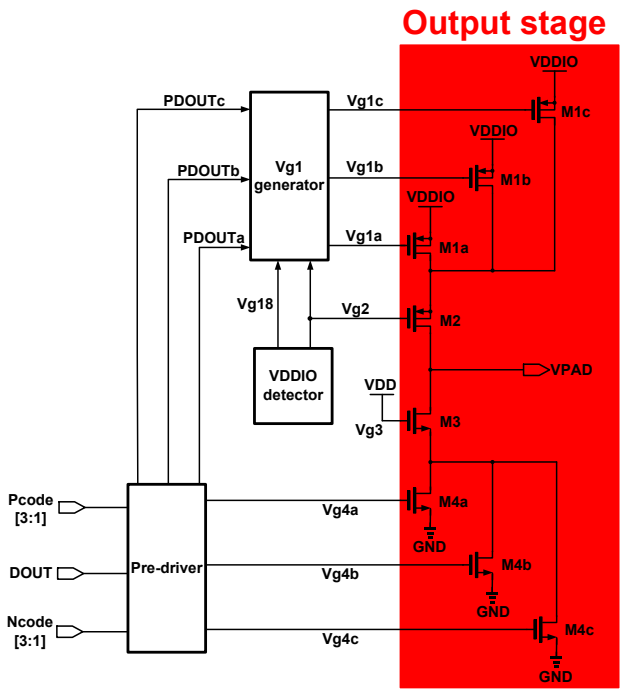

Fig. 6. Schematic of the 2×VDD output buffer.

The uncompensated and compensated VPAD given VDDIO = 0.9/1.8 V in Tx mode, as shown in Fig. 8 and Fig. 9, respectively. After compensation, the slew rate is enhanced to 0.530 (V/ns) from 0.498 (V/ns) and 0.523 (V/ns) from 0.477 (V/ns) given VDDIO = 0.9/1.8 V, respectively. Apparently, the data rate is 500/460 MHz when VDDIO = 0.9/1.8 V, respectively. The performance of the proposed design is summarized in the Table I. Table II shows the comparison between this work and several prior works. This work is the only one to provide all-PVT-corner detection and the slew rate compensation. Meanwhile, our design is also the only one to meet the date rate specifications of PCI-express given VDDIO = 0.9/1.8 V. Besides, the core area is the smallest compared with several prior works in Table II.

TABLE I
Compensation Results at Different VDDIOs

VDDIO	0.9 V	1.8 V
Data rate (MHz)	500	460
Slew rate improvement (V/ns)	8% (0.498→0.530)	6% (0.477→0.523)

IV. Conclusion

In this work, the hight speed 2×VDD output buffer with PVT detector for slew rate compensation is implemented using a typical 40 nm CMOS process. The data rate is 500/460 MHz when VDDIO = 0.9/1.8 V. The maximum slew rate is 0.53 (V/ns) when VDDIO = 0.9 V. Notably, the PVT sensor and PVT decider are implemented on chip, the core area is only 0.052 × 0.254 mm^2. The area overhead is only 31% for a single output buffer. Therefore, this work is proved on silicon to detect all PVT corners of PMOS and NMOS, respectively.

TABLE II
PERFORMANCE COMPARISON OF OUTPUT BUFFER

	[7] *JSSC*	[1] *TCAS-I*	[2] *TCAS-I*	This work
Year	2003	2009	2010	2012
Process (μm)	0.18	0.35	0.18	0.04
Supply voltage (V)	3.3	3.3	1.8	0.9
Transmitting voltage mode (V)	3.3	1.8/3.3/5.0	0.9/1.2/1.8 /2.5/3.3/5.0	0.9/1.8
Results	Measured	Measured	Measured	Measured
Date rate (MHz)	N/A	80/120/84	10/40/50 /2.5/3.3/5.0	500/460
Slew rate (V/ns)	0.40 $\sim$ 0.99	Max. 0.71	NA	0.530/0.523
Process corners detected	TT, FF, SS	N/A	N/A	TT, FF, SS FS, SF
Slew rate improvement	32%	N/A	N/A	8% / 6%
Core area (mm^2)	0.421 $\times$ 0.317	87.4 $\times$ 385	0.065 $\times$ 0.628	0.052 $\times$ 0.254

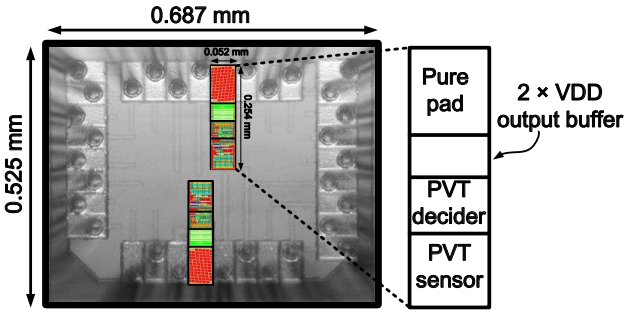

Fig. 7. Die photo of the proposed design.

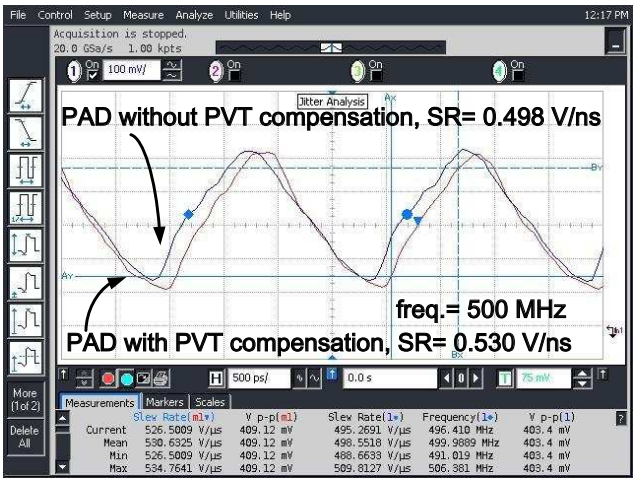

Fig. 8. The uncompensated and compensated VPAD with VDDIO = 0.9 V.

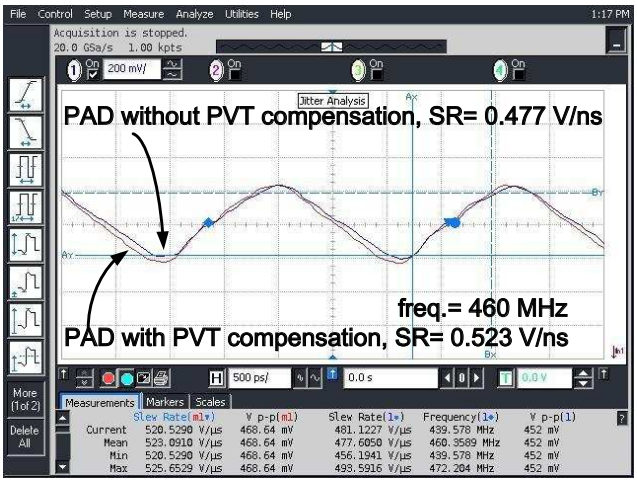

Fig. 9. The uncompensated and compensated VPAD with VDDIO = 1.8 V.

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