An Accurate Phase Shift Detector Using Bulk Voltage Boosting Technique for Sensing Applications

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***Abstract*—This paper introduces a phase shift detector (PSD) with high accuracy for sensing applications. The proposed design comprises a Narrow bandpass filter, a Comparator, and an Offset calibration circuit. Narrow bandpass filter rejects all the signals except that generated from a Fixed-frequency Generator. To reduce the error caused by circuit noise and external interface, Offset calibration circuit (OCC) is utilized to calibrate the Comparator. The proposed phase shift detector circuit is realized on silicon using a 0.18 μm CMOS technology. The post-layout simulation results show that the proposed design is able to detect the phase difference from -90° to 90°, where the maximum output error of the proposed PSD is 2.37%. Besides, the power consumption is 4.365 mW @ 10 MHz given a 0.9 V power supply voltage.**

***Index Terms*—analog processing circuit, phase shift detector, offset calibration circuit, phase-shift readout circuit, high accuracy**

I. Introduction

Biomedical sensors have been long used in many applications due to their high performance and small size, e.g., the concentration detection of the specific analyte. After the sensor reacts with the analyte, certain features of the sensor will be affected, such as resonant frequency or impedance. The phase shift phenomena is the one of the features has been widely utilized [1]-[4]. For example, the surface acoustic wave (SAW) sensor for direct methanol fuel cell (DMFC) is used to sense the concentration of the methanol [5], and the flexural plate wave (FPW) sensor is able to detect the severe acute respiratory syndrome coronavirus (SARS-CoV) [6].

Fig. 1 shows a typical phase shift detector for sensing applications. The input signal to the sensors is from a generator to generate a signal with a fixed frequency to sensors. Then, the phase shift detector will generate a digital signal corresponding to the phase difference of the sensors' output signals. The following microprocessor (MCU) is used to compute the phase difference and deliver a quantitative output. Chang *et al.* showed a control procedure of the miniature system composed of an unit gain buffer, a phase locked loops (PLL), and a frequency phase detector, as shown in Fig. 2 [6]. The PLL is composed of a phase detector (PD) detecting the input phase and a low pass filter generating an analog voltage proportional to the phase. Since the impedances of the two sensors in the experimental group and the control group would be different, the amplitude of the corresponding outputs would also be different. It will cause severe error if the output of the sensor (analog signal) directly coupled to the PLL (digital circuit). Marcellis *et al.* reported an analog auto-calibrating phase to voltage converter [7]. However, since the output of the phase to voltage converter is an analog signal, it needs an external circuit to convert the analog output into a digital signal, such as analog to digital converter (ADC). The additional circuit will likely cause additional error during the conversion process.

This study presents a novel phase shift detector generating a digital signal. A narrow bandpass filter is utilized to reject the coupled noise and provide a high gain. Besides, to reduce the error at the output stage, an Offset calibration circuit is proposed to calibrate the comparator.

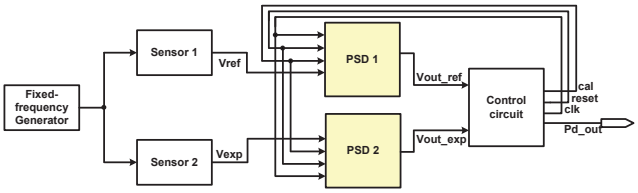

Fig. 1. Architecture of the typical phase shift detector for sensor application

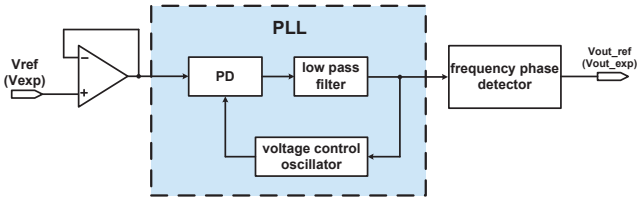

Fig. 2. Schematic of the PSD with PLL [6]

II. Phase Shift Detector Architecture

Fig. 3 shows the architecture of the proposed phase shift detector, consisting of a Narrow bandpass filter, a Comparator, and an Offset calibration circuit. Since the DC term of the sensor's output is 0 V, the noise will seriously degrade the sensitivity of the Comparator. Narrow bandpass filter in charge of screening out all of the unwanted signal outside of a pre-selected bandwidth. Then Comparator converts the output of Narrow bandpass filter into a digital signal. To reduce the error caused by the conversion, Offset calibration circuit (OCC) is utilized to carry out calibration. In the rest of this paper, the calibration method of OCC will be disclosed in detail, while the post-layout simulation results of OCC and the entire PSD will be demonstrated to justify the functionality. Since the

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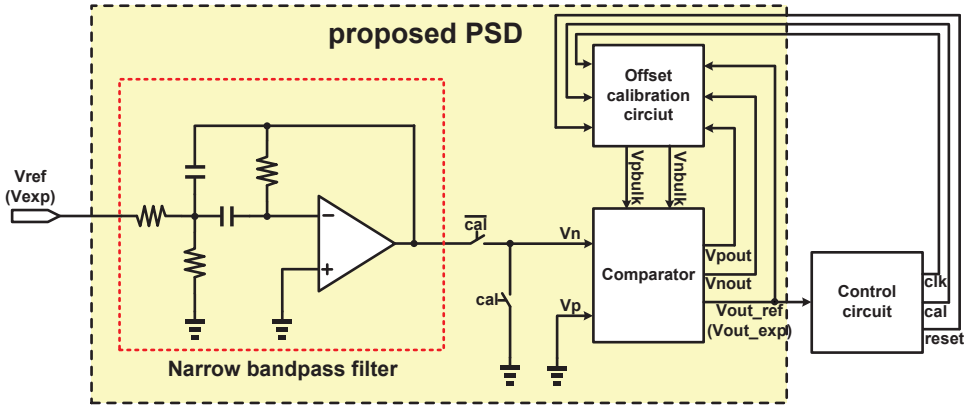

Fig. 3. Architecture of the proposed phase shift detector

Narrow bandpass filter is carried out by conventional 2-order BPF (band-pass filter) design methodologies, there is no need to rephrase hereby.

III. PSD Circuit Design and Analysis

A. Comparator

Fig. 4 shows the schematic of the proposed Comparator, which includes three stages: pre-amplification, decision circuit, and output buffer. Two supply voltages, VDD and VSS denoting 900 mV and -900 mV, respectively, are needed. The bulk of PMOS, MP1, MP2, MP5, and MP6 are coupled to VDD, and the bulk of all NMOS are coupled to the VSS, which are just like typical PMOS and NMOS configuration. Since generating a voltage higher than VDD is much easier than generating a voltage lower than VSS, the proposed Comparator has two additional input pins to select the bulk voltages of PMOS, MP3 and MP4, in the decision circuit stage.

According to the following equation for the threshold voltage

$$V_{tb} = V_{t0} + \gamma \times (\sqrt{V_{SB} + 2\phi_B} - \sqrt{2\phi_B}) \qquad (1)$$

where V_{tb} is threshold voltage, V_{SB} is the voltage difference between source and bulk, V_{t0} is the threshold voltage when V_{SB} is 0 V, γ is body effect parameter, and ϕ_B is the surface to bulk potential. If the bulk voltages of the MP3 or MP4 has been boosted differently, the drain currents of MP3 and MP4 will be correspondingly different even though the two PMOS have the same gate voltage. This feature can be taken advantage of so as to neutralize or reduce the input offset voltage of the Comparator. By simulation results, Fig. 5 shows the relationship between the input offset voltage of the Comparator and the PMOS bulk voltage. To cancel the offset voltage ranging from 40 mV to -40 mV, the bulk voltage of MP3 or MP4 would be raised to as high as 1074 mV. Thus, the following Offset calibration circuit decides which bulk to be raised based on the Vpout and Vnout such that offset cancellation is feasible.

B. Offset calibration circuit (OCC)

The proposed PSD has three modes: Calibrating mode, Normal mode, and DAC Reset mode. Fig. 6 shows the proposed OCC comprising an SR latch, a MUX, and two Bulk voltage

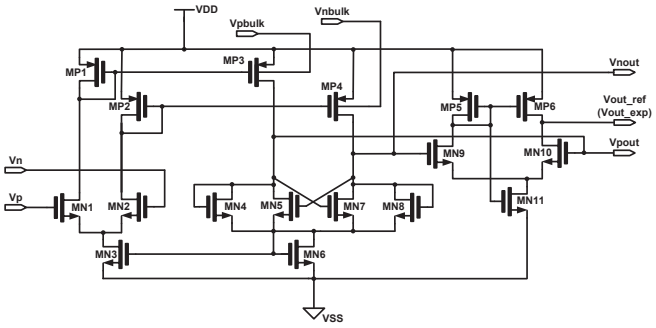

Fig. 4. Schematic of the proposed Comparator

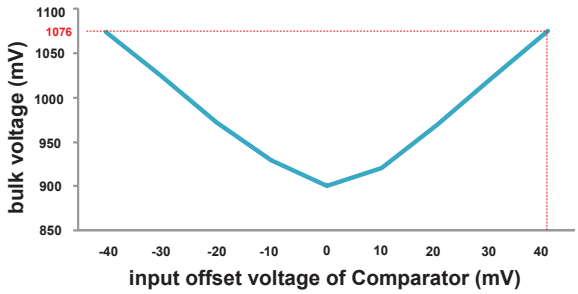

Fig. 5. Relationship between offset voltage and the PMOS bulk voltage

generators (BVG). Each BVG, as shown in Fig. 7, includes a counter and a DAC. In Calibrating mode, cal will be pulled up by the control circuit. The function of the proposed PSD in Calibrating mode is explained as the following steps.

step 1: Referring to Fig. 3 again, the inputs of Comparator, Vn and Vp, are coupled to 0 V when the cal is high.

step 2: Referring to Fig. 4, if the offset voltage of the Comparator is positive, the output Vout_ref and Vpout will both be pulled up high. By contrast, if the offset voltage of the Comparator is negative, Vout_ref will be pulled down low and Vnout will be high.

step 3: Referring to Fig. 6, the SR latch in OCC locks the Vpout and Vnout. Since one of SRout1 and SRout2 will be high, the corresponding BVG will be enabled.

step 4: The counter in the enabled BVG starts to count up, and the count is coupled to the following DAC.

step 5: The output of the DAC is coupled to the bulk voltage of either MP3 or MP4 in Comparator such that the offset voltage of Comparator can be reduced.

step 6: Once the offset voltage crosses over 0 V, the output of Comparator, Vout_ref, will be flipped.

step 7: The counter stops counting and locks the output. Then, the Calibrating mode stops.

Since the counter will record the count in the end of Calibrating mode, the proposed PSD is only activated in Calibrating mode when the PSD begins to work. However, the output of the DAC may drop after a long time in Normal mode because of the leakage. Thus, the proposed PSD has to be switched to DAC Reset mode to reset the output of DAC after the proposed PSD stays in Normal mode in a period of time pre-defined in the control circuit, as shown in Fig. 8.

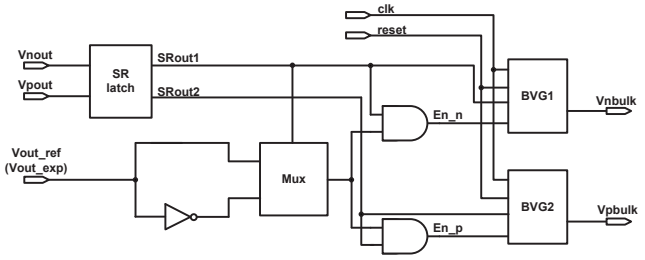

Fig. 6. Schematic of the proposed Offset calibration circuit

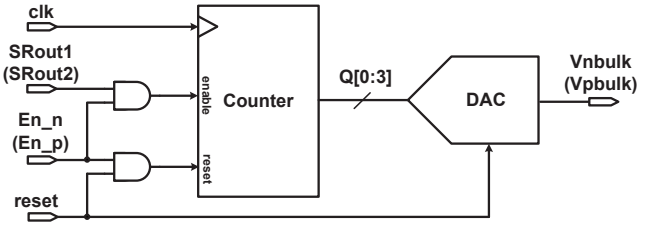

Fig. 7. Schematic of the Bulk voltage generator

IV. Implementation and Simulation

The proposed phase shift detector is realized on silicon using UMC 0.18 μm CMOS technology. Fig. 9 shows the entire circuit layout including I/O PADs, where two proposed PSD are included. The chip area is $589.9 \times 844.3\ \mu\mathrm{m}^2$, and the area of one proposed PSD is $308.1 \times 159.9\ \mu\mathrm{m}^2$.

Fig. 10 shows the simulation results of the proposed OCC. The blue curve shows the relationship between the offset voltage of Comparator and the output voltage of OCC, Vpbulk or Vnbulk. By contrast, the red curve is the ideal cancellation between the offset and the bulk voltages of MP3 or MP4. After the calibration by the proposed design, the worst-case

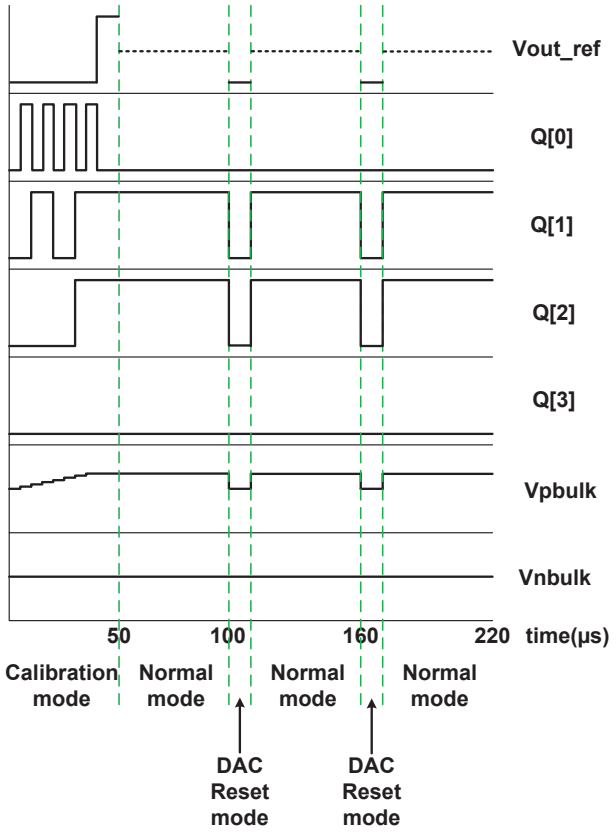

Fig. 8. The timing diagram of the proposed OCC

simulation result, FF 100°C, of the offset voltage is tabulated in Table I. The maximum offset voltage is 6.58 mV, and the original offset voltage is 30 mV. Namely, the minimum improvement is 76.70%.

During the simulation of the proposed PSD, two signals with the same amplitude and frequency but with different phase are coupled to two proposed PSDs. Fig. 11 shows the phase shift errors between the outputs and the inputs of the PSDs at different phases by the simulation results. The maximum error is 2.37% when the different phase is 25°.

The comparison with several prior works is tabulated in Table II. The proposed design attains the smallest output error, 2.37%.

TABLE I
THE CALIBRATION RESULT AND THE IMPROVEMENT OF THE PROPOSED OCC

Original offset (mV)	Calibrated offset (mV)	improvement (%)
40	4.34	89.15
30	6.58	78.07
20	1.62	91.90
10	0.71	92.90
-10	-2.33	76.70
-20	-3.23	83.85
-30	-2.32	92.27
-40	-5.59	86.02

TABLE II
COMPARISON WITH PRIOR WORKS

	[8]	[9]	[6]	[10]	this work
Year	2003	2006	2008	2013	2015
Process	0.5 μm CMOS	0.5 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.25 μm CMOS
Supply voltage	N/A	N/A	$\pm$12 V	3.3 V	$\pm$0.9 V
Phase range	0° $\sim$ 90°	0° $\sim$ 360°	-134° $\sim$ 134°	N/A	-90° $\sim$ 90°
output type	analog	analog	digital	analog	digital
Output error	$<$ 15%	$<$ 5%	$<$ 10 %	N/A	-2.37 %
Chip area (mm$\times$mm)	N/A	N/A	N/A	1.2	290

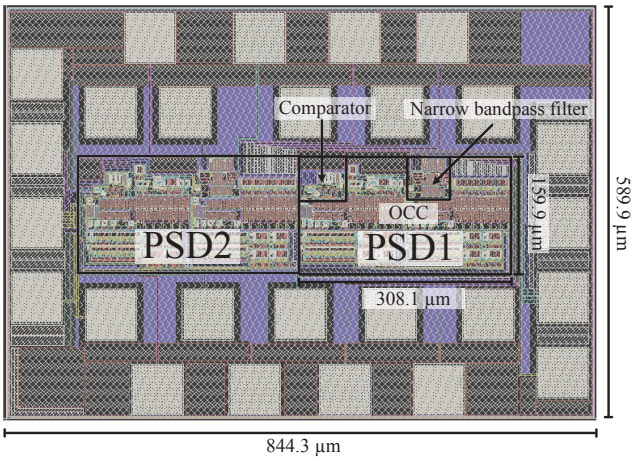

Fig. 9. The layout of the proposed design

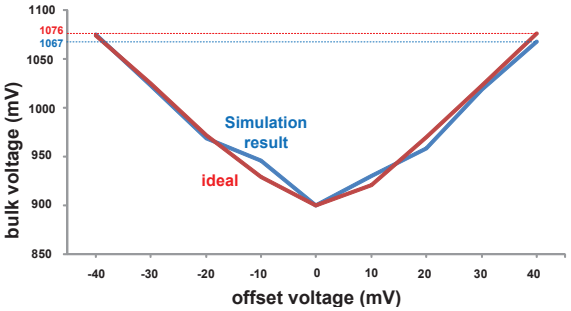

Fig. 10. The simulation results of the proposed OCC

V. CONCLUSION

This paper presents a phase shift detector with high accuracy for sensing applications. The proposed circuit is able to detect the phase difference from -90° to 90°. The maximum output error of the proposed PSD is 2.37%. Besides, the proposed PSD is able to generate a digital signal to demonstrate a quantitative data directly.

ACKNOWLEDGEMENT

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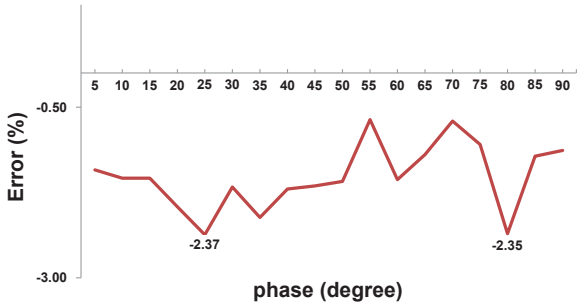

Fig. 11. The simulation results of the proposed PSD

REFERENCES

[1] F. Moeller, A. Rabah, S. M. Richie, and M. A. Belkerdid, "Differential phase shift keying direct sequence spread spectrum single SAW based correlator receiver," *IEEE Ultrasonics Symposium,* pp. 189-193, Oct. 1994.

[2] T. Hesjedal, W. Seidel, and H. Kostial, "Near-field phase shift photolithography for high-frequency SAW transducers," *IEEE Ultrasonics Symposium,,* pp. 247-250, Oct. 2002.

[3] F.-D. Lai, J.-M. Hua, and H.-M. Huang, "Application of an alternating phase-shifting mask design method to near-field photolithography for fabricating more than 2 GHz SAW devices," *IEEE Tran. on Ultrasonics, Ferroelectrics, and Frequency Control,* pp. 2208-2213, Oct. 2007.

[4] V. Radonic, G. Kitic, and V. Crnojevic-Bengin, "Novel Hilbert soil-moisture sensor based on the phase shift method," *IEEE Mediterranean Microwave Symposium,* pp. 377-380, Aug. 2010.

[5] J. Kondoh, S. Endo, and T. Nozawa, "Methanol sensor using shear horizontal surface acoustic wave devices for direct methanol fuel cell," *IEEE Inter. Ultrasonics Symposium,* pp. 743-746, Oct. 2012.

[6] W.-Y. Chang, P.-. Sung, C.-H. Chu, C.-J. Shih and Y.-C. Lin, "Phase detection of the two-port FPW sensor for biosensing," *IEEE Sensors Journal,* vol. 9, no. 5, pp. 501-507, May 2008.

[7] A. De Marcellis, G. Ferri, and E. Palange, "A novel analog autocalibrating phase-voltage converter for signal phase-shifting detection," *IEEE Sensors Journal,* vol. 11, no. 2, pp. 259-266, Feb. 2011.

[8] V. P. Chodavarapu, S. P. Khanolkar, E. C. Tehan, A. H. Titus, A. N. Cartwright, and F. V. Bright, "CMOS integrated optical sensor using phase detection," *Proc. IEEE Sensors,* pp. 1266-1270, Aug. 2003.

[9] S. S. Shanbhag, "CMOS integrated circuit for sensing applications," *IEEE Inter. Conf. on Embedded Systems and Design,* pp. 3-7, Jan. 2006.

[10] B. Sangjin, H.-S. Chung, H. Jongil, B.-H. Min, M.-Y. Park, and H.-K. Yu, "1-5.6 Gb/s CMOS clock and data recovery IC with a static phase offset compensated linear phase detector," *IET Circuits, Devices and Systems,* vol. 7, no. 3, pp. 159-168, May 2013.