A Primary-side Output Current Estimator with Process Compensator for Flyback LED Drivers

Zong-You Hou, Zong-Ying Ho, Jhih-Cheng You, and Chua-Chin Wang†, *Senior Member, IEEE*

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

***Abstract*—A primary-side output current estimator with process compensator for the flyback control circuits is designed and analyzed in this investigation. Flyback control circuits play a key role of smart lighting systems, where LED drivers require a compensator to keep the system stable. The process sensor is in charge of the detection of the chip process corner. Then, the process compensator correspondingly selects a comparator according to the output of the process sensor. Detailed analysis, including the method of the process sensor and the selection procedure of the process compensator, is reported. All-PVT-corner post-layout simulations of the proposed current estimator demonstrate 89.84 % efficiency, and 15.53 W power consumption given 5 V power supply and 50 kHz system clock rate.**

***Index Terms*—primary side, current estimator, flyback LED driver, process compensator**

I. Introduction

Many high energy-consuming and high pollution conventional technologies drive us to seek for substitute solutions which are high efficiency and environment-friendly technologies, e.g., lamp bulb vs. LED. LED has been recognized as the future lighting devices, since it attains longer operation time, more energy saving, and more compact compared to the counterpart lamp bulbs such as incandescent, fluorescent, and high intensity discharge (HID) devices [1], [2]. Therefore, white LED (WLED) has been widely used in automobile lighting, portable lighting, street lighting, residential lighting.

Nevertheless, the driver of the LED needs to keep pace with advancement of the LED technology, including the power management. For example, to achieve higher lightness, WLED requests a higher current with higher voltage drop with respect to conventional LEDs. However, high power dissipation becomes the price to pay.

The flyback driver has been recognized as an energy storage and converter isolator such that it is commonly used in LED lighting applications. To generate a stable voltage, an opto-coupler isolates the secondary side from the primary side in flyback drivers [3]. However, the switching components must sustain high voltage stress because conventional flyback driver systems demand a large current. Another critical problem for the conventional flyback drivers in boundary conduction mode (BCM) and discontinuous conduction mode (DCM) is the high peak current. Moreover, a primary detriment will increase the output power. Lin *et al.* presented a primary side control IC [4] to keep duty cycle as constant as possible. However, the current of the primary coil and the drain to source voltage of the power MOS switch will swing intensely when the bridge rectifier output voltage (Vin) is close to zero. Thus, the control IC must be reacted quickly enough to detect the valleys of the feedback signal, which is not practical in field applications.

The transfer function is very important for the LED system to analyze the system stability [5]. Therefore, the feedback circuit used in the flyback drivers must ensure its transfer function in the region of convergence. However, the transfer function of the LED system varies drastically with process variations, which will result in LED system instability.

A primary-side output current estimator with a process compensator for the flyback LED drivers is proposed in this work to resolve the mentioned problems. In Section II, the proposed design is shown and analyzed. Section III will demonstrate thorough simulation results to justify the performance of the proposed design. A conclusion is given in Section IV.

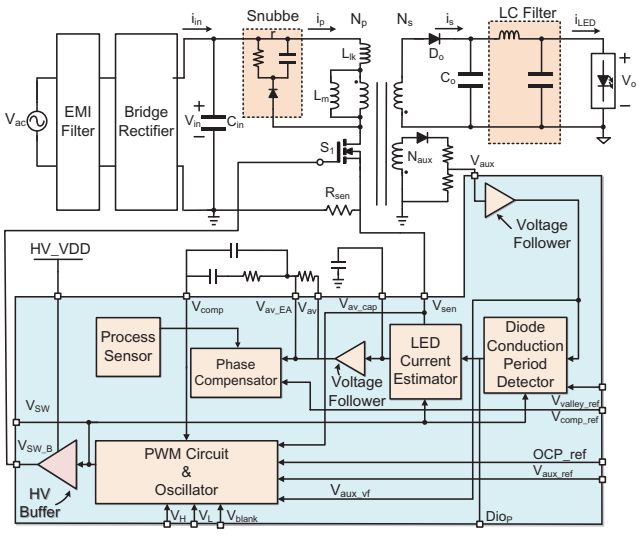

Fig. 1. Block diagram of the proposed flyback LED driver system.

†: Prof. C.-C. Wang is the contact author.

978-1-4673-6853-7/17/$31.00 ©2017 IEEE

II. Architecture of Flyback LED Driver

Referring to Fig. 1, a flyback LED driver system is shown, including a flyback driver and a flyback control circuit with the proposed process compensator. Because the inductor of flyback is split to work as a transformer, the flyback LED driver works like a buck-boost converter. On the other hand, the flyback control circuit decides the turn-on time of the switch (S_1) by detecting the output voltage of the auxiliary side. Therefore, the flyback control circuit can auto-adjusts the turn-on time of the S_1 to keep a fixed output current (i_{LED}).

The proposed flyback control circuit consists of a PWM circuit, a LED current estimator, a Diode conduction period detector, a Compensator, and a Process compensator. The LED current estimator generates a turn-off signal, which is compared with the sawtooth wave generated by PWM circuit. By tuning the period of the PWM circuit, the brightness of the LED can be adjusted. If S_1 is turned on, the LED current estimator generates a voltage proportional to the current of S_1. The diode conduction period detector is in responsible for estimating the conducting period precisely. The phase compensator is a conventional second order filter to adjust the dominant pole and the secondary pole such that the phase margin will be in 45 to 60 degree. However, the entire circuit is affected by process variations. Therefore, this work adds a process compensator to neutralize the effect caused thereby.

A. Diode Conduction Period Detector

Fig. 2 shows the schematic of the diode conduction period detector in Fig. 1. This circuit is designed to prevent misjudgment of the diode conduction period caused by the oscillation of V_{aux}. The falling edge of V_{SW} indicates that D_o is forward-biased. Thus, V_{aux} is raised up more than 0.2 V to pull Dio_P to high. By contrast, when D_o is reverse-biased, V_{aux} is compared with V_{aux_delay}, which is a delayed signal of V_{aux}, used to pull Dio_P to low. In addition, this circuit will ignore the oscillation of V_{aux}, because V_{sw} stays low.

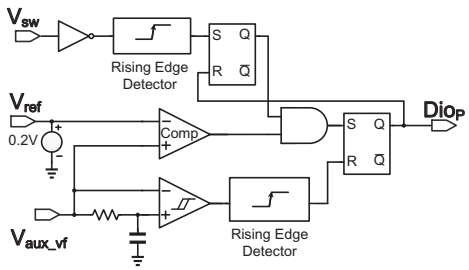

Fig. 2. Schematic of Diode Conduction Period Detector.

B. LED current estimator

Fig. 3 shows the schematic of the LED current estimator in Fig. 1. This circuit imitates operation of the S_1 to estimate i_{LED} by detecting V_{sen}. V_{sen} can be derived as follows.

$$V_{sen} = i_p \times R_{sen} \tag{1}$$

where i_p is the current of the primary side. Referring to [6], if the average over time is considered, V_{av} is written as Eqn. (2).

$$V_{av} = \frac{2R_{sen}}{n} \cdot i_{LED} \tag{2}$$

where n is the primary-to-secondary transformer turn ratio. In summary, i_{LED} can be indirectly estimated by V_{av} with an appropriate ratio $\frac{2R_{sen}}{n}$.

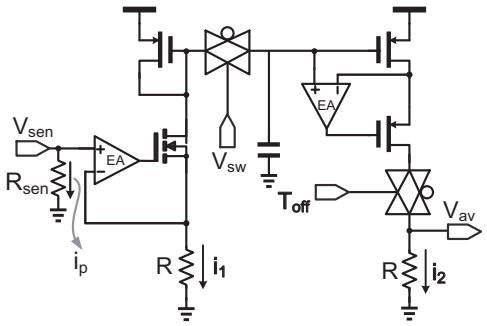

Fig. 3. Schematic of the LED current estimator.

C. Phase compensator

The phase compensator in Fig. 4 consists of an OPA, an OPA_comp, 2 transmission gates, 2 resistors, and 2 capacitors. The performance of amplifier is significantly affected by the process variation. Thus, an appropriate amplifier is used in the phase compensator to construct a second order filter according to the output of the process compensator. Furthermore, the second order filter can filter those signals with a frequency higher than that of AC power outlet to increase power factor. The transfer function is derived as follows.

$$\frac{V_{comp}}{V_{av}} = \frac{A_0/(1+s/w_p)}{1+(\frac{A_0}{1+s/w_p})(\frac{R_{CI}}{R_{CI}+(R_{FS}+1/sC_{FS})//(1/sC_{FP})})} \tag{3}$$

where A_0 is DC gain, w_p is dominant pole. Apparently, the performance of amplifier, namely A_0, is the key in the transfer function.

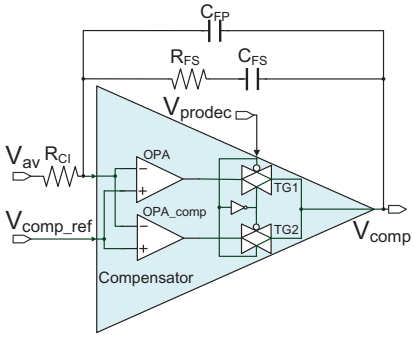

Fig. 4. Schematic of the phase compensator.

D. Process compensator

Process compensator shown in Fig. 5 is used to tell where the process corner is. It is composed of a process sensor and a process decision circuit. The process sensor is divided into two part : PMOS and NMOS threshold voltage sensors [7] as shown in Fig. 6 (a), and (b), respectively. Firstly, when the CLK is raised and reset_P is activated, net202 and VP is pulled up to VDD as well as net201 is discharged to $2\times V_{th,p}$, where $V_{th,p}$ is the threshold voltage of PMOS. Then, when the CLK is dropped, net201 and net202 are pulled to VDD as well as to VDD+$V_{th,p}$, respectively. Finally, the net202 is discharged to $3\times V_{th,p}$ as well as VP is also discharged to $5\times V_{th,p}$ by MP206 and MP208 when the CLK is raised high again. In the next cycle, net202 is pulled to $6\times V_{th,p}$ when the CLK is dropped. Furthermore, net202 is discharged to $8\times V_{th,p}$-VDD and VP is pulled up to $10\times V_{th,p}$-VDD when the CLK is raised. In summary, the relationship between $V_{th,p}$ and VP can be derived as follows.

$$VP(m) = 5m \times V_{th,p} - (m\text{-}1) \times VDD \tag{4}$$

where m is the number of CLK cycles in the PMOS threshold voltage sensor.

Similarly, the relationship between $V_{th,n}$ and VN can also be derived as follows.

$$VN(p) = p \times (VDD - 5 \times V_{th,n}) \tag{5}$$

where p is the number of CLK cycles in the NMOS threshold voltage sensor, and $V_{th,n}$ is the threshold voltage of NMOS.

Referring to Eqn. (4) and (5), the m and p will be attained corresponding to different process corners. The m and p can be used to determine which the five categories (ff, fs, tt, sf, and ss corners) of the process corner is in the process decision circuit. The LED system has the worst performance when NMOS is fast corner and PMOS is slow corner (namely FS). Therefore, V_{prodec} will turn on TG2 in the phase compensator (Fig. 4) and couple the output of the OPA_comp to V_{comp}.

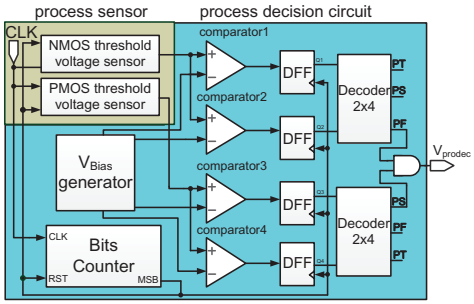

Fig. 5. Schematic of the proposed Process compensator.

E. Pulse Width Modulation

PWM circuit in Fig. 7 is a control signal generator of the power MOS switch. V_{ct}, which is a continuous sawtooth wave, is used to compare with other signals to determine the status of V_{sw}. Firstly, V_{sw} is turned on when V_{ct} is higher than V_{sw_set}. Then, V_{sw} is turned off when V_{ct} is higher than V_{comp}. Moreover, the valley detector means to reset V_{ct}, when the first valley of the V_{aux} is detected. On the other hand, V_{sw} is pulled down when the over-current protection is activated.

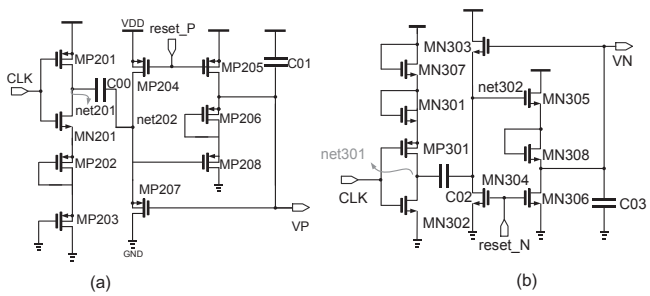

Fig. 6. Schematic of the proposed (a) PMOS threshold voltage sensor and (b) NMOS threshold voltage sensor.

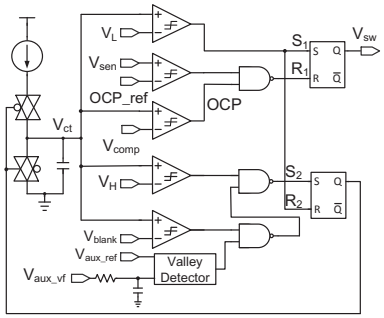

Fig. 7. Schematic of the PWM.

F. High-voltage Buffer

The high-voltage (HV) process we use to realize the proposed design offers low-voltage (LV) devices and HV devices. Referring to Fig. 8, the input of the HV buffer is converted to HV_VDD. Therefore, V_{sw} can be converted to an appropriate voltage level to drive power MOS, S_1.

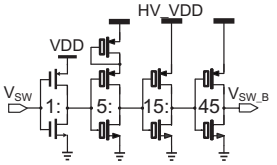

Fig. 8. Schematic of the HV Buffer

III. Implementation and Simulation

The proposed primary-side output current estimator with process compensator for the flyback LED driver is carried out using TSMC 0.5 μm CMOS high voltage mixed signal based LDMOS USG AL 2P3M polycide (T50UHV). Fig. 9 shows the layout, where the overall chip area is 782.4 × 1901.5 μm^2 and chip power consumption is 226.1 mW at 50 kHz

and VDD = 5 V. The all-corner post-layout simulation results of compensator's amplifier is shown in Fig. 10. Comparing with voltage and temperature variation, Fig. 10 (a) shows that the phase margin is more easily influenced by the process variation, especially FS corner. Therefore, the worst-case of the phase margin is enhanced from 37.89° to 60.01° by the proposed circuit as shown in Fig. 10 (b). The LED system power consumption is 15.53 W at 5 V and 50 kHz system clock rate. The performance comparison of the proposed design and several recent works is tabulated in Table I. Notably, only our design has process compensation and the efficiency is 89.84 % in the worst-case when the number of the LED string is 4 (34.28 Ω).

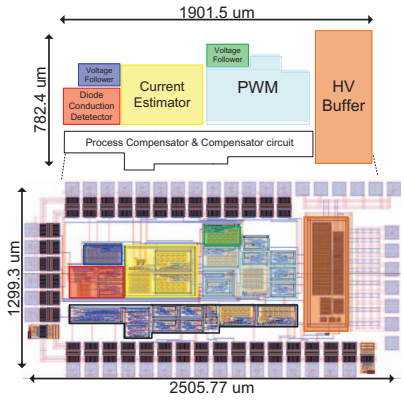

Fig. 9. Layout of the proposed design

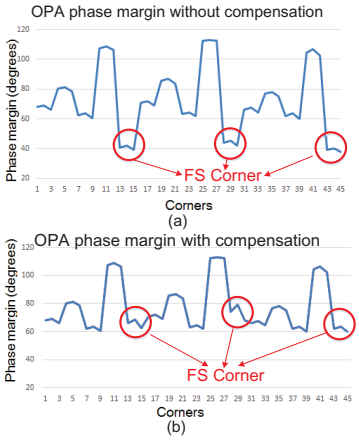

Fig. 10. Post-layout all-PVT-corner simulation of the proposed compensator

IV. Conclusion

In this paper, a primary-side output current estimator with process compensator for flyback driver control circuit IC is proposed. The proposed design is implemented using T50UHV. This work increases and maintain enough phase margin to prevent system from an unstable state caused by process variation. In summary, all-PVT-corner post-layout simulations of the proposed output current estimator demonstrates the 89.84 % efficiency when LED number is 4 (34.28 Ω).

TABLE I
Performance Comparison of LED Flyback Driver

	[8] APEC	[9] SSLCHINA	[10] ECCE	This work ISCAS
Year	2014	2014	2014	2016
Implementation	prototype	prototype	0.25 μm HV CMOS	0.5 μm HV CMOS
Switch Frequency (kHz)	125	25	100	50
Input Voltage Range (V)	90 ∼ 260	175 ∼ 265	90 ∼ 290	90 ∼ 260
Efficiency (%)	87	85	89.8	89.84
Power (W)	35	30	24	15.53
Chip Area (mm^2)	N/A	N/A	N/A	1.487
Process Compensator	N/A	N/A	N/A	yes
FOM‡	0.02	0.113	0.037	0.115

Note: ‡: FOM = Efficiency/(Power × Frequency)

Acknowledgment

This research was partially supported by Ministry of Science and Technology under grant MOST104-2622-E-006-040-CC2, MOST105-2221-E-110-058-, and MOST105-2218-E-110-006-. The authors would like to express their deepest gratefulness to CIC (Chip Implementation Center) of NARL (Nation applied Research Laboratories), Taiwan, for the thoughtful chip fabrication service.

References

[1] Y. Liu, D.-L Ding, C.-H Leung, Y.-K Ho, and M. Lu, "Optical design of a high brightness LED street lamp," in *Proc. Asia Communications and Photonics Conference and Exhibition (ACP)*, pp. 1-9, Nov. 2009.

[2] R. A. Pinto, M. R. Cosetin, M. Cervi, A. Campos, and R. N. do Prado, "Emergency lamp using high-brightness LED," in *Proc. International Symposium on Industrial Electronics (ISIE)*, pp. 257-262, Jun. 2011.

[3] W. Kleebchampee and C. Bunlaksananusorn, "Modeling and control design of a current-mode controlled flyback converter with optocoupler feedback," in *Proc. International Conference on Power Electronics and Drives Systems (PEDS)*, pp. 787-792, Nov. 2005.

[4] Y.-T. Lin, T.-J. Liang, and K.-H. Chen, "IC design of primary-side control for flyback converter," in *Proc. 2013 1st International Future Energy Electronics Conference (IFEEC)*, pp. 449-453, Nov. 2013.

[5] J. Cui, X. Yu, L. Wu, W. Xu, H. Qin, and L. Shao, "The control-loop design of quasi-resonant flyback converter for HI-bright LED driver," in *Proc. International Conference on Electrical and Control Engineering (ICECE)*, pp. 5045-5048, Sep. 2011.

[6] Z.-Y. Hou, T.-W Huang, and C.-C. Wang, "On-chip accurate primary-side output current estimator for flyback LED driver control," in *Proc. International Conference on IC Design and Technology (ICICDT)*, pp. 1-4, Jun. 2016.

[7] C.-C. Wang, C.-L. Chen, R.-C. Kuo, H.-Y. Tseng, J.-W. Liu, and C.-Y. Juan "On-chip process and temperature monitor for self-adjusting slew rate control of 2×VDD output buffers," *IEEE Trans. on Circuits and Systems I (TCAS-I)*, vol. 60, no. 6, pp. 1432-1440, Jan. 2013.

[8] P. Fang, and Y.-F. Liu, "Single stage primary side controlled offline flyback LED driver with ripple cancellation," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 3323-3328, Mar. 2014.

[9] Q. Zheng, W. Lin, Y. Xu, L. Wang, and N. Wu, "Research on a novel constant power control strategy for single-stage PFC LED driver," in *Proc. China International Forum on Solid State Lighting (ChinaSSL)*, pp. 5-8, Nov. 2014.

[10] J.-S. Li, T.-J. Liang, K.-H. Chen, Y.-J. Lu, and J.-S. Li, "Primary-side controller IC design for quasi-resonant flyback LED driver," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 5308-5315, Oct. 2015.