2×VDD Digital Output Buffer Insensitive to Process and Voltage Variations

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***Abstract*—A 2×VDD output buffer with process and voltage (PV) compensation technique is proposed to keep slew rate (SR) within predefined ranges regardless PV variations. The reason of temperature variation is not considered is that it is found to be relatively low correlated to slew rate for 90 nm process or better. All bias voltages in process and voltage variation detectors are generated from bandgap circuits such that variations have been guaranteed by simulation within less than 4.10%. The data rate is 650/500 MHz given 1.0/2.0 V supply voltage with 20 pF load, respectively, by physical measurements. The Δ SR improvement is 30.7% and 31.4% for 1×VDD and 2×VDD, respectively, when the proposed PV compensation design is activated.**

Keywords— I/O buffer, PV variation, mixed-voltage tolerant, slew rate compensation, gate-oxidxide reliability

I. Introduction

CMOS technologies have been developed rapidly with advantages, including low supply voltage, low fabrication cost per area, and low power consumption. However, many recent PCB-based applications still needs chips fabricated by legacy processes to achive certain functions, e.g., drivers. Therefore, when a PCB-based system is equipped with chips fabricated by different generations of CMOS process, which use different digital voltage levels, e.g., 1.8 V vs. 3.3 V, data exchange become an issue, where the slew rate is the major issue for digital transmission. Many researches in the past few years have been proposed to resolve problems given such a harsh SR condition such as over-stress problems, PVTL variations, which were mainly based on stacked architecture and variation detectors to compensate SR and increase reliability, respectively [1] - [6]. Besides, an improved digital-based process detector was also reported to simplify the detection mechanism and increase the detection speed [7].

However, if the temperature impact on SR variation is compared with those of process and voltage impact, as shown in Table I, the result by a Monte-Carlo simulation (100 times) shows that the impact of voltage and process variations is 3 times larger than that of the temperature. Therefore, the temperature detection can be ignored from I/O design, if the area cost is one of the major consideration factors. .

Based on the above simulation and observation, we propose to mainly focus on elimination approach againt process and voltage variations to compensate the SR. The delay mismatch resolution mentioned in [7] is also adopted in this design.

TABLE I
Comparison of Variation Factors to Slew Rate

VDD (V)	Corners	Temp. (°C)	ΔRise (V/ns)	ΔFall (V/ns)	Correlation Ratio (Rise/Fall)
0.9-1.1×VDD	TT	25	2.08	1.93	4.1/3.64
1×VDD	All	25	1.78	1.74	3.63/3.28
1×VDD	TT	0-100	0.49	0.53	1/1

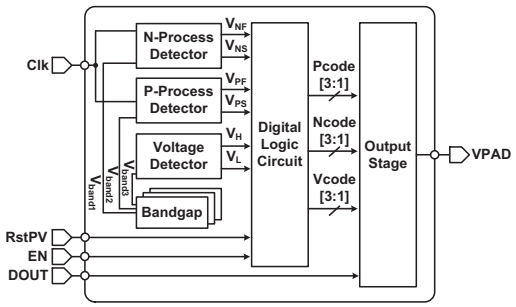

Fig. 1. Block diagram of the proposed 2×VDD digital output buffer.

II. 2×VDD Output Buffer Immune to PV Variations

Referring to Fig. 1, the proposed output buffer consists of N-Proccess Detector, P-Process Detector, Voltage Detector, 3 Bandgap circuits, Digital Logic Circuit, and an Output Stage. Notably, Clk is the system clock, and DOUT is the digital signal given by the internal digital core to be transmitted outward. RstPV and EN are 2 control signals for Digital Logic Circuit. The operation of the proposed design is outlined as follows.

1). Clk drives PMOS Detector and NMOS Detector at the same time. Each detector generates a ramping voltage to be compared with the output voltage of the corresponding bandgap circuit such that the delay of each detector will be measured simultaneously and independtly. V_{PS} and V_{PF} are then generated by the PMOS detection path, while V_{NS} and V_{NF} are generated by the NMOS ounterpart.
2). The voltage detection is carried out by comparing two voltages generated by a PMOS string with a pre-defined voltage generated by the 3rd bandgap circuit. V_H and V_L

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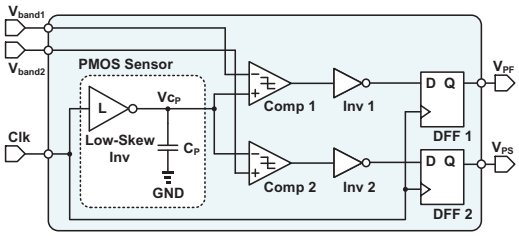

Fig. 2. Schematic of P-Process Detector.

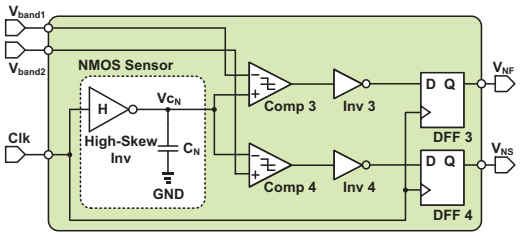

Fig. 3. Schematic of N-Process Detector.

will then be generated and devlievered to the following Digital Logic Circuit.

3). Digital Logic Circuit is basically an encoder to encode the mentioned output signals, namely, V_{PS}, V_{PF}, V_{NS}, V_{NF}, V_H, and V_L into 3 groups of digital signals, Pcode [3:1], Ncode [3:1], and V[3:1] to drive the large transistors in the Output Stage.

4). The swing of the digital output is allowed to be 1×VDD or 2×VDD depending on the VDDIO in Output Stage. Meanwhile, the on-off status of 6 driving PMOS transistors and 6 driving NMOS transistors is respectively determined by the digital outputs of Digital Logic Circuit such that the slew rate variation caused by process and voltage variations is reduced significantly.

A. Process variation detector

As mentioned earlier, the core of the proposed design is to estimate or find out what process corner the die is such that the compensation of the associated process variation is feasible. Referring to Fig. 2, P-Process Detector comprises a PMOS Sensor, 2 comparators (namely Comp1 and Comp2), 2 inverters, and 2 DFFs (D flip flop). To maginfy the process variation impact upon the signal timing, the aspect ratio (W/L) of the PMOS in the PMOS Sensor is relatively smaller than that of a regular inverter, while the aspect ratio of the NMOS therein in relatively large. Therefore, due to the long length of the pull-up and the large width of the pull-down, V_{C_P} at C_P will turn out to be a slow ramping but fast droping waveform. V_{C_P} is then compared with two pre-defined voltages, namely V_{band1} and V_{band2}, using Comp1 and Comp2, respetively. Notably, since Clk is an external clock with 50% duty cycle, it will sample the inverted outputs of the 2 comparators (V_{PF} and V_{PS}) and latch them into DFF1 and DFF2, respectively.

If the PMOS resides in the Slow corner, V_{C_P} will be charged slower such that V_{C_P} can not be rasied over V_{band1} and V_{band2}. Therefore, V_{PF} and V_{PS} will sampled as low at the rising edge of Clk. If the PMOS is in the Typical corner, V_{C_P} will be raised between V_{band1} and V_{band2} such that the outputs of DFF1 and DFF2, namely, V_{PF} and V_{PS}, are respectively latched with low (GND) and high (VDD). Finally, if the PMOS is "Fast", V_{C_P} will be charged over V_{band1} and V_{band2} to make V_{PF} and V_{PS} both registered with VDD. As soon as the above detection is done, which means Clk becomes high, the pull-down NMOS in the Low-Skew inverter will be turned on to ground V_{C_P}.

The counterpart of the P-Process Detector is the N-Process Detector, as shown in Fig. 3, consisting of an NMOS Sensor, 2 comparators (namely Comp3 and Comp4), 2 inverters, and 2 DFFs. The NMOS Sensor is a high-skew inverter composed of 2 NMOS transistors and a capacitor, C_N. The operation of the N-Process Detector is very similar to that of the P-Process Detector. As soon as the falling edge of Clk appears, the pull-up NMOS of the High-Skew inverter is turned on to charge C_N. That is, V_{C_N} at C_N is charged from GND gradually. If the NMOS resides in the Slow corner, the charging will be slow. When Clk transits from GND to VDD, namely rising edge, DFFs will be triggered to sample V_{NF} and V_{NS}, respectively. Since NMOS is assumed to be Slow, V_{C_N} can not be charged over 2 pre-defined bias voltages, i.e., V_{band1} and V_{band2} such that V_{NF} and V_{NS} are both 0. If it is in the Typical corner, V_{C_N} will stay between V_{band1} and V_{band2}such that V_{NF} and V_{NS} become 0 and logic 1, respectively. The last case is that when it is in th Fast corner, both of V_{NF} and V_{NS} are registered with 1. When the detection is done, the pull-down NMOS of the High-Skew inverter will be asserted to ground V_{C_N} and wait for the next falling edge to start another cylce of detection.

In short, the above senarios are summarized in the following Table II.

TABLE II
FUNCTION TABLE OF PROCESS DETECTORS

P Process Detector			
	V_{C_P}	V_{PF}	V_{PS}
Fast	$V_{C_P} > V_{band1} > V_{band2}$	Logic 0	Logic 0
Typical	$V_{band1} > V_{C_P} > V_{band2}$	Logic 1	Logic 0
Slow	$V_{band1} > V_{band2} > V_{CP}$	Logic 1	Logic 1
N Process Detector			
	V_{C_N}	V_{NF}	V_{NS}
Fast	$V_{C_N} > V_{band1} > V_{band2}$	Logic 0	Logic 0
Typical	$V_{band1} > V_{C_N} > V_{band2}$	Logic 1	Logic 0
Slow	$V_{band1} > V_{band2} > V_{C_N}$	Logic 1	Logic 1

B. Voltage detector

Referring to Fig. 4, the schematic of Voltage Detector is disclosed. A string of 9 diode-connected PMOS transistors are divided into 3 groups correspding to 3 subranges from VDD to GND : VDD $\sim V_H$, $V_H \sim V_L$, $V_L \sim$ GND [8]. It is easy to tell what the voltage variation is by such a configuration, since the variation of VDD between ±10% VDD can be directly sensed. The 9 PMOS transistors have the same size to auto-cancel the effect caused by process and temperature variations. That is, although the resistance of diode-connected MOS under

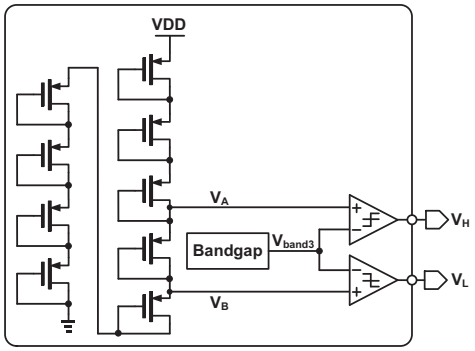

Fig. 4. Schematic of Voltage Detector [8]

different variations will drift, the voltages, V_H and V_L, are equally drifted as well. Therefore, when it comes to $\pm 10\%$ VDD variations, the output voltage of the bandgap circuit will be fluctuated between +1.49% and -1.26%. Detailed function is summarized in Table III.

TABLE III
FUNCTION TABLE OF VOLTAGE DETECTOR

Voltage Level	V_H	V_L
+10% VDD	Logic 1	Logic 1
VDD	Logic 1	Logic 0
-10% VDD	Logic 0	Logic 0

C. Digital logic

Process Detector and Voltage Detector deliver compensation signals, namely V_{PF}, V_{PS}, V_{NF}, V_{NS}, V_H, and V_L, to Digital Logic Circuit. EN forces Output Buffer to turn on all current paths. Notably, the priority of signal EN is higher than that of RstPV. RstPV = 0 will be in charge of turning on compensation mechanism. Then, Pcode [3:1], Ncode [3:1], and Vcode[3:1] are generated by hard-wired logic circuitry to drive different current paths of Output Buffer. By contrast, when RstPV = 1, Pcode [3:1], Ncode [3:1], and Vcode[3:1] are all set to (0 1 1) regardless whatever the outcome of Process Detector and Voltage Detector is.

D. Output stage

The schematic of Output Stage is shown in Fig. 5, consisting of Pre-Driver, Level Shifter, VDDIO Detector, and Driving Transistors. Pre-Driver receives the input signal DOUT, Pcode [3:1], Ncode [3:1], and Vcode[3:1] and utilizes a hard-wired encoder to generate a total of 12 signals, where $V_{pa1}, V_{pb1}, V_{pc1}$ and $V_{pa2}, V_{pb2}, V_{pc2}$ are coupled to the Level Shifter, while $V_{n201a}, V_{n201b}, V_{n201c}$ and $V_{n202a}, V_{n202b}, V_{n202c}$ are directly used as gate drives, respectively, to N201a, N201b, N201c, N202a, N202b, and N202c. Notably, when it comes to 2×VDD scenario, a V_{g2} will be generated to Level Shifter by VDDIO Detector. VDDIO detects the voltage level of VDDIO, which notifies Level Shifter to shift up the gate drives. Level Shifter will then shift up $V_{pa1}, V_{pb1}, V_{pc1}$ and $V_{pa2}, V_{pb2}, V_{pc2}$ to be gate drives of PMOS driving transistors to prevent over-stressed problems. Table IV revealed the internal voltage levels in Output Stage.

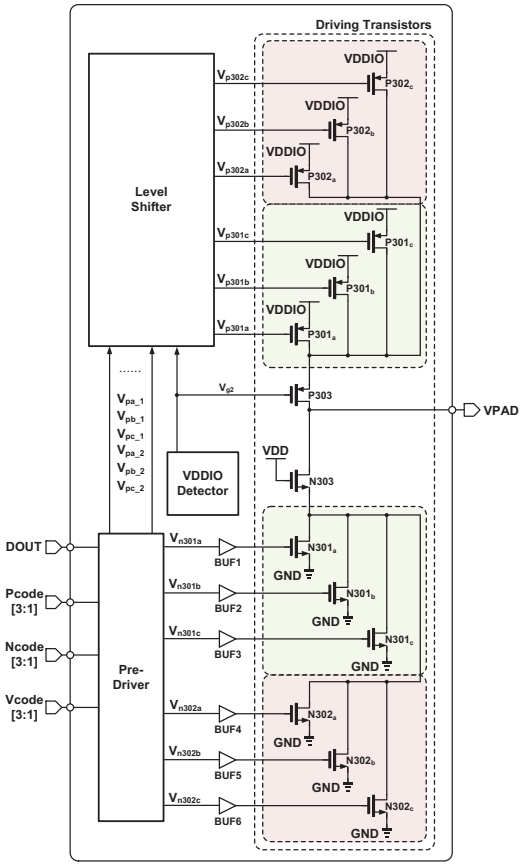

Fig. 5. Schematic of Output Stage in Fig. 1.

TABLE IV
VOLTAGE LEVELS OF DRIVING SIGNALS

VDDIO(V)	V_{p201x},V_{p202x}(V)	V_{g2}(V)	V_{n201x},V_{n202x}(V)
1.0	0.0/1.0	0.0	1.0/0.0
2.0	1.0/2.0	1.0	1.0/0.0

III. IMPLEMENTATION AND MEASUREMENT

The proposed design is realized by TSMC 90 nm CMOS Mixd Signal MS General Purpose Standard Process LowK Cu 1P9M 1.0 & 3.3 V. Fig. 6 shows the die photo of the prototype on silicon, where a single I/O buffer circuit is only 0.388 × 0.052 mm^2. Referring to Fig. 7, the slew rate enhancement for VDDIO = 1.0/2.0 V is 30.7% and 31.4%, respectively, with and without the proposed PV compensation. The maximum data rate of the proposed design is measured to be 650 MHz/500 MHz given VDD=1.0/2.0, respevtively, with the activated PV ccompensation. Table V summarizes the comparison of our work with several prior works. Apparently, the proposed design provides a high-speed all-corner-detected solution for 2×VDD data transmission on silicon with the best improevement on SR.

IV. CONCLUSION

A 2×VDD I/O buffer with the encoded PV compensation technique is reported in this work to regulate slew rate. The data rate is measured on silicon as 650/500 MHz when VDDIO = 1.0/2.0 V, respectively. The SR improvement is proved to be at

TABLE V
PERFORMANCE COMPARISON OF OUTPUT BUFFERS

	[3] *TCAS-I 2013*	[5] *ISCAS 2013*	[6] *EDSSC 2014*	[8] *ISCAS 2016*	This work
Process (nm)	90	40	90	90	90
Implementation	measurement	simulation	simulation	simulation	measurement
VDD (V)	1.2	0.9	1.0	1.0	1.0
VDDIO (V)	2.5	0.9/1.8	1.0/1.8	1.0/2.0	1.0/2.0
Process Corner Detected	Only TT FF SS	All	All	All	All
Lock Time	One cycle	Tens of cycle	$\geq$ One cycle	One cycle	One cycle
Maximum Date Rate (MHz)	N/A	460	330/500	800/500	650/500
SR Variation Improvement (%)	37.5	6	N/A	33.9	30.7 (Worst case)
Encoded compensation	NO	NO	YES	YES	YES
Core area (mm^2)	N/A	0.013	0.024	0.020	0.020

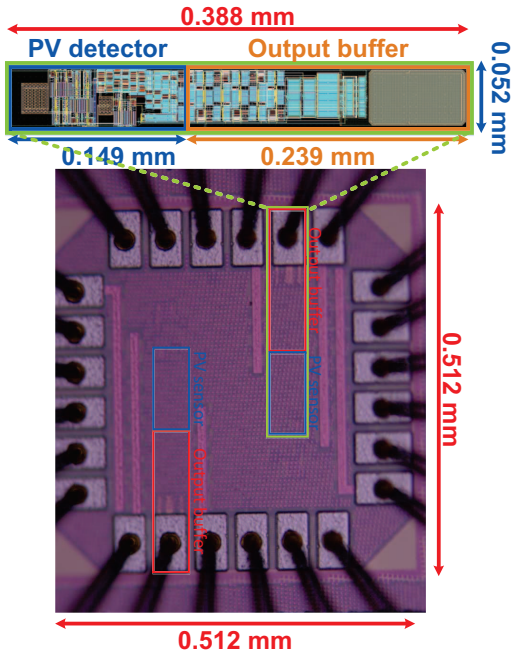

Fig. 6. Die photo of the proposed output buffer.

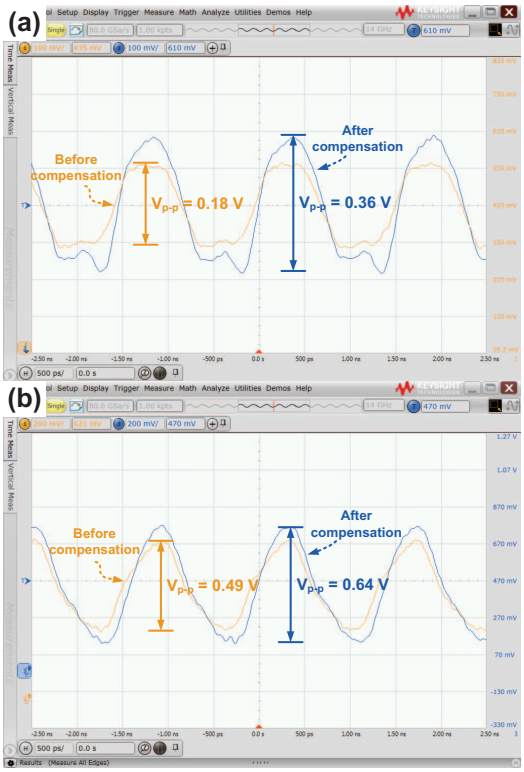

Fig. 7. Improvement of SR variation with/without PV compensation.

least over 30% regardless in VDD or 2×VDD data transmission mode.

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