# A PVT Validation Phase-Lock Loop with Multi-Band VCO Applied in Closed-Loop FOGs

1st Tsung-Yi Tsai
*Department of Electrical Engineering*
*National Sun Yat-Sen University*
Kaohsiung, Taiwan 80424
zack@vlsi.ee.nsysu.edu.tw

2nd Ting-Sheng Wang
*Department of Electrical Engineering*
*National Sun Yat-Sen University*
Kaohsiung, Taiwan 80424
w810@vlsi.ee.nsysu.edu.tw

3rd Yi-Jen Chiu
*Department of Photonics*
*National Sun Yat-Sen University*
Kaohsiung, Taiwan 80424
yjchiu@faculty.nsysu.edu.tw

4th Chua-Chin Wang†
*Department of Electrical Engineering*
*National Sun Yat-Sen University*
Kaohsiung, Taiwan 80424
ccwang@ee.nsysu.edu.tw

***Abstract*—This work presents a phase-lock loop (PLL) applied in closed-loop fiber-optic gyroscope (FOG) systems. Multi-band VCO not only reduces the gain of VCO and the corresponding jitter, but also resists PVT (process, voltage, temperature) variation to meet the automobile grade demand. The proposed PLL is realized by TSMC 40nm CMOS process to demonstrate 9 transfer functions selected by thermometer codes, where the worst case P2P (peak-to-peak) jitter is 15 ps at 0.99V, 100°C, FF corner by all-PVT-corner post-layout simulations.**

***Index Terms*—low jitter, PLL, multi-band, VCO, thermometer code, closed-loop, FOG, PVT**

## I. Introduction

Fiber-optic gyroscope (FOG) with high reliability, which can be completed solid state realized, has been developed in space and aviation industry for at least a decade. To have better linearity, wide dynamic range, and higher accuracy, the closed-loop system is considered as a better option than the open-loop counterpart to achieve these aspects. However, a closed-loop system is far more complicated, where PVT (process, voltage, and temperature) variations of semiconductor technologies, make the realization of a reliable clock source with low power, low jitter and fast lock time very difficult.

With reference to the FOG realization by semiconductor technologies, PVT variation is undoubted a basic problem needed to be validated. For PLL designs, many previous works have been presented to achieve low power [1] [2], low jitter [3] [4] [5], and fast lock time [6] [7]. Referring to [1], a 3rd-order low pass filter (LPF) as well as pre-scaler and divider were used to decrease the area and power consumption. In [3] and [4], VCO with a current sink bias circuit was used to reduce the jitter. Digital PLLs with modified phase detector (PD) have good response on lock time [6] [7]. Notably, large jitter is usually generated from oversized lock range and high gain K in VCO. Therefore, a multi-band technique was presented to lower the gain of VCO and then lower the jitter as well in [4], [8]- [10].

†: Prof. Chua-Chin Wang is the contact author.

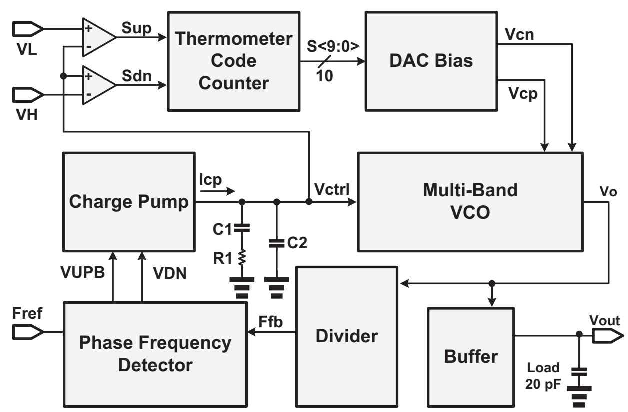


Fig. 1. System blocks of the proposed PLL with multi-band VCO.

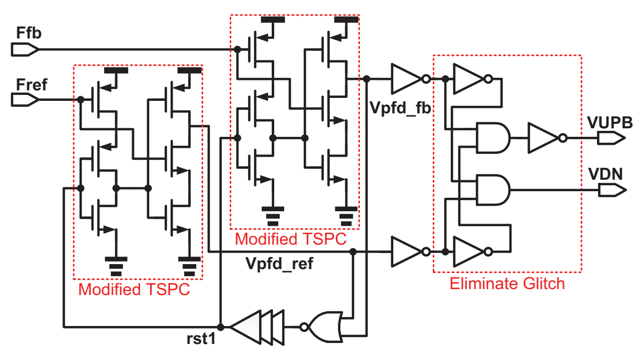


Fig. 2. Phase frequency detector with glitch elimination.

According to the mentioned problems, this work presents a PLL with multi-band VCO and PVT resistance feature. The input and output frequencies for the target FOG system, namely Fref and Fout, are 100 MHz and 1GHz, respectively.

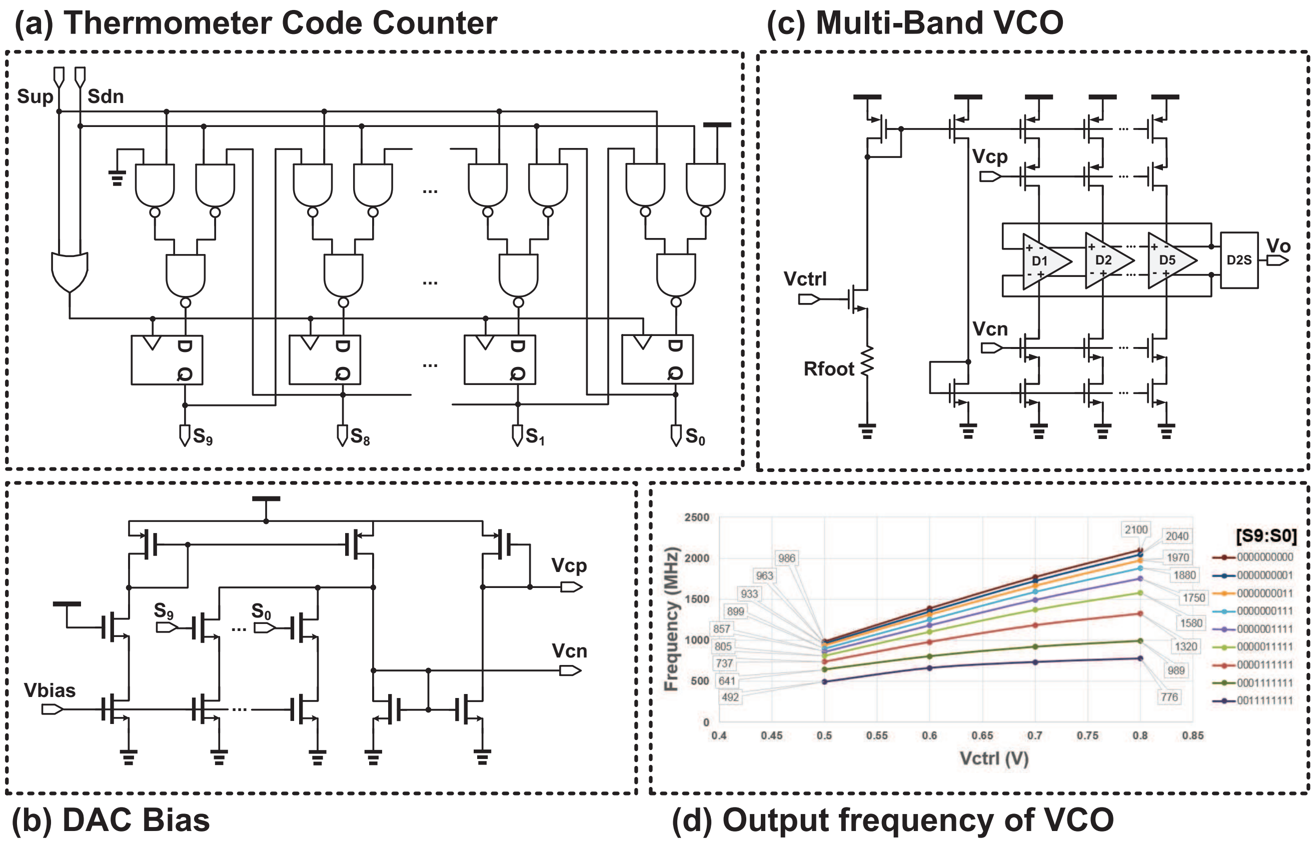


Fig. 3. Schematic of (a) thermometer code counter, (b) DAC bias, and (c) multi-band VCO. (d) Output frequency of multi-band VCO at TT corner, 25°C

## II. Phase-Lock Loop Circuit Design for FOGs

Fig. 1 shows the system view of the proposed PLL, which contains a Phase Frequency Detector (PFD), a Charge Pump, a 2nd-order LPF, Multi-Band VCO with Thermometer Code Counter and DAC Bias, a Buffer, and a Divider.

### A. Phase Frequency Detector and Charge Pump

Fig. 2 shows the schematic of PFD, which is composed of two positive-edge-triggered modified true single-phase-clock (TSPC). It will detect two clock signals from reference clock (Fref) and feedback clock (Ffb) to see which one is leading. If Ffb is leading, Vpfd_fb will be raised up to logic 1 to turn on VDN no matter the leading is generated by different frequency or phase variation. Then, the charge pump will discharge Vctrl. Otherwise, if Fref is leading, VUPB will be turned on to charge Vctrl.

### B. LPF and VCO Parameter Design

A 2nd-order LPF is used to compensate the system as shown in Fig. 1. Before calculating the value of passive elements shown in Fig. 1, the gains of PFD and VCO must be decided first, which are shown in Eqn. (1) and (2), respectively, in Table I. Then, the phase margin (PM) is set to 60° and the crossover frequency $F_3$ is 10 MHz. According to Eqn. (4) and (5), pole and zero are calculated to be $3.731\times10^{7}$ and $2.678\times10^{6}$ Hz. Therefore, the value of C2, C1, and R1 are tabulated is Eqn. (6) - (8). However, when it comes to

TABLE I
Logic function table of the RCA unit

| Function | Value | Eqn. |
|---|---|---|
| $K_{PFD} = \frac{Icp}{2\pi}$ | $1.592\times10^{-5}$ (rad/v) | (1) |
| $K_{VCO} = \frac{F_2 - F_1}{V_2 - V_1} \times 2\pi$ | $1.802\times10^{10}$ (rad/v) | (2) |
| PM = $60^o$ | | |
| $\omega_c = 2\pi \times F_3$ | $62.8\times10^{6}$ (rad/v) | (3) |
| $\iota_p = \frac{\sec(\theta_{PM}) - \tan(\theta_{PM})}{2\pi}$ , $f_p = \frac{1}{2\pi\iota_p}$ | $3.731\times10^{7}$ (Hz) | (4) |
| $\iota_z = \frac{1}{\omega_c^2 \times \iota_p}$ , $f_z = \frac{1}{2\pi\iota_z}$ | $2.678\times10^{6}$ (Hz) | (5) |
| $C2 = \frac{K_{PFD} \cdot K_{VCO} \cdot \iota_p}{\omega_c^2 \cdot \iota_z \cdot N} \cdot \sqrt{\frac{1+(\omega_c \cdot \iota_z)^2}{1+(\omega_c \cdot \iota_p)^2}}$ | 1.949 (pF) | (6) |
| $C1 = C2 \cdot (\frac{\iota_z}{\iota_p} - 1)$ | 25.24 (pF) | (7) |
| $R1 = \frac{\iota_z}{C1}$ | 2.354 (kΩ) | (8) |
| $K_{VCO1} = 5.95 \times 10^{9} \rightarrow$ PM = $79.8^o$ | | |

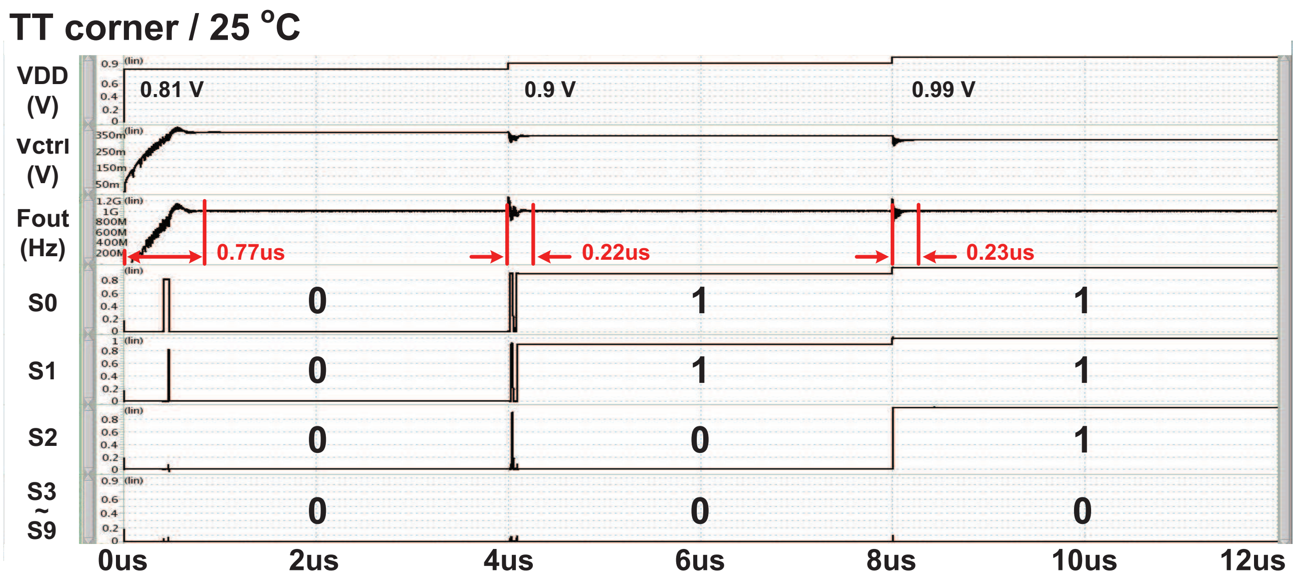


Fig. 4. Post-layout simulation waveforms of thermometer code [S9:S0] given different supply voltage.

multi-band VCO given such a RC value, the low gain $K_{VCO1}$ becomes $5.95 \times 10^9$, which gives a better PM = $79.8^o$.

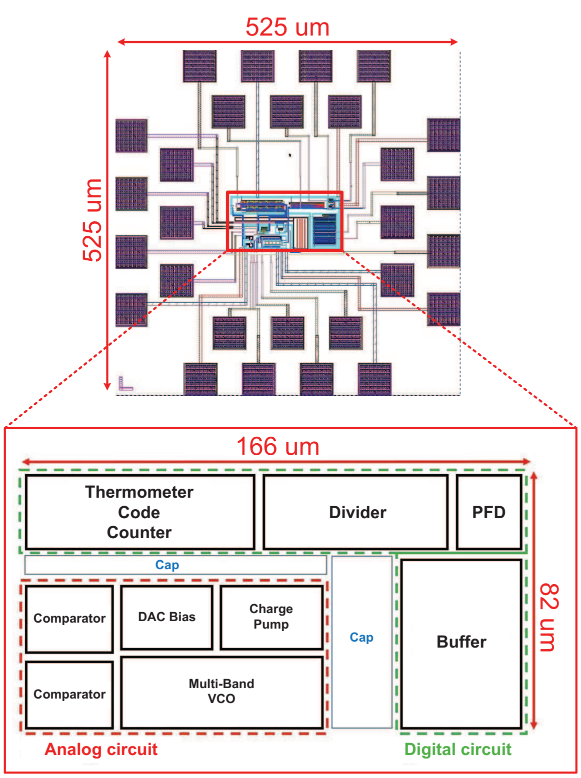


Fig. 5. Layout of the proposed PLL.

### C. Multi-band VCO

Referring to Fig. 3 (a), (b), and (c), the schematics of thermometer code counter, DAC Bias, and multi-band VCO are shown, respectively. Sup and Sdn is the comparison result between Vctrl and VL, VH. Initial condition of [S9:S0] is 000000000. If Vctrl exceeds VH, which means the PLL can't lock the frequency in the previous state, Sdn will be logic 1 and then turn [S9:S0] into 000000001. It will turn on different current paths in Fig. 3 (b) to adjust the bias voltage Vcp and Vcn in Fig. 3 (c). Output frequency of VCO with different [S9:S0] is shown in Fig. 3 (d) at TT corner, 25°C. However, if the frequency still can't be locked, the code of thermometer will keep counting up to the final band [S9:S0] = 011111111.

## III. Layout and Simulation Results

The proposed work is carried out and simulated using TSMC 40 nm CMOS process. Fig. 4 is the post-layout simulation waveform of [S9:S0] given different supply voltages. Notably, the process and temperature is at fixed TT corner and 25°C. Firstly, the supply voltage is 0.81 V and the system takes 0.77 $\mu s$ to lock at 1 GHz with [S9:S0] = 0000000000. Secondly, the supply voltage is then raised up to 0.9 V and takes 0.22 $\mu s$ to lock at 1 GHz with [S9:S0] = 0000000011. Finally, given the supply voltage 0.99 V, the system will lock the frequency after 0.23 $\mu s$ with [S9:S0] = 0000000111. It shows that the presented PLL with multi-band VCO can actually lock the frequency regardless PVT variations.

Fig. 5 shows the layout of PLL, where whole area is 525 $\mu$m $\times$ 525 $\mu$m. Notably, core area is 166 $\mu$m $\times$ 82 $\mu$m. Table II shows the comparison table with several previous works. Our work attains the lowest P2P jitter, and has been demonstrated

TABLE II
PLL PERFORMANCE COMPARISON TABLE

| | *JSSC* [3] 2010 | *TCAS-II* [4] 2014 | *TCAS-I* [6] 2015 | *VLSID* [7] 2016 | *MWSCAS* [9] 2011 | *IWS* [10] 2018 | This work 2019 |
|---|---|---|---|---|---|---|---|
| Process (nm) | 130 | 65 | 180 | 65 | 130 | 40 | 40 |
| Supply voltage (v) | 1.2 | 0.4 | 1.8 | 0.4 | 0.5 | 0.9 | 0.9 |
| Frequency (GHz) | 1.35 | 0.35 | 1.25 | 5 | 0.4 | 3.2 | 1 |
| Oscillator type | Ring VCO | Ring VCO | Ring DCO | QDCO | Ring DCO | Ring DCO | Ring VCO |
| Implementation | Meas. | Meas. | Meas. | Post-layout sim. | Pre-layout sim. | Post-layout sim. | Post-layout sim. |
| RMS jitter (ps) | 3.7 | 30.8 | 8.884 | 1.7 | N/A | 5.1 | 5.81 (0.9V / 25°C / TT) |
| P2P jitter (ps) | 32 | N/A | 32.5 | N/A | 30.23 | N/A | 15 (0.99V / 100°C / FF) |
| Lock time ($\mu$s) | 7.5 | N/A | 2.9184 | 1.5 | N/A | N/A | 3.58 (0.9V / -55°C / SS) |
| Power (mW) (mW) | 16.5 | 0.109 | 32 | 25 | 0.37 | 5.05 | 8.7066 (0.99V / 100°C / FF) |
| Core area ($\mathrm{mm}^2$) | 0.2 | 0.0081 | 0.7735 | 1 | N/A | 0.045 | 0.0136 |
| $\mathrm{FOM}_1$ (dB) | -197.7 | -215.3 | -194.7 | N/A | N/A | -213.8 | -225 (0.9V / 25°C / FF) |
| $\mathrm{FOM}_2$ (dB) | -216.46 | N/A | -205.97 | -221.4 | -210.7 | N/A | -216.6 (0.9V / -55°C / SS) |

$\mathrm{FOM}_1 = 10 \cdot \log \left[(\text{RMS jitter(s)})^2 \times \text{Power(mW)}\right]$
$\mathrm{FOM}_2 = 10 \cdot \log \left[(\text{P2P jitter(s)})^2 \times \text{Power(mW)}\right]$
Meas. = Measurement / Sim. = Simulation

to be functionally correct among various PVT variations. Besides, 2 different FOMs (figure of merit) comparison, namely $\mathrm{FOM}_1$ and $\mathrm{FOM}_2$ (in dB), also show the superiority of the proposed design.

## IV. CONCLUSION

This work utilizes TSMC 40 nm process to present a phase-clock loop using multi-band VCO, which reduces jitter and resists PVT variations. Our work achieves the lowest 15 ps P2P jitter at 0.99V, 100°C, FF corner, which will be very much needed in FOG systems.

## ACKNOWLEDGMENT

The investigation was partially supported by Ministry of Science and Technology (MOST), Taiwan, under grant MOST 107-2218-E-110-004- and MOST 107-2218-E-110-016-. The authors would like to express our deepest gratefulness to TSRI (Taiwan Semiconductor Research Institute) in NARL (Nation Applied Research Laboratories), Taiwan, for the assistance of thoughtful chip fabrication.

## REFERENCES

[1] K. Lee, C. Hong, H. Ying, D. Kim, S.-H. Kim, and S.-M. Park, "A 6.6 mW, -94 dBc/Hz, 1.0-to-4.5 GHz phase-lock loop in 65-nm CMOS," *Inter. SoC Design Conf. (ISOCC),* pp. 235-236, Nov. 2015.

[2] J. Luo, L. Zhang, L. Zhang, Y. Wang, and Z. Yu, "A 24GHz low power and low phase noise PLL frequency synthesizer with constant KVCO for 60GHz wireless applications," *Inter. Symp. on Circuits and Systems (ISCAS),* pp. 2840-2843, May 2015.

[3] D.-S. Kim, H. Song, T. Kim, S. Kim, and D.-K. Jeong, "A 0.3-1.4 GHz all-digital fractional-N PLL with adaptive loop gain controller," *IEEE J. Solid State Circuits (JSSC),* vol. 45, no. 11, pp. 2300-2311, Nov. 2010.

[4] J.-W. Moon, K.-C. Choi, and W.-Y. Choi, "A 0.4-V, 90 350-MHz PLL with an active loop-filter charge pump," *IEEE Trans. on Circuits and Systems II: Express Briefs (TCAS-II)*, pp. 319-323, May 2014.

[5] B. Yuan, and H. Liu, "A generalized low power and lower jitter charge pump PLL," *IEEE Inter. Workshop on Microwave and Millimeter Wave Circuits and System Technology*, pp. 471-474, Oct. 2013.

[6] J.-M. Lin, and C.-Y. Yang, "A fast-locking all-digital phase-locked loop with dynamic loop bandwidth adjustment," *IEEE Trans. on Circuits and Systems I: Regular Papers (TCAS-I)*, vol. 62, no. 10, pp. 2411-2422, Oct. 2015.

[7] P. Paliwal, J, Fadadu, A. Chawda, and S. Gupta, "A fast settling 4.7-5 GHz fractional-N digital phase locked loop," *Inter. Conf. on VLSI Design (VLSID)*, pp. 553-554, Jan. 2016.

[8] K.-C. Kuo, and Y.-H. Hsu, "A low power multi-band selector DLL with wide-locking range," *IEEE Inter Conf. on Integrated Circuit Design and Technology and Tutorial (ICICDT)*, pp. 25-28, Jun. 2008.

[9] W.-H. Chen, W.-F. Loke, and B. Jung, "A PVT-tolerant, ultra-low-power phase-locked loop for wireless implantable biomedical devices," *IEEE Inter. Midwest Symp. on Circuits and Systems (MWSCAS)*, pp. 1-4, Aug. 2011.

[10] Z. Wang, T. Hu, J. Yang, N. Xi, and F. Lin, "A 100 MHz-3.2 GHz 5.1 mW area-efficient PLL clock generator," *IEEE MTT-S International Wireless Symposium (IWS)*, pp. 1-3, May 2018.