A PVDF-film Energy Harvesting Circuit Using 40-nm CMOS Process

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***Abstract*—This paper presents an energy harvest circuit design integrated with piezoelectric devices made of polyvinylidene fluoride (PVDF) films. The piezoelectric devices will be used in wearable electronics, e.g., insole and clothes, to prevent child or elderly missing. The proposed design consists of a low-voltage piezoelectric energy harvest circuit, PVDF films, and discretes, which will be integrated with Bluetooth low-energy (BLE) Tx/Rx. Therefore, when the kid or elder is out of a pre-defined distance, the missing beacon via Bluetooth devices will alarm to the family so take actions. The harvest circuit is realized using TSMC 40nm CMOS process, wherein the proposed 2-stage stepping-up architecture boosts the generated from 120 mV to 1 V. Since the output of PVDF film is an AC signal, an AC/DC converter based on a voltage multiplier not only carries out AC/DC conversion, but also elevate the DC voltage to 0.26 V, which is then through boosted by DC/DC converter to 1 V. The all-PVT-corner post-layout simulations demonstrate the worst output power is 4.2 mW, which is more than enough to drive a low-power wireless frontend, e.g. Bluetooth lower energy (BLE) Tx/Rx.**

Keywords—CMOS Process, Energy harvest, PVDF, Voltage multiplier, Boost converter, Schmitter trigger

I. Introduction

In the past decade, thanks to fast development of the microelectronics industry and semiconductor technology, many consumer electronic devices not only become smaller, but also more complex. It is more evident that this trend throws big impact upon evolution of Internet of Things (IoT), and wireless personal area networks (WPAN) applications. However, the development of advanced technologies should be encouraged to applied to resolutions of social problems in addition to entertainment usage. One of the major social issues is the missing children and demented elderly [1]. An early warning system can be equipped in the wearable clothes or shoes, consisting of self-powered wireless devices and reliable power sources, to reduce the number of missing kids and elderly. If the power supply is based batteries, it will make the users uncomfortable such that they might like to wear. Thus, powering the wireless devices by ambient energy harvesting becomes an attractive approach. Although the earliest energy harvesting dates back to the windmill and the waterwheel, recent nano-scale CMOS technology is proved to drive energy harvesting systems capable of capturing environment energy such as thermoelectricity, solar power, radio frequency (RF) power, and piezoelectric pressure. All of the mentioned materials have been proved to transform the captured energy into electricity in prior literatures.

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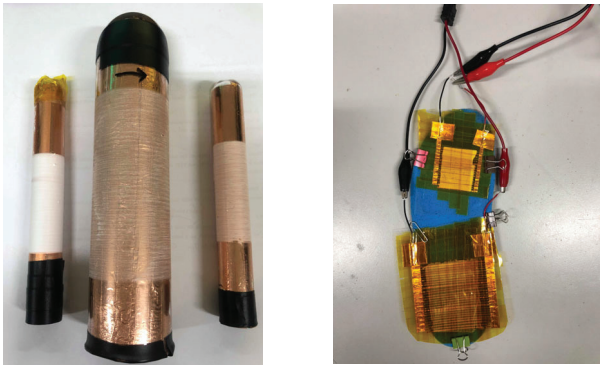
Omnipresent piezoelectric energy harvesting is considered as one of the eco-friendly energy sources. The material of piezoelectric used in this investigation is Polyvinylidene fluoride (PVDF), as shown in Fig.1(a). If distorted, the PVDF film generates power. Consequently, different magnitudes of distortion generate corresponding output power. A possible application is shown in shown in Fig.1 (b), where it is placed insole. Notably, it consists of two parts: one is placed at forefoot, and another placed at heel. Thus, the proposed PVDF film will be buried under shoe pad, while the proposed CMOS-based power harvester as well as the BLE Tx/Rx chips are embedded inside the heel. Thanks to the softness of PVDF film, users will not feel any uncomfortableness when they walk or run. It is much better than traditional piezoelectric materials.



(a) (b)

Fig. 1 (a) PVDF film; (b) insole prototype with PVDF film.

II. Implementation for PVDF Film Power Harvet

A. System Specification

Apparently, to achieve the wireless early warning function by PVDF-based system, the energy harvester must be able to provide reliable power supply to the following BLE Tx/Rx, which demands at least 1 V and 4.2 mW such that over 100 m wireless connection is ensured [2]. The proposed architecture as shown in Fig. 2, which device consists of an single chip including an AC/DC converter, a Volatge monitor, and a DC/DC converter, and another BLE IC (Tx/Rx IC).

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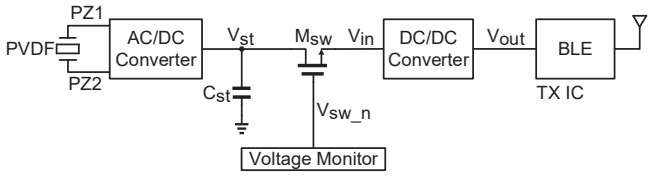

Fig. 2 Proposed PVDF energy harvester.

Notably, this investigation is meant to realize the first chip in Fig. 2. The AC/DC converter is based on the voltage multiplier, as shown in Fig. 3, which is widely used to pump a lower voltage to higher level in energy harvesting systems.

The DC/DC converter is a synchronous type using power MOSs instead of diodes to elevate the overall efficiency. Due to PVDF output power is very low, a water bucket fountain approach is employed, where the energy is kept in a capacitor until it is full [3]. The voltage monitor is a watch dog device to monitor the capacitor voltage to decide the on/off status of the power MOS.

B. AC/DC Converter

An AC/DC converter is almost required in any energy harvesting circuit, e.g., full wave rectifier, negative voltage converter (NVC), and voltage multiplier [4]. The voltage multiplier as the AC/DC converter is used in this work because of the efficiency and simplicity, as shown in Fig. 3, for real applications in wearable electronics. Another reason is that it generates a high voltage which relaxes the input voltage issue for the following DC/DC converter design. Meanwhile, since the input voltage amplitude PZ1 and PZ2 is very low, it need a low threshold voltage MOS in the voltage multiplier design. So used the advanced processed 40 nm CMOS which have lower enough to turn on the transistor. By the derivation of the recursive function of the voltage multiplier, the overall output voltage of V_{st} is expressed as in (1).

$$V_{st} = 4 \cdot N(V_{PZ} - V_{th}) \quad (1)$$

where N is the number of pumping stage, V_{PZ} is the AC signal amplitude of the PVDF film, and V_{th} is the threshold of native NMOS transistor.

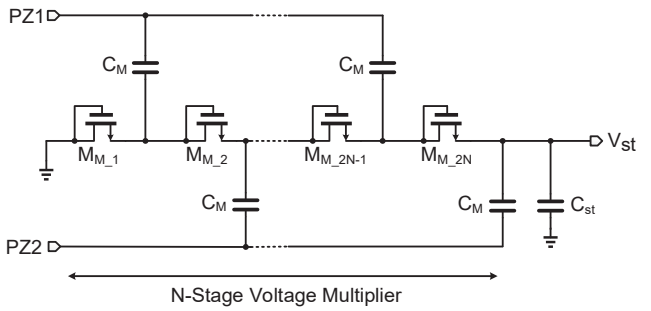

Fig. 3 Voltage Multiplier.

C. CMOS-based Voltage monitor

Typical output power of PVDF film is very low such that it needs to store the energy at the capacitor C_{st} until the stored energy is large enough to drive the next stage. A CMOS-based Schmitt trigger as in[5] is used to monitor the capacitor's voltage V_{st}. When V_{st} is higher than V_{SPH} (high switching voltage, about 0.26 mV) the MOS switch M_{sw} in Fig. 2 will be turned on. At the same time, an enable signal (V_{sw_n} = high) activates the DC/DC converter. When the Vst drops below V_{SPL} (low switching voltage, about 0.24 mV), the Schmitt trigger sends a disable signal (V_{sw_n} = low) to shut off DC/DC converter, and C_{st} is recharged at the same time.

D. DC/DC converter

The schematic of the DC/DC converter is shown in Fig. 4, which is a boost type [6]. A PMOS switch P_{sw} is utilized to replace a diode such that the big voltage drop can be avoided. A constant on-time/off-time (COOT) control comprises a digital control logic is shown in Fig. 5. T_{on}/T_{off} generators are shown in Fig. 6 and Fig. 7, respectively. At the presence of an enable signal (V_{sw_n} = high) from the voltage monitor, DC/DC converter starts to work.

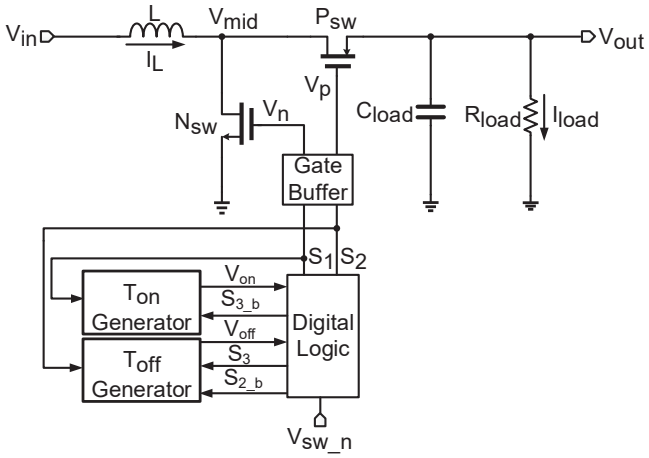

Fig. 4 Boost DC/DC converter

Digital logic in Fig. 4 is the critical control circuit in the boost converter. It is in charge of the timing sequence of all signals thus making the converter follow the pre-defined functionality. Namely, it is a FSM (finite state machine). There are a total of 3 modes, which are idle mode, on-time (T_{on}) mode, and off-time (T_{off}) mode.

- idle mode : When V_{sw_n} signal is low, the digital logic is reset. S1 = 0, S2 = 0, S3 = 1, V_{con} = 1 and V_{coff} = 0. The system waits for C_{st} charged to a voltage high enough to turn on the power MOS. Notably, S1 is the signal to move to the on-time mode. S2 is for the off-time mode. S1 and S2 are gate drives of N_{sw} and P_{sw}, respectively.
- on-time mode : When the voltage of C_{st} is high enough, V_{sw_n} generated by the Schmitt trigger is high. The DC/DC converter enters on-time mode (S1 = 1, S2 = 0, S3 = 0), where NMOS N_{sw} is turned on, and PMOS P_{sw} is off. The inductance current (I_L) flows through N_{sw} to store energy in the inductor (L). The duration of the on-time mode is controlled by the Ton generator. After a pre-defined time, Ton generator will send a signal from 1 to 0 to switch S1 which means to start the off-time mode.
- off-time mode : When V_{con} drops below V_{in}, the DC/DC converter enters the off-time mode (S1 = 0, S2 = 1, S3 = 0). NMOS N_{sw} is turned off, PMOS and P_{sw} is on. The inductance current (I_L) flows through P_{sw} to charge the load capacitor (C_{load}). The duration of the off-time mode is governed by the Toff generator.

T_{on} / T_{off} generators are responsible for timing controls of on-time and off-time modes, respectively. Based on the charging and discharging equations of a capacitor, any desired time duration can be attained by proper selections of C, V and I. T_{on} generator determines the "high" pulse width of V_n applied to the NMOS power switch N_{sw}, and the T_{off} generator is in charge of "low" pulse width of V_p driving the PMOS power switch P_{sw}. Current mirrors generating charge and discharge current are used for the mentioned demands.

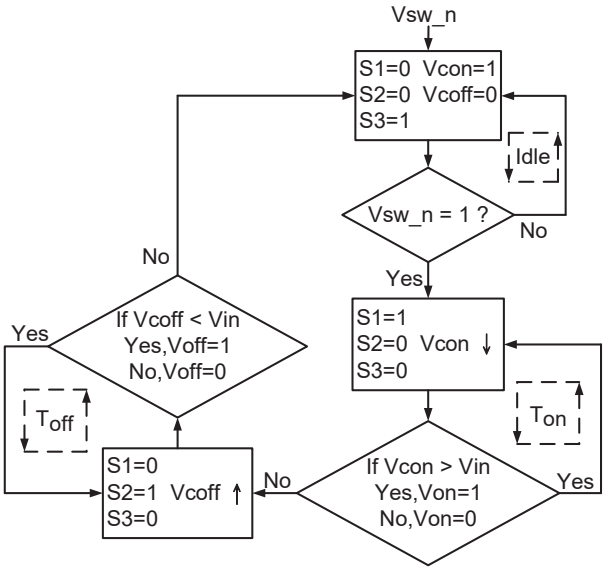

Fig. 5 Timing control

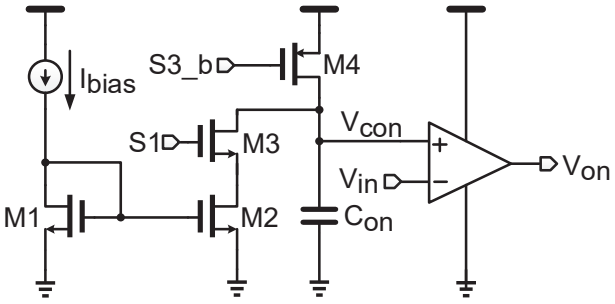

Fig. 6 Ton generator.

Referring to Fig. 6, in on-time mode (S1 = 1, S2 = 0, S3 = 0), M3 is on and M4 is off. The capacitor C_{on} is discharged by a constant I_{on} until V_{con} lower than V_{in}. In the off-time mode (S1 = 0, S2 = 1, S3 = 0), M3 and M4 are off such that the voltage of node V_{con} will be kept close to V_{in}. Referring Fig. 7, in on-time mode (S1 = 1, S2 = 0, S3 = 0), M7, M10 and M11 are off. By contrast, in off-time mode (S1 = 0, S2 = 1, S3 = 0), M11 is off, switch M7 and M10 are on. Thus, the capacitor C_{off} is charged by a constant I_{off} until V_{coff} higher than V_{in}.

E. Reference Current Generator

The reference current generator which provide an stable bias current (I_{bias}) in Fig. 8 is an indispensable for the DC/DC converter, not only for T_{on} generator, T_{off} generator and comparator. Because of the duty cycle of the power switch (N_{sw} and P_{sw}) which is depend on reference current generator. So the precise and stable reference current generator is play an important role. A lot of factor would affect the accuracy of I_{bias} such as supply voltage and temperature. By setting the proportional to temperature (PTAT) and complimentary to temperature (CTAT) in a proper ration to suppress the temperature effect the accuracy.

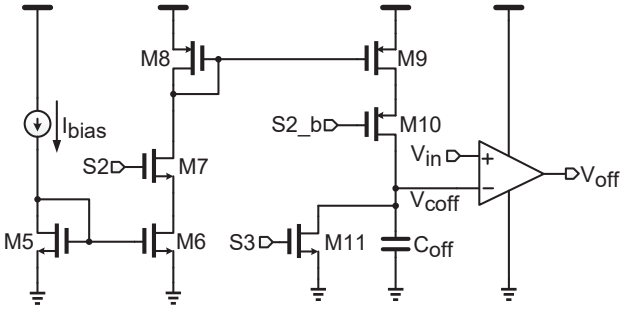

Fig. 7 Toff generator.

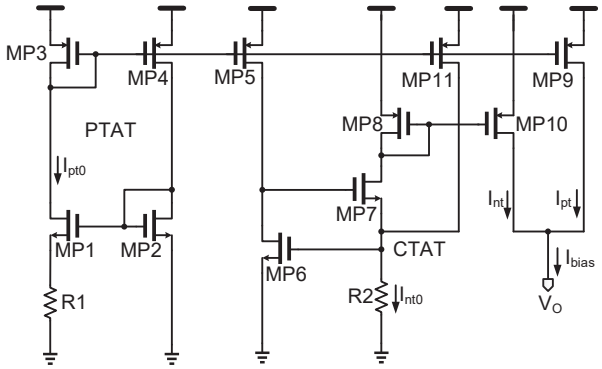

Fig. 8 Reference current generator.

In the PTAT which MP1 and MP2 work in the subthreshold saturation region, MP3 and MP4 work in strong inversion saturation region. For the current of subthreshold MOS is expressed as in (2).

$$I_D = I_0 \cdot exp(V_{GS} - V_T) \tag{2}$$

In this circuitry, MP1, MP2, MP3 and MP4 compose the PTAT current generator, and the generating PTAT current I_{pt0} is copied to the output by the current mirror composed of MP3 and MP9. In addition, MP5, MP6, MP7 and MP8 compose the CTAT current generator and the generating CTAT current I_{nt0} is copied to the output by the current mirror composed of MP8 and MP9. Then, the output current Ibias can be expressed as in (3), (4) and (5)

$$I_{pt0} = \frac{(V_{GS\_MP2} - V_{GS\_MP1})}{R_1} \tag{3}$$

$$I_{nt0} = \frac{V_{GS\_MP6}}{R_2} \tag{4}$$

$$I_{bias} = \frac{S_9}{S_3} \cdot I_{pt0} + \frac{S_{10}}{S_8} \cdot I_{nt0} \tag{5}$$

which V_{GS} is differential of gate and source. S3, S8, S9 and S10 are the aspect ratios of the transistor MP3, MP8, MP9 and MP10.

III. Simulation and Verification

The proposed PVDF-film energy harvest circuit is designed using Taiwan Semiconductor Manufacturing Company (TSMC) 40 nm CMOS process. The PVDF film is tested by LeCroy 610Zi to verify the output features, including voltage and current. The PVDF output voltage is roughly a sine wave with 120 mV amplitude. Hence, the simulations of

the proposed design is firstly based on 120 mV sine wave as the input signal. Fig. 9 shows the simulation waveforms of the boost DC/DC converter. Initially, V_{st} is low waiting for input AC signal to charge C_{st} to a voltage high enough for harvesting function. As V_{st} is higher than V_{SPH} (about 260 mV), an enable signal (V_{sw_n}) is asserted to move the boost converter from idle mode to the on-time mode.

When the boost converter is activated, the output voltage is 1 V and load current is 4.2 mA which is good to power the Bluetooth low-energy chip. The system will return to idle as the V_{st} is lower than V_{SPL} (about 260 mV) to recharge again. Fig. 10 shows the output voltage of the boost converter is very small (about 3 mV), which still can provide a stable power supply source for all MOS devices. Fig. 11 shows layout view of proposed PVDF energy harvester.

Table I tabulates the performance comparison between our design vs. several prior works. Apparently, our design attains the lowest input voltage and highest pump gain.

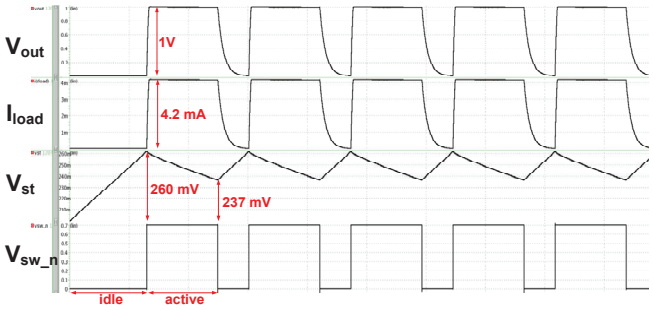

Fig. 9 Boost converter waveform.

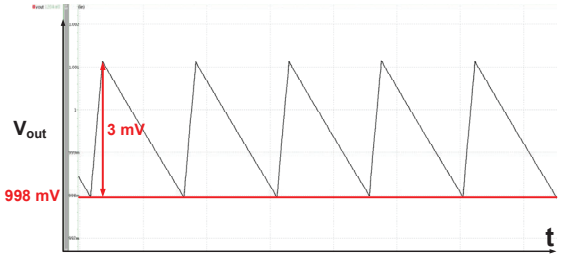

Fig. 10 Output voltage ripple.

TABLE I. PERFORMANCE COMPARISON WITH PRIOR WORKS

	[7]	[8]	[9]	[10]	ours
Year	2011	2014	2016	2017	2019
Material	Vibra.	PZT	Piezo.	Vibra.	PVDF
Tech.	0.5 um	0.18um	PSpice	0.5 um	40 nm
Vin	1 V	1 V	0.54 V	0.51 V	0.12 V
Vout	3 V	1.8 V	3.3 V	3 V	1 V
ripple	N/A	N/A	N/A	40 mV	3 mV
Pump gain	3	1.80	6.11	5.88	8.33

IV. CONCLUSIONS

In this work, a PVDF-film harvesting design is presented. The proposed architecture is designed and verified by TSMC 40-nm CMOS process. Due to the output voltage of PVDF film is very low. Obviously can not use the traditional diode as AC/DC converter which about 0.7 V, so need an advanced processed which have low V_{th} MOS. With the input amplitude generated by PVDF film is 120 mV, the simulation result of proposed architecture voltage to demonstrate that the harvested power is enough to drive a BLE RF frontend to achieve the early warning function for wearable electronics.

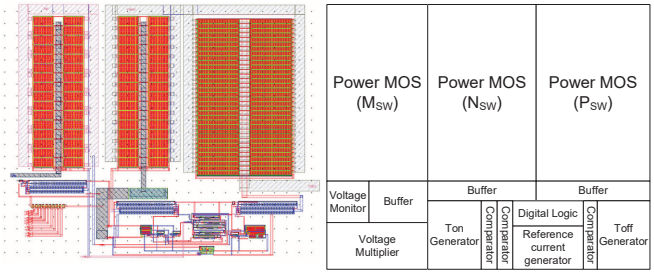

Fig. 11 Layout view of proposed circuit.

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