A 10-bit 50-MS/s SAR ADC with Split-Capacitor Array Using Unity-Gain Amplifiers Applied in FOG Systems

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***Abstract*—This paper presents a 10-bit 50-MHz SAR ADC with novel split-capacitor array design for FOG (fiber optic gyroscope) systems. Unlike the traditional SAR ADCs using bridge capacitors for the split capacitor array, this design uses the unity-gain buffer to replace the bridge capacitor. Thus, the linearity and the immunity to the process variation of the capacitor array could be improved. Besides, the settling time and the size of the capacitor array are both reduced. The proposed design is implemented with a typical 40 nm CMOS process. The DNL and INL are simulated to be 0.51 LSB and 0.56 LSB, respectively. The simulated SNDR is 51.23 dB with the 12.5 MHz input signal to show ENOB = 8.22 bits at the 50 MS/s sampling rate.**

Keywords—SAR, ADC, split-capacitor array, FOG

I. INTRODUCTION

Because of the features including low power consumption, medium sampling rate, and medium resolution, successive approximation register analog-to-digital converter (SAR ADC) is widely used in various low power systems [1], [2], [3], implantable biomedical systems [4], [5], and fiber optic gyroscope (FOG) system [6]. In an FOG system, when the gyro rotates, the phase shift of the optical signal is detected by the photo detector, and then converted to digital signal for further processing to attain the rotation degree. In the FOG system with 0.5^{o}/hr specifications, the required sampling rate and resolution are 50 MS/s and 10-bit, respectively, as shown in Fig. 1.

In recent SAR ADC designs, the input signal is coupled to the top plate of the capacitor array to reduce the effects of the mismatch and the noise from the comparator and the capacitor array [1], [2], [4], [7], [8]. The performance and the power consumption of the SAR ADC is then improved. The split capacitor array method is further employed to reduce the size and the driving power of the capacitor array [2], [9], as shown in Fig. 2. However, additional control circuits are required and extra power consumption are generated [9]. In a prior work [2], the bridge capacitor is not an integer multiple of the unity capacitor, which results in the complex control procedure and mismatching problem.

In order to avoid the complex control circuit and the problem of the bridge capacitor, this paper proposes a splitting capacitor array using the unity gain amplifiers for SAR ADCs. Because of the unity-gain buffers, the size and the settling time of the capacitor array could be reduced. Besides, the linearity loss of the capacitive DAC caused by the process variation of the bridge capacitor is avoided.

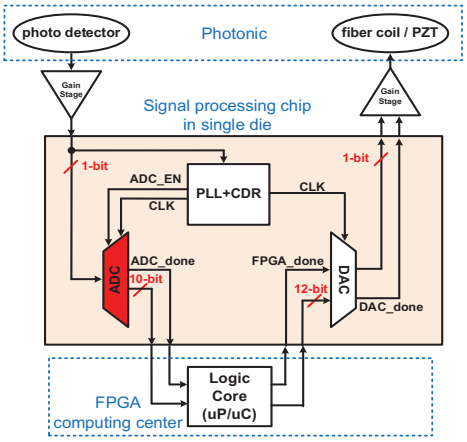

Fig. 1. Block diagram of the FOG system.

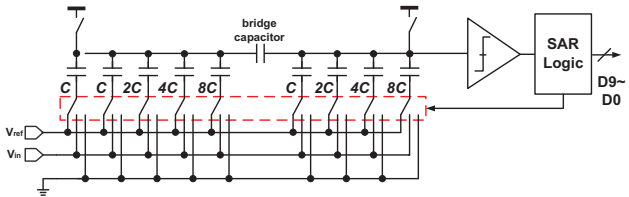

Fig. 2. SAR ADC with traditional split-capacitor array [9].

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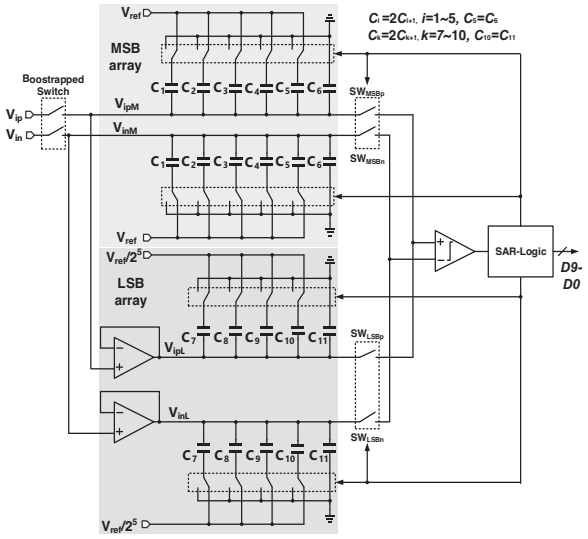

Fig. 3. The proposed SAR ADC with split-capacitor array using unity-gain buffers.

II. 10-BIT SAR ADC WITH SPLIT-CAPACITOR ARRAY USING UNITY-GAIN BUFFERS

Fig. 3 shows the block diagram of the proposed 10-bit 50-MS/s SAR ADC with split-capacitor array using unity-gain buffers, consisting of an MSB (Most Significant Bit) array, an LSB (Least Significant Bit) array, two Bootstrapped Switches, two unity-gain buffers, a comparator, a SAR-Logic circuit, and the switches, namely SW_{MSBp}, SW_{MSBn}, SW_{LSBp} and SW_{LSBn}. Because the unity-gain amplifiers are used, the size of the capacitor array is reduced from 2^N to $(2^{N-4}+2^{N-5})$ times of the unit capacitor for N-bit resolution. In this work, the size reduction of the capacitor array is 90.63% for 10- bit resolution. Notably, the unity-gain buffer is composed of a 2-stage OTA with the voltage gain of 48 dB and the gain bandwidth of 179.1 MHz at the corner of TT, 25ºC, 0.9 V.

The operation waveforms of the proposed design are illustrated in Fig. 4. When Clks is logic high, the bootstrapped switches are turned on to sample the differential input signals, V_{ip} and V_{in}, for both of the MSB and LSB arrays. The sampled signals in MSB array, V_{ipM} and V_{inM}, would enter the coarse conversion when Clks becomes logic low. During the coarse conversion, V_{ipM} and V_{inM} are compared by the comparator driven by Clkc at logic 1. For Clkc at logic 0, the MSB array are switched to the next configuration according to the comparison results and the SAR-Logic circuit. Simultaneously, V_{ipM} and V_{inM} are settled to the updated value and the bit, D9, is obtained. After 5 cycles of Clkc, the code of D5 is generated and then the switches, SW_{MSBp} and SW_{MSBn} are turned off. The signals, V_{ipM} and V_{inM}, are held at the MSB array. At the same time, the switches, S_{WLSBp} and SW_{LSBn}, are turned on such that the circuit enter the fine conversion. The sampled differential signals, V_{ipL} and V_{inL}, are directly coupled to the LSB array to process the compare and settling procedure driven by Clkc. After 5 cycles of Clkc, D0 is obtained. Then, Clks is pulled high and the MSB and LSB array would be reset for the next sampling cycle.

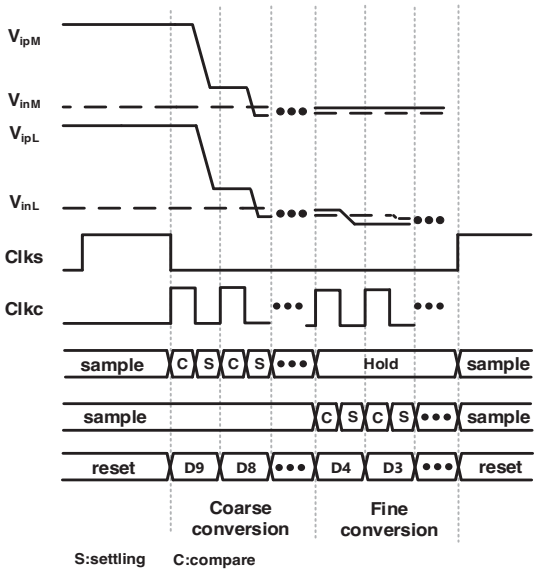

Fig. 4. Illustrative waveforms of the proposed SAR ADC with split-capacitor array using unity-gain buffers.

A. Bootstrapped Switch

Fig. 5 reveals the schematic of Bootstrapped Switch, which could improve the sampling linearity. M_{N1005} and M_{N1006} are the n-type switches, while M_{P1006} and M_{P1007} are the p-type switches. With the n-type and p-type switches are used simultaneously, the sampling range is increased and the clock feedthrough could be avoided [4]. $M_{N1001} \sim M_{N1004}$, $M_{N1007} \sim M_{N1009}$, and M_{P1010} are the bootstrapped circuit for the n-type switches. The other transistors are utilized for the p-type bootstrapped circuit, which is symmetric to the n-type bootstrapped circuit. When CLKs is at logic 0, the voltage of VDD is stored at the capacitor. When CLKs becomes logic 1, the gate voltages of M_{N1005} and M_{N1006} is charged to Vin+VDD, such that M_{N1005} and M_{N1006} are turned on without the distortion caused by the variation of the driving gate-source voltage from input signal. Thus, the linearity could be improved. The operation of the p-type bootstrapped circuit is similar. The gate voltages of M_{P1006} and M_{P1007} would be coupled to Vin-VDD when CLKs is at logic 1.

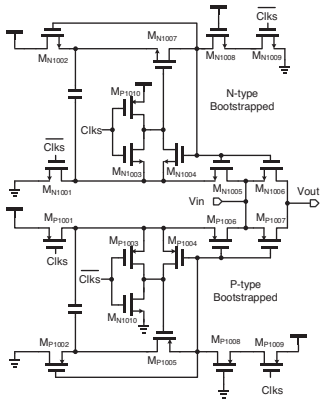

Fig. 5. Schematic of the bootstrapped switch [4].

B. SAR-Logic Circuit

Because of the usage of the unity-gain buffers, the control of the split-capacitor array becomes very easy. The schematic of the SAR-Logic circuit, is shown in Fig. 6. The series DFFs, DFF_S9 ~ DFF_S0, receive the input clk signal and generate the shift sampling signals, S9 ~ S0, for the MSB and LSB array, as shown in Fig. 7. The DFFs, DFF_d9 ~ DFF_d0, would store the output of the comparator, comp, for the codes, D9 ~ D0, respectively. After D0 is stored, eoc is pulled high to indicate the end of conversion for the specific point. And then the reset signal, rst, would be pulled down to reset the all DFFs for the next conversion.

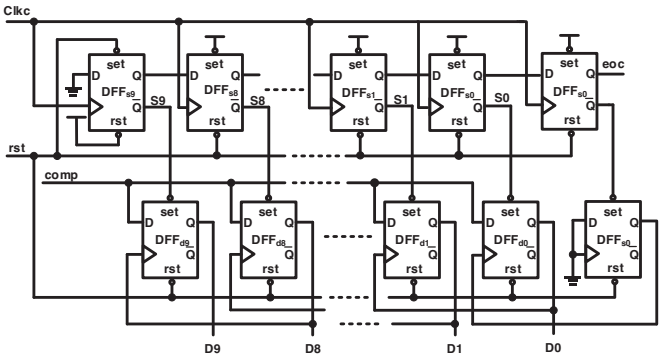

Fig. 6. Schematic of SAR logic circuit.

III. Implementation and Simulation Results

The proposed design is implemented using a typical 40 nm CMOS process. Fig. 8 shows the layout of the design, where the area is 536.2 × 531.88 μm^2, and the core area is 100 × 158 μm^2. To achieve the better matching and to reduce the unwanted effects caused by the process variation, the layout of the MSB and LSB array are drawn in a symmetric style, as shown in Fig. 9 (a) and (b), respectively. The symbol Cn denotes the nth capacitor. The symbol D refers to the dummy capacitor. The MOM (Metal-Oxide-Metal) capacitor with capacitance of 3 fF is used as the unit capacitor. The layout view of the unit capacitor is shown in Fig. 9 (c), where the area is 4.37 × 4.37 μm^2. Fig. 10 and Fig. 11 show that the worst case of the simulated DNL and INL are 0.51 LSB and 0.56 LSB, respectively. Referring to Fig. 12, the FFT spectrum with sampling rate of 25 MS/s is revealed. The simulated SNDR is 52.2 dB by given the 12.5 MHz input signal. For 50 MS/s sampling rate, the SNDR is 51.2 dB with 12.5 MHz input signal, as shown in Fig. 13. Table I summarizes the performance comparison with several prior works. The power consumption of the proposed design is 0.87 mW, which includes the power consumption of the output buffers for driving the capacitive loads of 60 pF. The power consumption of the SAR-Logic circuit, the comparator and the unity-gain buffers are 0.03 mW, 0.03 mW, and 0.29 mW, respectively. The power consumption could be further reduced, if the unity-gain buffer is turned on for the fine conversion only. By the comparison of FOM, the proposed design possesses the best performance in the required energy for each conversion step.

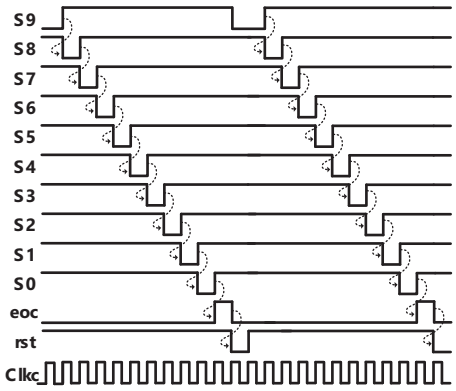

Fig. 7. Illustrative waveforms of the SAR logic circuit.

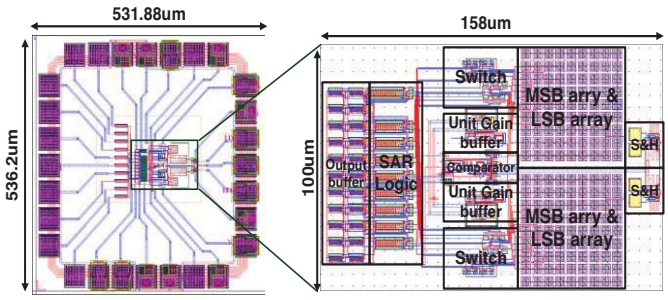

Fig. 8. Layout of the proposed design.

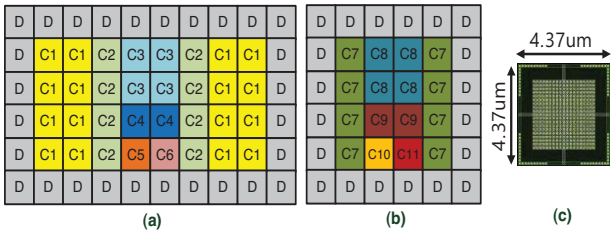

Fig. 9. Layout floorplan of (a) MSB; (b) LSB capacitor array; (c) the layout view of the unit capacitor.

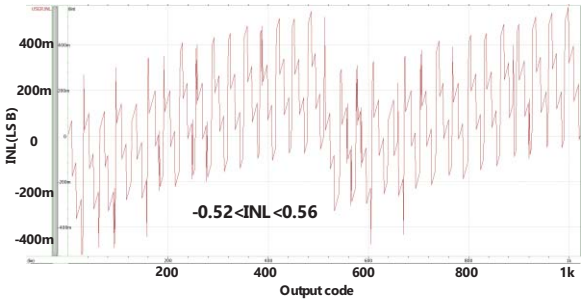

Fig. 10. Simulated DNL of the proposed design.

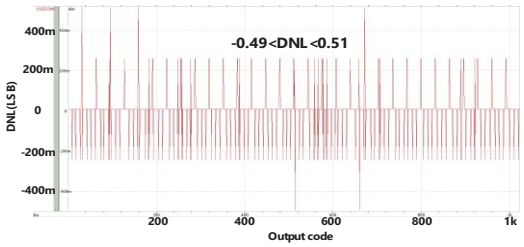

Fig. 11. Simulated INL of the proposed design.

IV. Conclusion

This paper proposes the 10-bit 50-MS/s SAR ADC using unity-gain buffers for applications in FOG systems. With the usage of the unity gain buffers, the linearity of the capacitor array is improved. Moreover, the effect caused by process drift of the bridge capacitor is avoided. Besides, the settling time and the size of the capacitor array are also reduced. Thus, the conversion energy of 58.36 fJ for each conversion step is achieved.

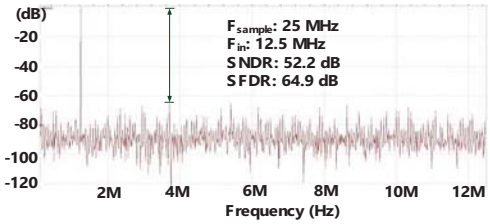

Fig. 12. Simulated FFT spectrum at 25 MS/s.

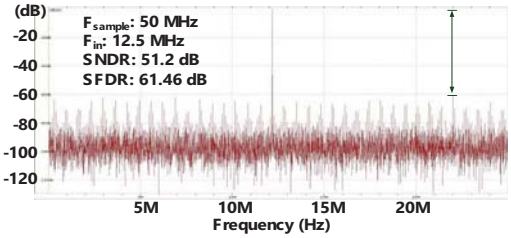

Fig. 13. Simulated FFT spectrum at 50 MS/s.

TABLE I. Comparison with Several Prior Works

	[10]	[7]	[11]	This work
Year	2015	2016	2020	2021
Publication	PRIME	ASSCC	EJ	ICET
Technology(nm)	90	45	180	40
Verification	Post-layout Sim.	Meas	Meas	Post-layout Sim.
VDD(V)	1.8	1.1	1.8	0.9
Resloution(bit)	10	10	12	10
Fs(MS/s)	150	800	50	50
SNDR(dB)	53	48	64.30	51.23
SFDR (dB)	60	56	-	61.46
ENOB (bit)	8.51	7.68	10.39	8.22
Power (mW)	15	9.8	4.73	0.87
Core area (mm^2)	-	0.15	0.17	0.015
FOM¶(fJ/step)	275	59.73	70.56	58.36

Note: ¶ FOM=$\frac{Power}{Fs*2^{ENOB}}$ (fJ/conv. step).

Acknowledgment

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