Analysis of Layout Arrangment for CMOS Oscillators to Reduce Overall Variation on Wafer

Pang-Yen Lou
Department of Electrical Engineering
National Sun Yat-Sen University,
Kaohsiung, Taiwan 80424
Email: lou0105cat@vlsi.ee.nsysu.edu.tw

Yung-Yuan Ho
Department of Electrical Engineering
National Sun Yat-Sen University,
Kaohsiung, Taiwan 80424
Email: kadora7riko@vlsi.ee.nsysu.edu.tw

Chua-Chin Wang†
Department of Electrical Engineering
National Sun Yat-Sen University,
Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

Abstract—This investigation demonstrates the analysis of various layout arrangements for oscillators (OSC) realized by CMOS technologies. More importantly, the analysis shows that the serpentine style of OSC stages (tiles) attains the minimum variation on wafer. Based on the analytic solution, various OSCs realized using 0.18 μm CMOS process, where the chip area of 1.458×0.908 mm^2, are simulated to justify the robustness of the proposed layout arrangement.

Keywords— oscillator, serpentine style, variation minimization, CMOS, on wafer

I. Introduction

Thanks to the advancement of CMOS semiconductor technologies, transistors as well as devices are downsized rapidly and constantly. The continuous shrinkage of nanometer processes, e.g., from 180 nm, 90 nm, ..., 16 nm, manufacturing variations on wafer become serious threat to the functionality of devices. The reason is no matter what process is used , it is suffered from various environmental factors, e.g., temperature, vibration, power surge, etc. OSC is one of the major components of digital circuits, which is usually the clock generator. This works manages to explore what kind of layout arrangement of OSCs with many identical delay stages will attains the best resistance to the variations caused by manufacturing on wafers.

II. Layout Anslysis of Oscillators

Fig. 1 shows a typical differential OSC, consisting of 16 delay stages, 2 16-to-1 MUXs, a Driving Buffer, and a Decoder to select a number of active stages such that the frequency is determined. Typical process variation on wafer are usually caused by the non-uniform doping concentrations of chemical substances. Thus, various layout styles will have difference resistance to these on-wafer variations. Assuming that the variation at the origin A(0,0), $P_A(0,0)$, has the fixed variation "c". We then assume the variation amount along the x axis for each beffer stage is "a", and that along the y axis is "b". In other words, the variation is assumed to be a linear function

† C.-C. Wang is the contact author. He is also with Institute of Undersea Technology (IUT) of NSYSU, Taiwan.)

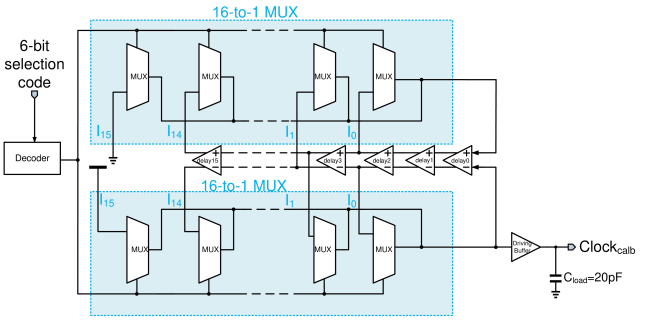

Fig. 1. An illustrative OSC with 16 delay stages.

against distance. For example, delay stage B(i,j) has the variation $P_B(i,j)$ as follows.

$$P_B(i,j) = a \times i + b \times j + c \quad (1)$$

- straight line layout : As shown in Fig. 2, the total variation $P_{total1}(i,j)$ is:

$$\sum_{i=1}^{16}\sum_{j=1}^{1} P_{total1}(i,j) = \sum_{i=1}^{16}\sum_{j=1}^{1}(a \cdot i + b \cdot j + c) = 136a + 16b + 16c \quad (2)$$

The average of the variation $P_{totalaverage1}(i,j)$ in this case is:

$$P_{totalaverage1}(i,j) = 8.5a + b + c \quad (3)$$

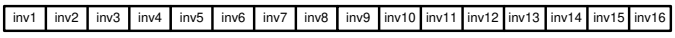

Fig. 2. Straight line layout style of OSC.

- serpentine layout : Referring to Fig. 3, the total variation $P_{total2}(i,j)$ in this case is:

$$\sum_{i=1}^{4}\sum_{j=1}^{4} P_{total2}(i,j) = \sum_{i=1}^{4}\sum_{j=1}^{4}(a \times i + b \times j + c) = 40a + 40b + 16c \quad (4)$$

Then, the average of the variation $P_{totalaverage2}(i,j)$ is:

$$P_{totalaverage2}(i,j) = 2.5a + 2.5b + c \quad (5)$$

inv1	Inv2	inv3	inv4
inv8	inv7	inv6	inv5
inv9	inv10	inv11	inv12
inv16	inv15	Inv14	inv13

Fig. 3. Serpentine layout style of OSC.

Based on Eqn. (2) and (4), we have the following observation.

$$\begin{aligned} & P_{total1}(i,j) \geq P_{total2}(i,j) \\ \Rightarrow & 136a + 16b + 16c \geq 40a + 40b + 16c \quad (6) \\ \Rightarrow & 4a \geq b \end{aligned}$$

Namely, the variation of the serpentine style is better than that of the straightline style as long as "a" is more than or equal to 1/4 of "b".

III. Simulation and Discussion

The proposed OSCs are realized on silicon using TSMC 0.18 um CMOS process, as shown in Fig. 4. Because of area limitation, the chip only comprises the serpentine style layout and straight line layout. The chip size is 1.458 × 0.908 mm^2, and the core area is 989 × 344 μm^2.

Fig. 5 shows the many more various buffer stage arrangements and their corresponding post-layout simulations of generated clock frequencies. The pre-layout simulation of the OSC is aimed at 490 MHz, which ignores the on-wafer variations. The post-layout simulation of the serpentine style layout (D in Fig. 5) shows the frequency nearest to that generated in the pre-layout simulation.

Table I tabulates the performance comparison of the proposed design and several recent patents regarding layout styles.

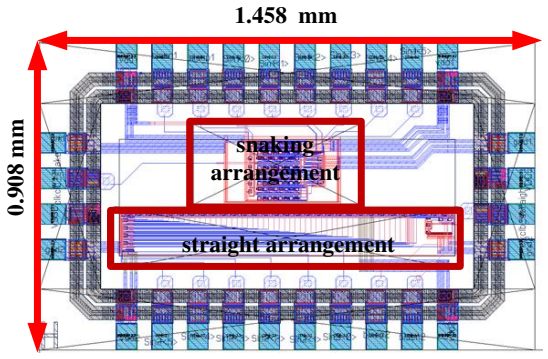

Fig. 4. Layout of various OSCs.

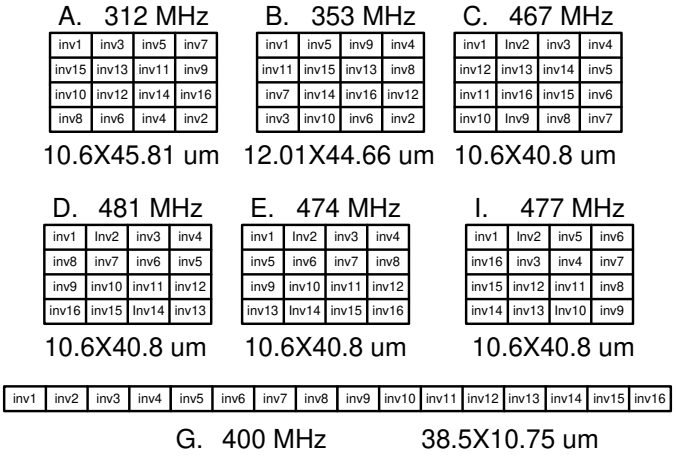

Fig. 5. Various arrangements and the clock rates of OSC by post-layout simulations.

TABLE I
Comparison with Prior Patents.

	[1]	[2]	[3]	this work
Year	2006	2012	2015	2021
Layout arrangement	straight	straight	serpentine	serpentine
Variation analysis	N/A	N/A	N/A	Yes

IV. Conclusion

This investigation presents an analytic and robust method to explore the best layout style for OSCs to resist the on-wafer variation. Moreover, the proposed serpentine layout style can be applied in other CMOS technology nodes to make the chip performance more predictable in the early design phase.

Acknowledgment

This work was partially supported by Ministry of Science and Technology (MOST), Taiwan, under grant MOST 109-2224-E-110-001- and MOST 109-2218-E-110-007-. Moreover, this work was also partially supported by the Ministry of Economic Affairs, Taiwan, under grant 107-EC-17-A-17-S3-050. The authors would like to express their deepest gratefulness to TSRI (Taiwan Semiconductor Research Institute), Taiwan, for their chip fabrication service.

References

[1] D. R. Dancer, "Digitally controlled ring oscillator," U.S.A. Patent US96112503, Jun., 2006.

[2] S. Wadhwa, D. Mehrotra, and P. M. Furth, "Low voltage, wide frequency range oscillator," U.S.A. Patent US8975974B2, Mar., 2012.

[3] C. L. Lin, "Quadrature output ring oscillator and method thereof," R.O.C. Patent TW 1547095 B, Aug., 2015.