A 4-Stage Negative Voltage Charge Pump with Randomly Selectable Parallel Switches

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***Abstract*—A charge pump generating negative voltages meant to be applied in drivers of smart window film (SWF) is proposed. More specifically, the proposed charge pump comprising 4 stages of negative charge pump and 4-phase clock generator, where the 4 stages are parallelly floorplanned to be randomly selectable by external digital signals, to generate required negative pulse train which are needed in the mode control of SWF. Post-layout simulations of the proposed design show that the a -2.85 to -15.9 V pulse train will be generated given VDD = 5 V and Vin = GND, where the switching frequency is 20 MHz, and the peak efficiency is 58%. The voltage of the output negative pulse train meets the required voltage mode range (-8 to -10 V) for SWF to demonstrate its multi-mode functions, namely transparency, tinted, or privacy modes.**

Keywords—negative voltage generation, charge pump, smart window film, HV CMOS, 4-phase clocking, randomly selectable

I. Introduction

Electrochromic window has been widely used in many so-called Green Building demonstrating various modes depending on the necessity or sunlight. For instance, when the sunlight is strong, the window can be powered to provide shield to resist sunlight to keep the indoor temperature relatively low. Most of this type of window is coated with a thin film, where liquid crystal is sandwiched in the middle of layers [1]. Apparently, liquid crystal will be polarized if appropriate voltages are applied. This film is also known as smart window film (SWF), which demands digital driving signals with ± 8 to ± 10 V swings. A negative voltage is needed to prevent the SWF from image sticking effect caused by the residue voltage .

Although many negative voltage generators have been reported, most of these works were not meant to be integrated with solar cells which have limited and unstable output voltage, e.g., [2], [3]. DC-DC converters are one of the possible solutions to generate negative voltages. No matter boost type, buck type, or buck-boost type, they all need an external negative reference voltage to carry out the required function [4], [5]. By contrast, charge pumps (CP) based on capacitors are considered a better way to be integrated with solar cells so that a compact solution is feasible for SMF applications [6], [7], [8], [9], [10], [11]. However, most of the prior CPs are suffered from poor efficiency, low voltage swing, or low driving current, which are not fully applicable to SWF applications. The critical part is the generation of -8 to -10 V voltages which are needed to erase the residue voltage of the previous state of SWF. Thus, a 4-stage CP-based negative voltage generator is proposed featured with parallel switches. More importantly, the proposed design is realized by High Voltage (HV) CMOS technology where Deep P-well and N+ Buried Layer are available to carry out perfect isolation between ground and negative voltage layers such that the negative voltage will be reliably generated.

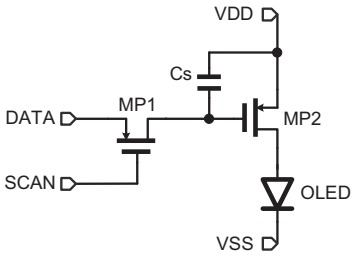

Fig. 1. Simplified driver circuit of an OLED

II. Negative Voltage Generator with Stage Selectable Mechanism

Referring to Fig. 1, a simplified driver for OLED is shown, where VDD is meant to turn on the device. If the previous state of the OLED device is opposite to the current state, the residue charge on Cs will become a problem to enter the next state, since it takes time to discharge the residue charge therewith. The best strategy is to apply negative voltage to neutralize the residue charge on Cs. This is the reason why and how the negative voltage generator is needed.

A. System Design of Negative Voltage Generator

The proposed negative voltage generator system is illustrated in Fig. 2, including 4 CPi (i=1, 2, 3, 4) stages, a VCO (voltage-controlled oscillator), and a Comp (comparator). Each CPi stage is composed of NLSi (negative level shifter), parallel HV N-device MNi, NCPS (negative charge pump stage), 4-phase CGi (clock generator), and an AND gate. The functions of these sub-circuits are described in the following subsections.

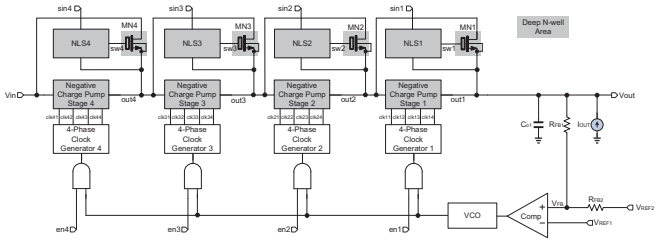

Fig. 2. System architecture of the proposed design

• The 4-phase CGi is in charge of generating 4 non-overlapping clocks.
• The output capacitor, Co1, is tuned to eliminate the ripples.
• VCO and R_{FB1}, R_{RB2} consist of a PFM (phase frequency modulation) feedback control to stabilize the entire system.
• HV n-device, MNi, in each CPi stage is the bypass path when this CPi stage is not selected such that the voltage generated in the previous CP(i-1) stage is coupled to the next stage, CP(i+1). Besides, the bypass path attributed to MNi facilitates the 4 stages in the proposed CP can be enabled at will, e.g., 1, 3, 4, 2, not necessarily restricted to 1, 2, 3, 4.
• NLSi in each CP stage generates corresponding gate drives so that the bulk voltage in that stage is biased correctly to fully turn on and off the HV n-device.

B. Requirements of HV N-device

The bulk bias of all the devices on the output path shall be kept in negative so as to provide a negative output voltage. Thus, all the devices in each CP stage and the corresponding parallel device must be N-type. What even more important is that these N-devices must be able to prevent the PN junction from conductance so that they are equipped with an isolation ring composed of deep P-well and N+ buried layer, as shown in Fig. 3.

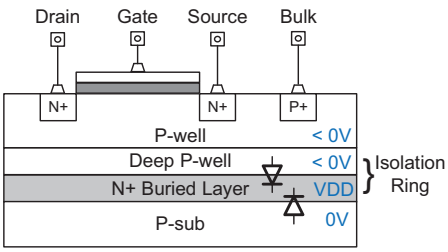

Fig. 3. Sideview of HV N-device

C. Negative Charge Pump

The negative charge pump circuit in each CP stage is given in Fig. 4, where all the devices are HV devices. The operation is illustrated by Fig. 5. Notably, clk1, clk2, clk1aux, clk2aux are non-overlapping clocks generated by the 4-phase CG in the same CP stage. A total of 5 states in the first half period are addressed as follows.

• T1 : IN is grounded. Node np1 and na1 is dropped to -VDD. Node np2 is 0, na2 becomes VDD-VTH.
• T2 : clk2 is now high to drive node na1 to -VTH.
• T3 : All clock signals are low such that this is a steady state.
• T4 : clk1 is pulled high to drive node np1 low such that node na1 is pulled up to -VTH.
• T5 : clk1aux is now pulled high so that node na1 becomes VDD-VTH.

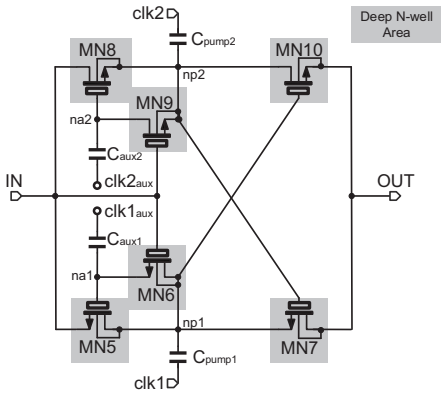

Fig. 4. Schematic of negative charge pump

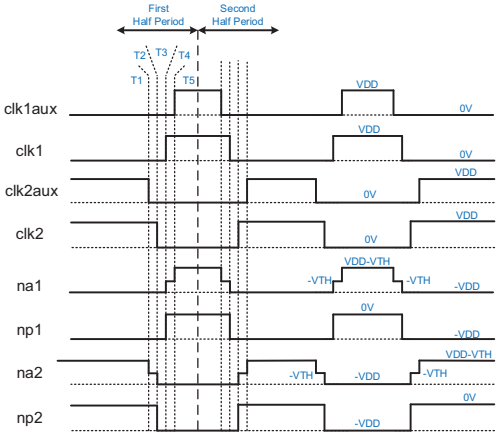

Fig. 5. Timing of negative charge pump

Notably, the operation of the second half period in Fig. 5 is totally opposite to that of the first half period. In short, the voltage at np1 is passed to OUT and IN is passed to node np2 in the first half period. By the above operation, a -VDD output voltage will be generated by a single CP stage.

D. Negative Level Shifter

The negative level shift, NLSi, of each CP stage is shown in Fig. 6. Notably, bulks of HV N-devices, MN 11 and MN12, are biased in negative voltage range as those in NCPi. By contrast, P-devices, NP3 and MP4, needs to be HV PMOS

with high tolerance of VDS drop. Then, when Bypass_ctrl = VDD, MP3 and MN12 are off, MP4 and MN11 are on, to result in Bypass_sw = VDD. It is vice versa if Bypass_ctrl = GND. In this way, the input range [0, VDD] is shifted to [-VDD, VDD].

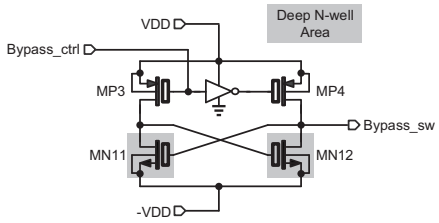

Fig. 6. Timing of negative level shifter

E. 7-stage VCO

The requirement of a SWF driver is not a high-speed clock for fast system operations. By contrast, it needs a low power clock generator if the SWF system relies on a battery system. Thus, we take advantage of the current starved ring VCO as shown in Fig. 7, where a total of 7 delay stages are used. The frequency selection is determined by VIN. When VIN = VDD, the maximal frequency of this design is fixed at 20 MHz.

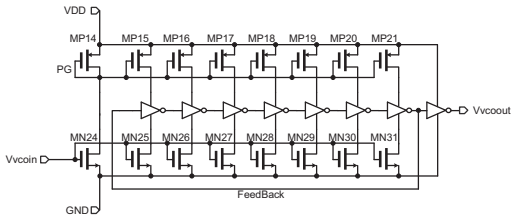

Fig. 7. 7-stage VCO

F. Power Analysis

The efficiency is the primary concern for any power circuit design. The switching loss is defined as Eqn. (1),

$$P_{SW} = V_{DS} \times I_D \times f_{sw} \times \frac{Q_{GS} + Q_{GD}}{I_G} \quad (1)$$

where P_{SW} is the switching loss, V_{DS} is the drain-source voltage, I_D is the drain current, f_{sw} is the switching frequency, I_G is the gate current, Q_{GS} and Q_{GD} are gate-source and gate-drain charges, respectively. Three major low power features are demonstrated in the proposed design.

1). Since the parallel bypass power N-device is utilized in each CP stage, V_{DS} on these path is reduced such that the switching loss is reduced as well.
2). No need to sequentially turn on because all CP stages are parallelly driven. The settling time for a specific output voltage is reduced.
3). Low-frequency 4-phase clock generators result in lower switching loss.

III. Simulation and Verification

The proposed 4-stage CP-based negative voltage generator is realized using 0.18 um HV BCD CMOS process. Fig. 8 shows the overall layout, where the area is 3321×1569 um^2. The output load is assumed as 60 pF = pad (20 pF) + wire bond (20 pF) + probe (20 pF), which is the worst case. To demonstrate the expected performance, Fig. 9 and 10 show the typical case given the output current = 0.5 mA and 5.5 mA, respectively. Notably, the 4 stages of the proposed charge pump are activated in the order of 1, 3, 2, 4, and then disabled in a different order as 4, 2, 3, 1, at the corner of (TT, VDD, 25^{o}C). Fig. 11 is the worst case at (SS, 90% VDD, 0^{o}C) and the output current loading = 5.5 mA, where the order of enable and disable is the traditional sequence. By all means, the above simulation results are adequately to prove that the proposed CP is allowed the random selection of stages. Besides, The proposed design is able to generate -10.5 V at the worst case with the largest load, which meets to the demand required by SWF applications.

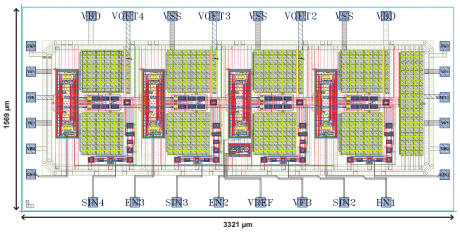

Fig. 8. Layout of the proposed negative voltage generator

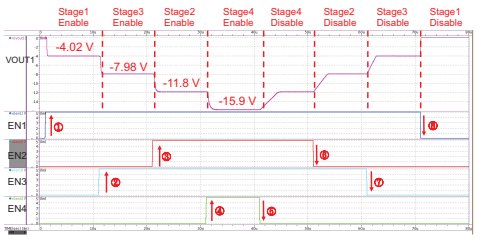

Fig. 9. Simulation at the typical corner (TT, VDD, 25^{o}C) with load current = 0.5 mA

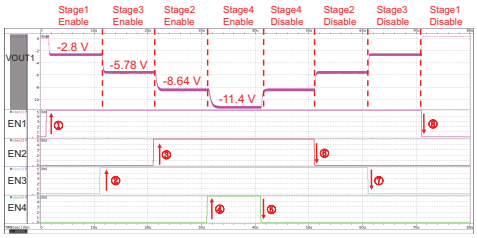

Fig. 10. Simulation at the typical corner (TT, VDD, 25^{o}C) with load current = 5.5 mA

TABLE I.
PERFORMANCE COMPARISON OF NEGATIVE VOLTAGE GENERATORS

	[6] *ICECS 2016*	[7] *BioCAS 2018*	[8] *VLSID 2020*	[9] *TCAS-I 2020*	This work
Process (nm)	130	180	180 BCD	250 BCD	180 BCD
Verification	simulation	simulation	simulation	measurement	post-layout sim.
VDD (V)	1.2	3/1.8	1.8	3.0	5.0
Max. Vout (V)	-9.4	-8.954	+24.0	-9.3	-15.9
Max. Iout (mA)	-0.05	-5.5	+0.1	-5.5	-5.5
flying cap. (pF)	1	100	N/A	100	72.9
switching (MHz)	50	N/A	20	100	20
#activated stages	8× (fixed)	3× (fixed)	15× (fixed)	4× (variable)	4× (variable)
peak eff. (%)	67.43	55.28	49	52	58.08
FOM	26.41	909.1	65.33	886.6	1015.82

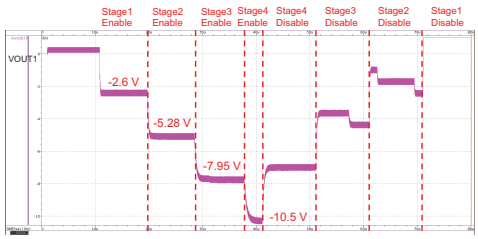

Fig. 11. Simulation at the worst corner (SS, 90% VDD, 0°C) with load current = 5.5 mA

Fig. 12 is the efficiency vs. different stages, when the output current is 5.5 mA. The best efficiency is 58.08% at -12.6 V output. A simple performance comparison is tabulated in Table I, where FOM is defined as Eqn. (2). By the comparison summarized in Table I, the proposed negative voltage generator attains the best FOM.

$$\text{FOM} = \frac{\text{peak efficiency} \times \text{max. Iout} \times \text{max. Vout}}{\text{VDD}} \quad (2)$$

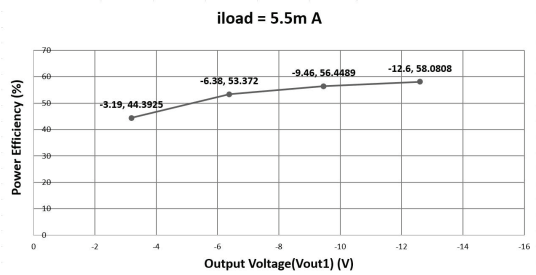

Fig. 12. Power efficiency when Iout = 5.5 mA

IV. CONCLUSION

Referring to Table I, the proposed negative voltage charge pump attains the best FOM by far. The proposed design not only generate a wide range of voltage swing from -2.85 to -15.9 V, but also a current range from 0.5 to 5.5 mA. It is featured with independently selectable bypass switches so that any order of stage election is allowed. This results in the reduction of switching loss and a peak efficiency of 58%. Besides attaining the best FOM compared with the state of art, what even more important is that the proposed design meets SWF driver demand no matter what PVT corner is. This feature will lead to the realization of SWF on portable devices, e.g., biker's helmet, and car's windshield.

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