A High Resolution And Wide Range Temperature Detector Using 180-nm CMOS Process

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***Abstract*—This paper presents a highly linear and high resolution temperature detector implemented using a typical TSMC 180-nm CMOS process. It is composed of PTAT & CTAT current generator circuits and a current-to-frequency converter. The PTAT current generator is based on a bandgap reference circuit connected to a cascode current mirror, while the CTAT generator is a current mirror driven by a voltage-to-current circuit. Post-layout simulation shows a detection range of –40°∼ 100°C and a 0.5°C resolution. The maximum linearity error is simulated to be 0.406% for the PTAT/CTAT ratio. The power consumption of the design is 15.4 mW at the maximum output frequency = 4.07 MHz, and the area of 0.682 mm ^{2}.**

***Index Terms*—temperature detection, high linearity, PTAT, CTAT, current-to-frequency conversion**

I. Introduction

Temperature detection and security control have become very crucial in industrial, commercial appliances, and equipment applications, etc. The reason is because excessive heat may result in increased power consumption, unstable system performance, and even equipment damage. Temperature monitoring systems, including temperature sensors as a critical component, are required to prevent these hazards [1].

CMOS temperature sensors have recently seen increased demand owing to their compact size, and low power consumption. It can also be integrated in existing chips for temperature monitoring. These temperature sensors provide voltage, current, resistance, or frequency outputs that are proportional or complementary to the temperature being measured [1]–[5]. They are frequently incorporated into on-chip systems with signal conditioning circuitry.

There are various advantages to use CMOS temperature sensors, including efficiency and reliability of temperature monitoring systems. Integration of signal filtering circuitry simplifies system design and lowers overall costs. As a result, CMOS temperature sensors are quickly becoming a popular alternative for temperature monitoring and control applications across a wide range of sectors.

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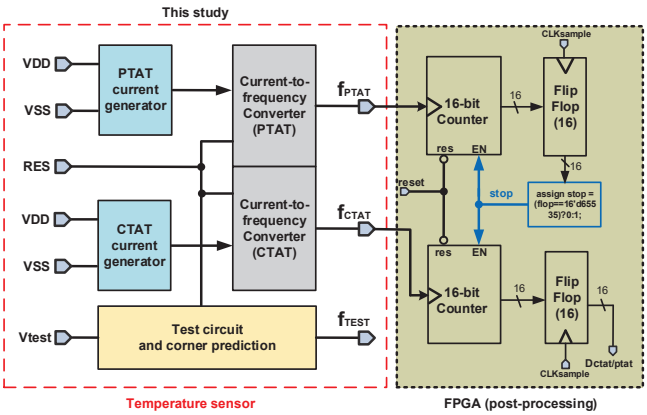


Fig. 1. Temperature detector architecture

This investigation is presented as follows: Section II discusses the overall circuit design. It also includes the theoretical derivations of the proposed circuit. Section III presents the post-layout simulation results as well as the implementation of the proposed circuit. Finally, the paper is concluded in Section IV.

II. Temperature Sensor Design

Fig. 1 shows the architecture of the proposed temperature sensor with an external FPGA post-processing unit. The temperature sensor is composed of three main circuits: 1. PTAT current generator; 2. CTAT current generator; 3. current-to-frequency converter; and a Test circuit. The sensor mainly converts temperature of the circuit into a frequency. The output signal can then be processed using the external FPGA.

The option to have two separate outputs, PTAT and CTAT, is to improve the resolution of the detector. By this way, we can compare the PTAT and CTAT behavior to further see the effects of temperature variation of the circuit during post-processing. Previous studies normally had their outputs to be proportional to the temperature. This results in poor linearity due to channel length modulation and leakage threat [2], [3], [6].

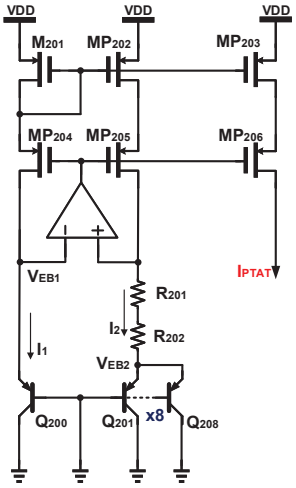


Fig. 2. PTAT current generator circuit

A. PTAT Current Generator

The PTAT current generator is based on a bandgap reference circuit to make use of the fact that bipolar devices have current that is exponentially varying with the input voltage. Through this feature, we can use the current difference to have an output that is proportional to the temperature. The PTAT current generator is shown in Fig. 2. Eqns. (1) & (2) show the derived current equations. Another design choice we made is to use calibrated NWELL (R_{201}) and polysilicon (R_{202}) resistors to reduce 1st and 2nd order temperature variations [3].

Eqns. (1) and (2) show the derivation of the PTAT current of the circuit of Fig. 2. The output current shows a proportional variation with temperature. The total resistance as mentioned previously is calibrated to reduce temperature variations.

$$\begin{aligned} V_{EB1} &= V_T \ln\left(\frac{I_1}{I_S}\right) \\ V_{EB2} &= V_T \ln\left(\frac{I_2}{I_S}\right) \end{aligned} \tag{1}$$

$$I_{PTAT} = \frac{V_{EB1} - V_{EB2}}{R_{201} + R_{202}} = \frac{V_T \cdot \ln(8)}{R_{total}} = \frac{k \cdot T \cdot \ln(8)}{q \cdot R_{total}} \tag{2}$$

where V_{EB1} is the voltage drop over Q_{200}, V_{EB2} is the voltage drop over Q_{201} to Q_{208}, V_T is the thermal voltage, k is the Boltzmann's constant, q is the charge of an electron, and R_{total} is the total resistance of the NWELL (R_{201}) & polysilicon (R_{202}) resistors.

B. CTAT Current Generator

Referring to Fig. 3, the CTAT current generator is designed based on the mirrored current of a low dropout (LDO) regulator. The design takes advantage of the temperature coefficient of R_{301} to have a CTAT behavior. Eqn. (3) shows the CTAT current equation, which is a mirrored current at R_{301} with the regulated voltage equal to V_{EC}, where V_{EC} is

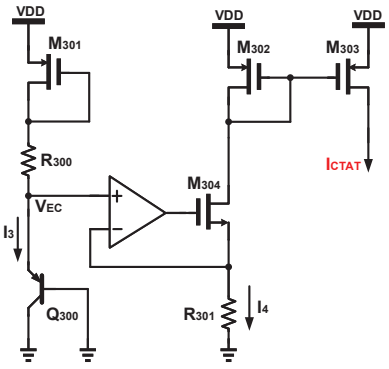


Fig. 3. CTAT current generator circuit

the voltage drop of Q_{300}. The current variation with respect to the temperature is shown in Eqn. (4) and is further derived using chain rule of differentiation in Eqn. (5). To make sure that the output current attains a CTAT behavior, we suggested that the the first term of Eqn. (5) is always greater than the second term.

$$I_{CTAT} = I_4 = \frac{V_{301}}{R_{301}} = \frac{V_{EC}}{R_{301}} \tag{3}$$

$$\frac{\partial I_{CTAT}}{\partial T} = \frac{\partial}{\partial T}\left(\frac{V_{EC}}{R_{301}}\right) \tag{4}$$

$$\frac{\partial I_{CTAT}}{\partial T} = -\frac{V_{EC}}{R_{301}^2} \cdot \frac{\partial R_{301}}{\partial T} + \frac{1}{R_{301}} \cdot \frac{\partial V_{EC}}{\partial T} \tag{5}$$

C. Current-to-Frequency Converter

Fig. 4 shows the circuit diagram of the current to frequency converter used in the design. It is made up of a 5-stage differential ring oscillator with a start-up circuit. To have a good balance of linearity and high resolution, we have used a cross-coupled differential pair with symmetrical load, as highlighted in Fig. 4. The derived frequency of the oscillation is shown in Eqn. (6).

$$f_{osc} = \frac{1}{2\pi C_L}\sqrt{g_{mMN0}^2 - (g_{mMP8}^2 - g_{mMP6}^2)^2} \tag{6}$$

D. Test Circuit

Test circuit in Fig. 1 is an independent current to frequency converter with the same architecture to Fig. 4 included on the same chip. It accepts a voltage input Vtest during the test mode. This redundancy is used to predict the corner in which the chip falls into. Fig. 5 shows the test mode output of the circuit at Vtest equal to 2.06 V. There are significant differences in frequency output of the test circuit so that it can be used for further corner prediction.

III. Simulation and Implementation

The temperature detector is implemented using a typical TSMC 180-nm CMOS process. Fig. 6 show the layout of the proposed temperature sensor. It has a total area of 0.683 mm^2 with a core area of 0.196 mm^2.

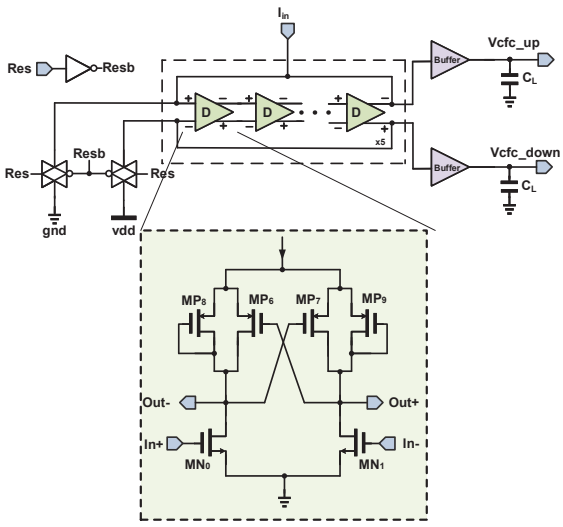
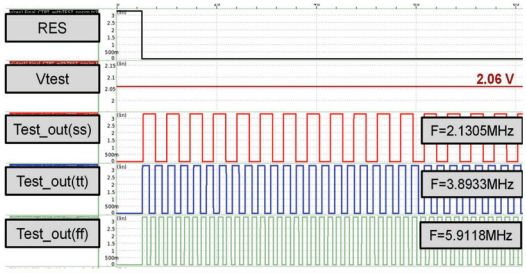


Fig. 4. Current-to-frequency converter



@Vtest=2.06	SS	TT	FF
Test_out (Mhz)	2.1305	3.8933	5.9118

Fig. 5. Test mode post-simulation result

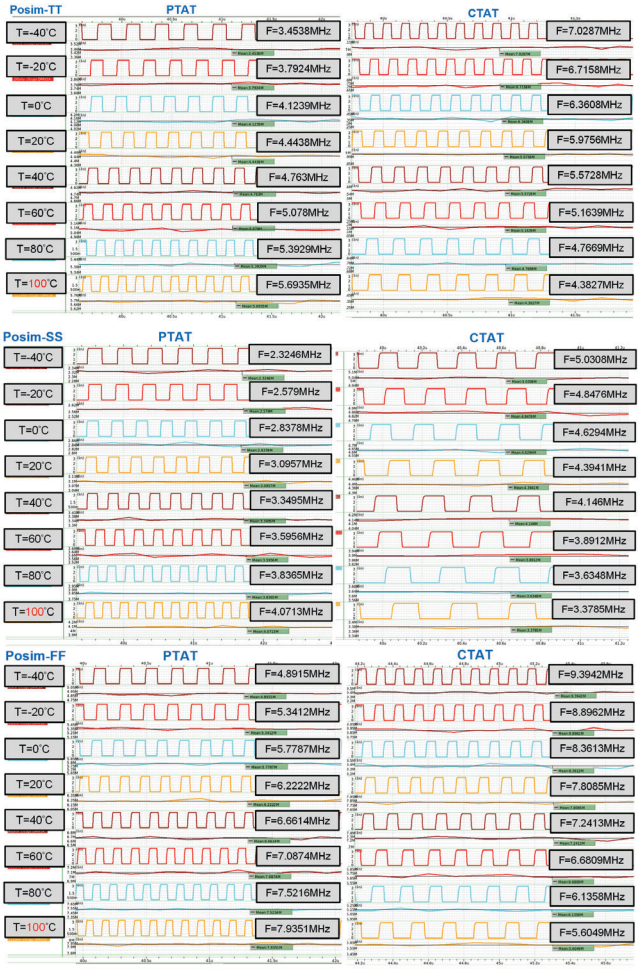


Fig. 7. Temperature (PTAT and CTAT) detector simulation results at TT, SS, and FF corners

Referring to Fig. 7, the post-layout simulation results of the PTAT and CTAT current generator outputs of the proposed design are shown. It can be observed that it gives out a PTAT and CTAT behaviour as expected. Fig. 8 shows the temperature vs. frequency output at the worst corner. It can be observed that the the PTAT output have a maximum error of 0.466% at the 37° C mark and 0.871% at 15° C mark for the CTAT output. To have additional insight from the circuit, we compared the currents of the PTAT and the CTAT generators. Fig. 9 shows that the ratio has a proportional relation to the temperature. It has a linear characteristic with a maximum linearity error of 0.406%.

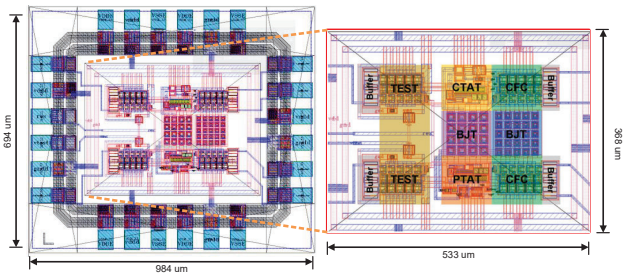


Fig. 6. Layout of the temperature detector

Table I summarizes the performance comparison of different temperature sensors in previous years. It can be seen form the table that our design achieved the best resolution in terms of the temperature, since it can detect 0.5° C. It also offers the best linearity compared to previous designs. A 0.384° C maximum detector error and a 0.466% linearity error is observed from the simulations. An FOM using the temperature range divided by the temperature error detection is used to compare the different designs. Referring to technology roadmap in Fig. 10 of different temperature sensors, it can be inferred that our design is the best so far.

IV. Conclusion

A highly linear temperature sensor implemented in TSMC 180-nm CMOS process is presented on this paper. It has a chip size of 694×984 μm^2 with a core of 368×533 μm^2. It has a wide detection range of –40° C ∼ 100° C and a

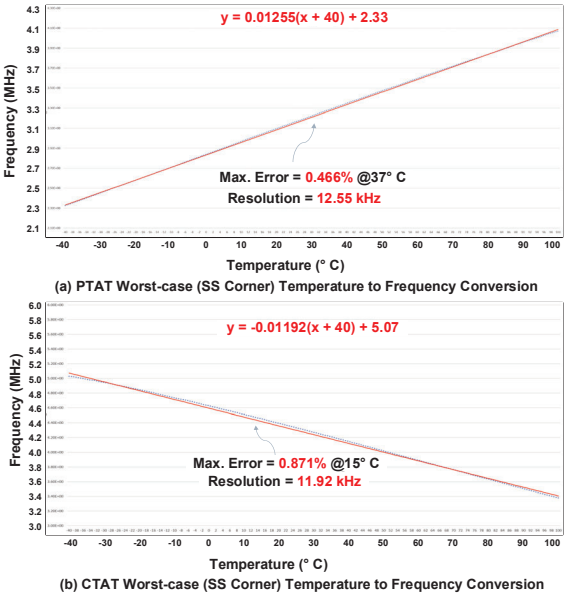


Fig. 8. Temperature vs. frequency simulation, (a) PTAT worst-case (SS); (b) CTAT worst-case (SS)

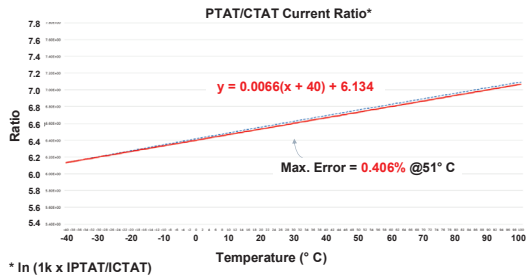


Fig. 9. PTAT/CTAT current ratio vs. frequency. $f = \ln(1000 \times \frac{I_{PTAT}}{I_{CTAT}})$

resolution of 0.5° C. Our design achieved a high linearity with a maximum linearity error based on the post-layout simulations. An FOM based on the temperature range and temperature error showed that our design performed the best to date.

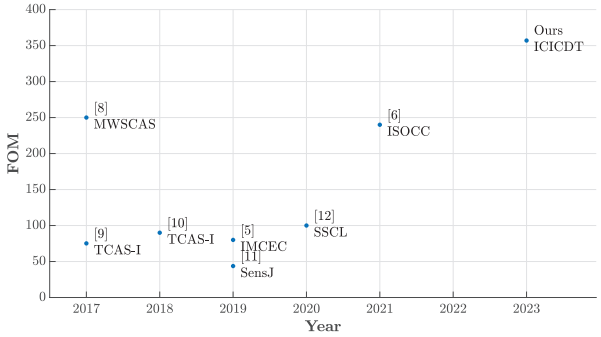


Fig. 10. Technology roadmap of temperature sensors

TABLE I
COMPARISON TABLE WITH PREVIOUS WORKS

	[7]	[8]	[4]	[9]	[5]	Ours
Year	2017	2018	2019	2020	2021	2023
Process (nm)	180	50-HV	65	65	180	180
VDD (V)	0.6	5.0	0.8	0.9	3.3	3.3
Area (mm^2)	0.45	2.39	N/A	0.32	1.64	0.682
Power (W)	75n	11m	0.9u	6.4n	48.5m	15.4m
f_{out} (kHz)	28.5–29.3	500–2200	60–85	N/A	403–465	2320–4070
Range (°C)	0–100	-5–40	0–80	-30–70	-40–80	-40–100
Res. (°C)	1	1	1	N/A	3	**0.5**
Error (°C)	1.33	1.04	-1	-1	0.5	**0.384**
Lin. Err. (%)	5.5	1.42	N/A	1.7	0.392	**0.466**
FOM	75.18	43.69	80	100	240	**367.1**

FOM = Temp. Range/ Temp. Error

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