A Wide Range 2-to-2048 Division Ratio Frequency Divider Using 40-nm CMOS Process

Soumika Majumder, Venkata Naveen Kolakaluri, Oliver Lexter July A. Jose, and Chua-Chin Wang
Dept. of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

2024 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-3099-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISCAS58744.2024.10558236

***Abstract*—This work presents a high-resolution programmable frequency divider to select the frequencies that will be generated in DCO (Digitally Controlled Oscillator) or VCO (Voltage Controlled Oscillator) that will benefit the design of high-speed, wide-range PLL for Internet-of-Things (IoT) applications. The design is verified through post-layout simulations at 1 GHz input clock. The design achieves a division ratio range of 2-2048 with minimum and maximum operating frequencies of 488 KHz and 500 MHz, respectively. This work is carried out using 40-nm CMOS technology at 60 pF capacitive load and an average power consumption in worst case post layout simulation is 0.470 mW at 500 MHz.**

***Index Terms*—Frequency divider, high-resolution, dynamic sampling, programmable, duty cycle**

I. Introduction

The necessity for wide range operating frequency in low voltage, small area, and relatively low power components that combine performance with the ability to be produced inexpensively in large quantities are now the key challenges for developing high speed wireless communication systems. The key component of the transceiver in RF system is the phase-locked loop to supply a stable clock, and in many cases the PLL must be programmable [1]. Accordingly, the advantage of programmable frequency divider is to select different input frequencies to get a wide range of output frequencies. It plays a vital role in the designs of the phase-locked loops (PLL) and in all digital phase-locked loop (ADPLL) as shown in Fig. 1(a). Its primary requirement is to divide a frequency with wide division ratio, low power, and high resolution. The most basic programmable frequency divider, which achieves maximum modulus range and minimal power dissipation but has a low operating frequency, is a programmable counter. However, the ripple counter only offers one constant modulus while enabling fast speed performance. Most prior high-frequency divider designs rely on a computational technique that might be inaccurate due to PVT variations and limited frequency tuning range, which limits its usability [2].

An adaptive multi-modulus frequency divider designed on 40-nm CMOS process claimed a two-stage high operational frequency divider with low power dissipation [3]. The design works in high power saving mode, but with a limited range of division ratio, i.e., 1-49.

A 0.6 Programmable frequency divider designed with standard gates and a Johnson counter with configurable length was reported [4]. This design consumes excessive power using 180-um technology. However, the major drawback of the mentioned design is the extremely low maximum clock frequency. This divider allows division range from 2 to 11.

This paper illustrates a wide range programmable frequency divider with higher resolution, lower power consumption using 40-nm CMOS technology. A wide division ratio of 2-2048, which is benefited for a high speed and wide range PLL [5], has been achieved with the help of 10-bit master slave synchronous counter and a clock count comparator block. This design is configurable based on the requirement and is scalable to different frequencies. The proposed architecture works for 33-50% input clock duty cycle, but the output frequency is tuned to always 50% duty cycle. The design features input DFF array with an adaptive refresh rate which reduces glitches that improves overall loop stability in ADPLLs or PLLs.

II. Proposed Programmable Frequency Divider

Fig. 1 (b) shows the block diagram of the proposed high-resolution frequency divider, which can be integrated in a PLL circuit, shown in Fig. 1 (a), for high-speed data transmission applications. The Input DFF array samples input data $D_{[0:9]}$, and the sampling rate is determined by the output frequency. When the clock count is equal to $D_{in[0:9]}$ decimal equivalent, the Clock counter resets the counting, and the input data is updated. The Input DFF array and Clock counter are coupled to the Clock count comparator and generate the unadjusted divided frequency (on time $\neq$ off time) based on $D_{in[0:9]}$. A Duty corrector is utilized to correct the duty cycle of the output frequency f_{out} (aiming at 50 %). Finally, the F/2 bypass selector provides an f_{out} = f_{clk}/2 without passing through the Duty corrector, extending the f_{out}'s range.

The output frequency (f_{out}) can be calculated based on the following cases:

Case 1: Division ratio, $DR \neq 0$

$$f_{out} = \frac{V_s}{2} \tag{1}$$

Case 2: $DR = 0$

$$f_{out} = V_s \tag{2}$$

Prof. Chua-Chin Wang is the corresponding author. He is also with Ins. of Undersea Technology, National Sun Yat-Sen University, Taiwan and an adjunct professor at Vel Tech, Chennai, India

Oliver Lexter July A. Jose is also connected with Dept. of Electronics Engineering, Batangas State University, The National Engineering University, Philippines.

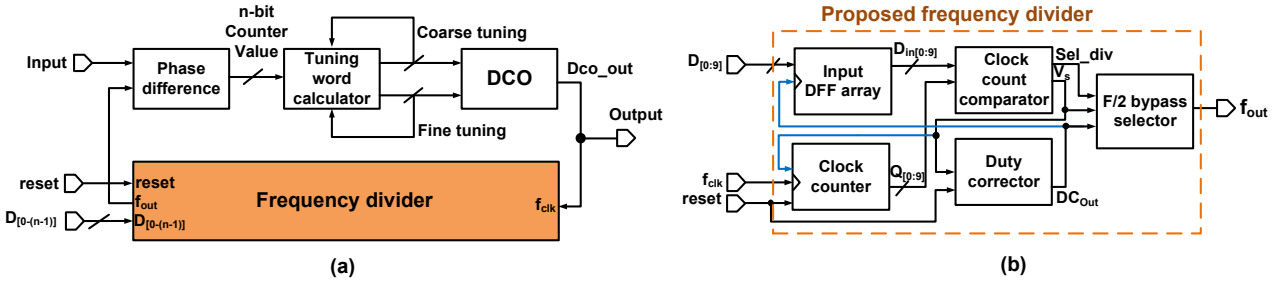

Fig. 1. (a) Basic PLL architecture; (b) Proposed programmable frequency divider block diagram

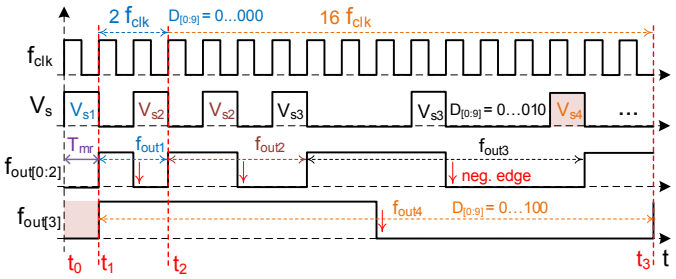

Fig. 2. Timing diagram of the proposed frequency divider

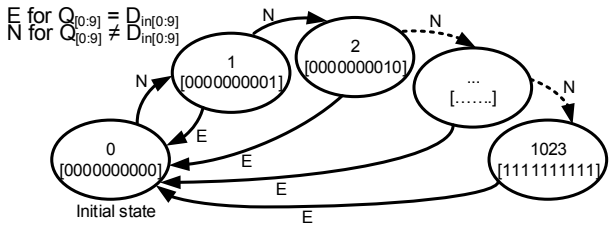

Fig. 3. State diagram of clock counter

where DR and V_s are given by Eqn (3) and (4), respectively.

$$DR = \sum_{N=0}^{N-1} D_N \cdot 2^N + 1 \tag{3}$$

$$V_s = \frac{f_{clk}}{DR} \tag{4}$$

The timing diagram for the proposed frequency divider is illustrated in Fig. 2. When $D_{in[0:9]}$ = 0000000000, it generates V_s as the reference for the output frequency. V_s is generated when the synchronous counter output $Q_{[0:9]} = D_{in[0:9]}$. In this state, the output frequency is half as the f_{clk}. The f_{out} signal is shifted by T_{mr} (equal to one clock cycle) for the safe read and write margin of the DFF in the Duty corrector. For instance, when $D_{in[0:9]}$ = 0000000010, V_{s3} is generated, having an output frequency of $f_{out[3]}$. Furthermore, it is also shown in the timing diagram that the input $D_{in[0:9]}$ is updated at the negative edge of f_{out}.

A. Input DFF array and Clock counter

The DFF array reads the input data $D_{[0:9]}$ periodically at the negative edge of the f_{out} signal. The DFF array synchronizes the N-bit input data and eliminates false triggering.

Fig. 3 shows the Clock counter state diagram that converts a number of clock pulses (depending on resolution) into binary equivalent. The Clock counter is based on master-slave DFF topology, which minimizes the effect of RAC (race around condition). A soft reset is employed through a multiplexer circuit at the input of master-slave DFF to ensure a synchronized transition to the default state ($D_{in[0:9]}$ = 0000000000). When $D_{in[0:9]} \neq Q_{[0:9]}$, the Clock counter updates to the next state

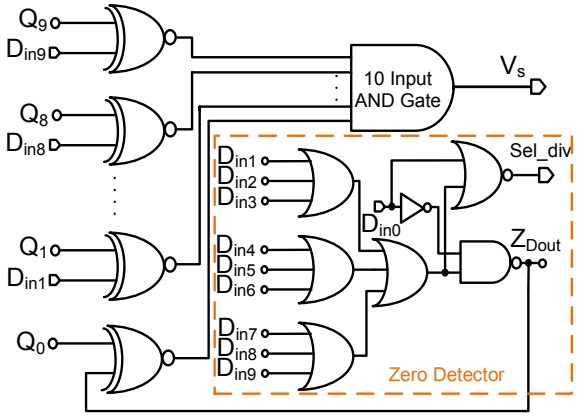

Fig. 4. Clock count comparator

sequentially until $D_{in[0:9]} = Q_{[0:9]}$. Once if $D_{in[0:9]} = Q_{[0:9]}$, the Clock counter will be reset to the default state, which marks the end point of f_{out}.

B. Clock count comparator

The Clock count comparator shown in Fig. 4 generates the output frequency (with no duty correction) by comparing the input clock cycle count to the $D_{[0:9]}$. When the Clock counter outputs $Q_{[0:9]} = D_{out[0:9]}$, the Clock count comparator resets the Clock counter to its initial state $Q_{[0:9]}$ = 0000000000. For $D_{[0:9]}$ = 0000000000, the clock counter enters the zero state, resulting in f_{out} = 0, whereas the f_{out} must be equal to f_{clk}. To avoid the stuck at zero state, the zero detector circuit within the Clock count comparator complements the overrides the LSB comparison input when $D_{in[1:9]}$ = 000000000. The zero

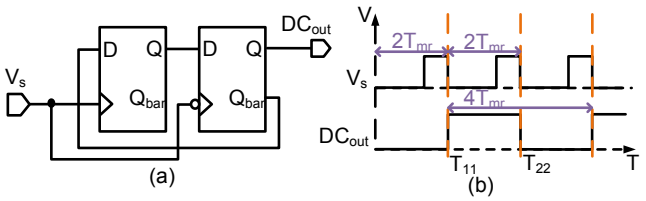

Fig. 5. Duty corrector (a) circuit and (b) timing diagram

TABLE I
OUTPUT FREQUENCY COMPARISON BETWEEN IDEAL AND SIMULATION

Binary Input	ideal f_{out} (MHz)	post-sim f_{out} (MHz)
0000000000	500.00	500.00
0000000001	250.00	250.00
0000000011	125.00	125.00
0000000111	62.50	62.50
0000001111	31.25	31.30
0000011111	15.63	15.60
0000111111	7.81	7.81
0001111111	3.91	3.91
0011111111	1.95	1.95
0111111111	0.98	0.98
1111111111	0.49	0.49

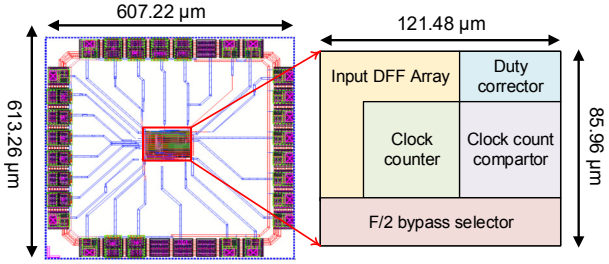

Fig. 6. Proposed frequency divider layout

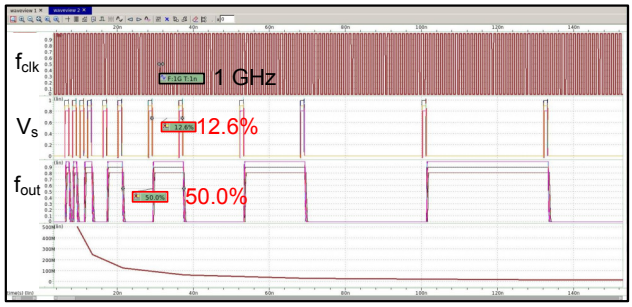

Fig. 7. Proposed frequency divider all-PVT corners post-layout simulation using Johnson counter

detector in the Clock count comparator generates the Sel_div signal, which controls the F/2 bypass selector.

C. Duty corrector

Fig. 5 (a) shows the duty corrector that ensures the f_{out} duty cycle is approximately 50%. The pulse width of the V_s signal generated by the clock count comparator is always one clock signal wide for all possible f_{out}. Since the %duty cycle for any signal is proportional to its pulse width, the duty cycle of V_s (V_{s4}) gets narrower as the f_{out} (f_{clk}/8) decreases, as shown in Fig. 2. In spite of the change in the ratio of V_s signal on and off time as shown if Fig. 5 (b), the duty corrector output (DC_{out}) maintains equal on and off time, based on the negative edge of V_s signal.

D. F/2 bypass selector

The duty corrector keeps the DC_{out} duty cycle at 50 %, which reduces V_s by half, as shown in Fig. 5 (b). When the division ratio = 2, the V_s duty cycle = 50 % without passing through to the duty corrector. When the division ratio = 2, the expected f_{out} = f_{clk}/2 with a duty ratio equal to 50%. As a result, there is no need for the V_s signal to pass through the duty corrector. The F/2 bypass selector in the form of a multiplexer bypassed the duty corrector when the division ratio = 2, which increases the frequency range and satisfies Eqn. (2).

III. SIMULATION AND IMPLEMENTATION

Fig. 6 shows the proposed frequency divider architecture layout implemented using a 40-nm CMOS process. The schematic and layout of the proposed chip have been developed in the Cadence schematic editor and layout editor, respectively. The pre-layout and post-layout simulations have been visualised with the help of the Synopsis WaveView Tool. The design has an overall chip area of 613.26 x 607.22 μm^2 and the core area is 85.96 x 121.48 μm^2.

Fig. 7 represents the all-PVT-corner post-layout simulation of the proposed frequency divider evaluated at five process corners (FF, FS, TT, SF, and SS), V_{supply} = 0.81, 0.9, and 0.99 VDD, and temperatures = 75, 25, and 0°C. The clock frequency and load capacitance used during the simulation are 1 GHz and 60 pF, respectively. The duty cycle of V_s at $D_{[0:9]}$=000000111 is 12.6 %. The V_s will go to the Duty corrector, adjusting the duty cycle to 50 % as illustrated in Fig. 7. In addition, an exponential decay relationship between f_{out} and $D_{[0:9]}$ pattern from Table I shows the accuracy of the design.

Table I shows the f_{out} comparisons between the ideal result (using Eqn. (1) to (4)) and post-layout simulation result (shown in Fig. 8). The proposed frequency divider has a low deviation of less than 0.2 %, showing design robustness. The frequency divider attains the lowest f_{out} = 488 kHz, verifying the design's high division ratio (equal to 2048).

The eye diagram post-layout simulation (worst corner) for the proposed frequency divider at the lowest division ratio and the highest power consumption (fout = 500 MHz) is illustrated in Fig. 9. The eye diagram has a width (w_{EYE}) and height (h_{EYE}) of 0.97 ns and 0.904 V, respectively. The w_{EYE} and h_{EYE} exhibit minimal deviation from expected values ($w_{EYE\_expected}$ = 1 ns and $h_{EYE\_expected}$ = 0.900 V), which indicates little signal degradation and validates the robustness

TABLE II
PRIOR PFD PERFORMANCE COMPARISON

	[2]	[6]	[7]	[3]	[1]	[8]	[4]	this work
Year	2006	2010	2011	2013	2018	2020	2020	2023
Publication	TCAS2	EDSSC	TCAS2	ASICON	ICSE	IWS	ICECS	
Technology (nm)	90	350	90	40	180	40	180	40
Verification	Meas.	Meas.	Meas.	Post-sim.	Meas.	Meas.	Post-sim.	Post-sim.
V_{DD} (V)	1.2	3.0	1.0	0.9	1.8	1	0.6	0.9
Clock frequency (GHz)	4.7	4.5	5.5	4	3	9.3	0.025	1
Div. ratio	64-127	256-511	1-256	1-49	1200-1240	2-4	2-11	**2-2048**
Power (mW)	2.4	21.3	1.0	0.156	3.51	5.07	0.0037	0.470 @500MHz
Min. duty cycle	-	-	-	-	-	-	33 to 50%	50%
FOM	3.89	0.422	1408	1256.4	0.883	3.6686	37.162	**2178.72**

$$*FOM = \frac{\frac{Max.ratio}{Min.ratio}}{Power \times \frac{1}{ClockFrequency}}$$

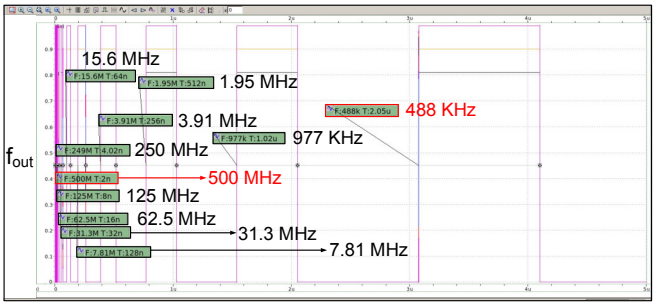

Fig. 8. f_{out} for all possible inputs in Table I

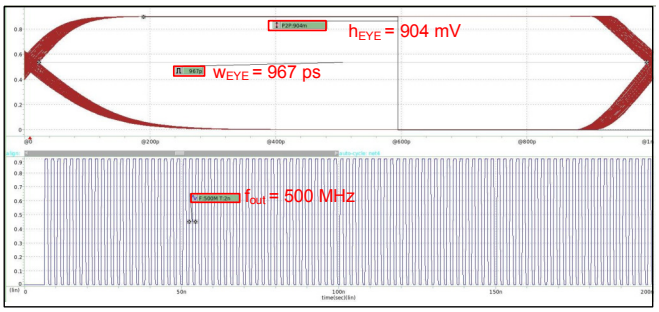

Fig. 9. Proposed frequency divider eye diagram post-layout simulation

of the design.

The performance comparison between prior works is tabulated in Table II. Our frequency divider achieved the highest division ratio range of 2-2048, which can be used to improve loop stability in PLL applications. The results in Table I verify that the proposed design is scalable, which can be implemented in higher resolution for a wide range of frequencies and high accuracy. Most prior works only rely on theoretical analysis, which is easily affected by PVT variations. Finally, the proposed frequency divider has the highest FOM of 2178.72, which makes our design superior to all prior works.

IV. CONCLUSION

This study demonstrates a wide division ratio frequency divider is implemented using TSMC 40-nm CMOS process. The design is a 10-bit resolution with a 2-2048 division ratio. The DFF array synchronizes the input data of the frequency divider and eliminates false triggering. The Clock counter of the proposed design minimizes the effect of RAC and synchronizes its transition. The functionality of the design is confirmed through all-PVT-corner post-layout simulations with an input clock frequency of 1 GHz at a load capacitance of 60 pF. A 0.2 % deviation between ideal and post-layout simulation output frequency demonstrates the design robustness. Finally, the accuracy of the design is verified by the exponential decay relationship between f_{out} and the Johnson counter input pattern.

ACKNOWLEDGMENT

Thanks to NSTC (National Science and Technology Council), Taiwan, for granting partial funding under NSTC 111-2623-E-110-002-, 112-2221-E-110-063-MY3, and NSTC 110-2623-E-110 -001-.

REFERENCES

[1] A. A. Ahmad, S. H. Md Ali, N. Kamal, S. R. Abdul Rahman, and M. Othman, "Design of phase frequency detector (PFD), charge pump (CP) and programmable frequency divider for PLL in 0.18μm cmos technology," in *Proc. 2018 IEEE International Conference on Semiconductor Electronics (ICSE)*, Aug. 2018, pp. 242–245.

[2] M. Ali and E. Hegazi, "A multigigahertz multimodulus frequency divider in 90-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 12, pp. 1333–1337, Dec. 2006.

[3] H. Yuan, Z. Ma, and Y. Guo, "An adaptive multi-modulus frequency divider," in *Proc. 2013 IEEE 10th International Conference on ASIC*, Oct. 2013, pp. 1–4.

[4] R. A. Robles and T. Harada, "A 0.6v programmable frequency divider and digitally controlled oscillator for use in a digital PLL in the subthreshold region," in *Proc. 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Nov. 2020, pp. 1–4.

[5] Analog Devices, *Phase-Locked Loop (PLL) Fundamentals*, July 2018. [Online]. Available: https://www.analog.com/media/en/analog-dialogue/volume-52/number-3/phase-locked-loop-pll-fundamentals.pdf

[6] W. Li, H. Chen, and L. Shi, "A 4.5-GHz 256–511 multi-modulus frequency divider based on phase switching technique for frequency synthesizers," in *Proc. 2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, Dec. 2010, pp. 1–4.

[7] C.-S. Lin, T.-H. Chien, and C.-L. Wey, "A 5.5-GHz 1-mW full-modulus-range programmable frequency divider in 90-nm CMOS process," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 9, pp. 550–554, Sep. 2011.

[8] M. ZhU, T. Ding, X. Liao, S. Ye, D. Jiang, and D. Zhao, "A low-noise VCO and a low-power frequency divider in 40-nm CMOS," in *2020 IEEE MTT-S International Wireless Symposium IWS*, Sep. 2020, pp. 1–3.