A 10-MHz 5-V On-chip 6-layer Multi-level Digital Transformer Using T18HVG2 Process

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***Abstract*—Most digital transformer designs used non-overlapping coil topology, which increases the design area on silicon. This study demonstrates a digital transformer based on a multi-layer, over-lapping coil topology that increases the transformer's mutual inductance. Two interwound coils composed of 6 metal layers are implemented to realize the transformer and fabricated using 18 μm HV CMOS process. To demonstrate the operation of the proposed transformer, the rise time (t_{rise}), fall time (t_{fall}), and propagation delay (t_{pro_delay}) of six chips are measured at an operating frequency of 10 MHz with a worst power consumption of 52 mW. The digital transformer is also tested at various duty cycles to ensure its suitability for power conversion applications.**

***Index Terms*—Digital transformer, high-frequency, coreless, CMTI, HV CMOS, metal layers**

I. Introduction

Nowadays, the reliability of power MOSFETs gained significant importance, since it has been used in many applications, such as automotive, aviation, military, etc. [1]. Power MOSFET can operate at a higher switching frequency. However, the high switching frequency may lead to large dv/dt switching transients, which may jeopardize the control circuit. Hence, an isolation circuit between the driver and control circuit is required to eliminate the effect of dv/dt switching transients [2].

The CMTI (common mode transient immunity) is a parameter that determines the effectiveness of the isolation circuit in a driver [3]. A high CMTI indicates that the isolation circuit provides adequate galvanic isolation against dv/dt switching transients [4]. In general, the isolation can be realized through capacitive, optical, or magnetic coupling approaches. A digital transformer can be used as an isolation circuit, which transfers data and minimizes the dv/dt variation.

Capacitive isolation uses parallel plate capacitance in transmitting a signal from the primary to the secondary side [5]. Bi-directional signal transmission is possible in this type of isolation, which reduces the number of channels required in data transmissions. However, the sensitivity to high dv/dt common noise and difficulties in transmitting frequencies close to the DC level affect the overall performance of the capacitive isolation. The optical isolator uses light as a transmission media, which can work ideally from DC to any frequency [6]. The light intensity of LED (light source) degrades over time, affecting the control signal integrity.

In the magnetic isolation, two coils, namely primary and secondary, transmit signals from the controller to the driver, which can be cored or coreless [4]. The coil-based transformer has a much higher CMTI, which makes it less affected by dv/dt common noise. The cored magnetic transformer shows better performance than the coreless transformer. However, a coreless transformer consumes less area, making it easier to be implemented on chip. A single-layer, non-overlapping coil-based on-chip transformer for a digital isolation system was reported [7]. The transformer topology occupies a large area while having a low mutual inductance. Another transformer implemented a multi-layer, non-overlapping coil transformer to increase the self-inductance of both primary and secondary coils [8]. Aside from consuming a large area, it generates an imbalance flux linkage between layers, which results in poor signal transmission.

This paper demonstrates a coreless, 6-layer overlapping coil on-chip digital transformer. The topology is three sets of interwound coils composed of 6 metal layers that produce a high mutual inductance while having an area the same as a single coil. The design is implemented using standard 0.18 μm HV CMOS process (T18HVG2). The high mutual inductance is verified based on the time period comparison between the waveforms at the primary side and the secondary side.

II. Analysis of on-chip coreless transformer

The equivalent model used in the proposed on-chip transformer is shown in Fig. 1 [9]. The coil resistance in the model (R_{PRI} and R_{SEC}) caused ohmic losses in the transformer. L_{PRI} and L_{SEC} are the self-inductances which affect the overall frequency response of the transformer. The higher the self-inductance, the wider the operation frequency range. The distance between the primary and secondary coil winding and between turns is small, resulting in a parasitic coupling capacitance C_{CPT}. The C_{CPT}, however, reduces the CMTI of

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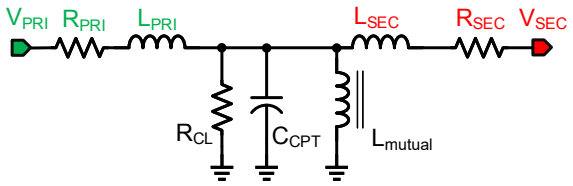

Fig. 1. Pulse transformer equivalent circuit model [9]

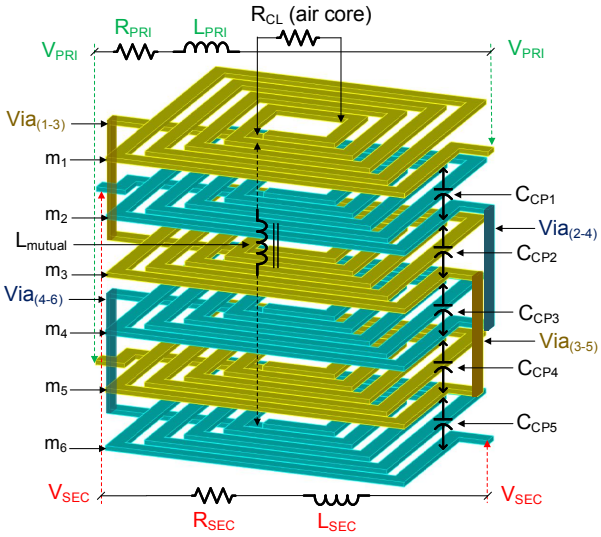

Fig. 2. Proposed 6-layer overlapping on-chip digital transformer

the on-chip transformer, because it is affected by high dv/dt. The mutual inductance (L_{mutual}) defines the effectiveness of signal transmission between primary and secondary coils. The value of mutual inductance varies directly with the ratio of L_{PRI} and L_{SEC}. The higher the mutual inductance, the better the signal integrity. Finally, the R_{CL} (core loss) consists of hysteresis and eddy current losses, degrading the mutual inductance of the on-chip transformer.

Fig. 2 shows the topology for the proposed on-chip digital transformer. The transformer consists of 6 metal layers, three interwound alternating metal layers for primary and secondary sides. Each layer for both primary and secondary are coupled through vias ($\text{Via}_{[1-3,3-5]}$ for primary and $\text{Via}_{[2-4,4-6]}$ for secondary). The design is considered an air-cored transformer, since no core medium is employed. Each layer is wound in a square spiral pattern for higher primary (L_{PRI}) and secondary (L_{SEC}) coil self-inductance, which also produces high mutual inductance (L_{mutual}) in between [10]. Square spiral pattern coil also provides a symmetrical magnetic field for efficient coupling.

The top and side perspective views for a single metal layer are shown in Fig. 3 (a) and (b), respectively. Each layer consists of t_N turns with a metal width of m_{width} and m_{space} separation between each consecutive turn. The outermost turn t_N has a width and length of t_{out_width} and t_{out_length}, respectively. The innermost turn t_1 has an effective width (excluding m_{width}) of t_{in_width} and length of t_{in_length}.

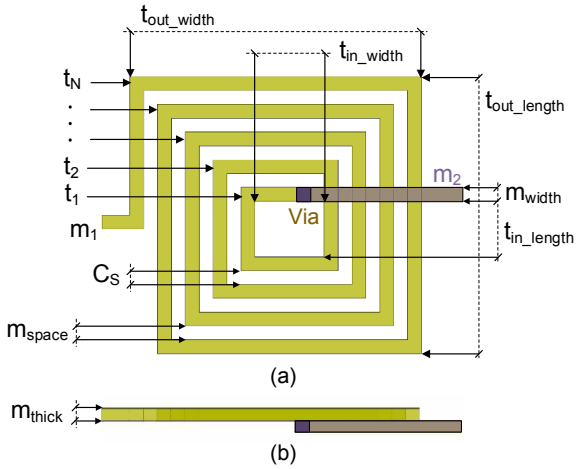

Fig. 3. The proposed on-chip digital transformer (a) top view; (b) side view

Finally, m_{thick} represents the thickness of each metal and C_S is the parasitic capacitance between turns.

A. Self and mutual inductance, and metal resistance

The coil resistance (R_{PRI} and R_{SEC}) causes ohmic losses in the transformer. It is the resistance across the endpoints of primary/secondary coils. The resistance of the primary and secondary coil can be approximated using Eqn. (1) and (2), respectively.

$$R_{PRI} = R_1 + R_{Via_{1-3}} + R_3 + R_{Via_{3-5}} + R_5 \quad (1)$$

$$R_{SEC} = R_2 + R_{Via_{2-4}} + R_4 + R_{Via_{4-6}} + R_6 \quad (2)$$

where $R_{[1-6]}$ are individual metal resistance of layers 1 to 6 and $\text{R}_{Via[1-3,3-5,2-4,4-6]}$ are the via contact resistance between different layers. The equivalent resistance of the metal trace of each layer (R_m) is given by Eqn. (3) [11].

$$R_m = \rho \cdot \frac{Le_{Total}}{m_{thick} \cdot m_{width}}[1 + \alpha(Temp - 25°C)] \quad (3)$$

where ρ is the specific resistivity of the material, Le_{Total} is the total trace length (total metal length), and α is the temperature coefficient of the metal layer used.

The total primary/secondary self-inductance (L_{PRI}/L_{SEC}) is the inductance across endpoints of primary/secondary coils. The summation of the individual layer inductance will result in a higher self-inductance of primary and secondary coils represented by Eqn. (4),

$$L_{PRI} = L_1 + L_3 + L_5; \quad L_{SEC} = L_2 + L_4 + L_6 \quad (4)$$

where $L_{[1-6]}$ are the individual metal inductance of layers 1 to 6. The inductance value of a single metal (L_m) layer can be approximated using Eqn. (5) [12].

$$L_m = \frac{1.27 \cdot \mu_0 \cdot N^2 \cdot d_a}{2}\left(\ln\left(\frac{2.07}{\phi} + 0.18\phi + 0.13\phi^2\right)\right) \quad (5)$$

where μ_0 is the free space permeability, ϕ is the fill ratio, N is the number of turns, and $d_a = (t_{oud\_width} + t_{in\_width})/2$ (for $t_{out\_width} = t_{out\_length}$ and $t_{in\_width} = t_{in\_length}$).

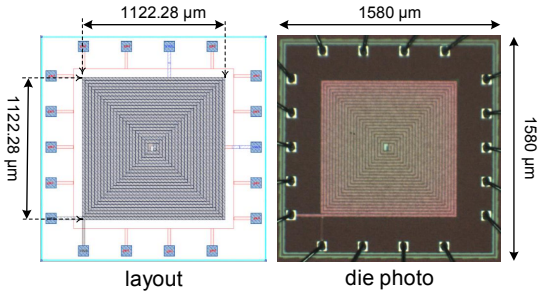

Fig. 4. Digital transformer layout and die photo

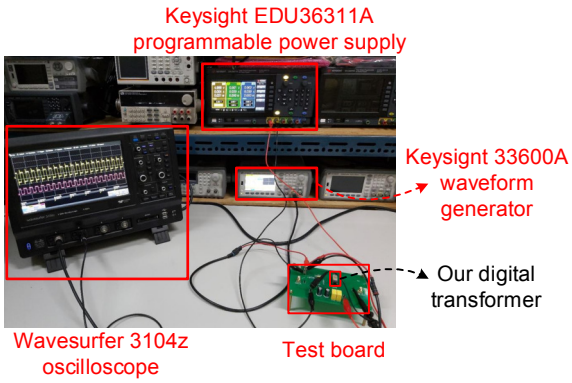

Fig. 5. Research measurement set-up

The effectiveness during data transmission is defined by mutual inductance between primary and secondary coils. The coupling coefficient (k_{coup}) between the primary and secondary coils affects the value of L_{mutual}. In the proposed design, the metal layers are stacked on top of each other to increase k_{coup}, which also increases L_{mutual}. The L_{mutual} is characterized by Eqn. (6).

$$L_{mutual} = K_{coup}\sqrt{L_{PRI} \cdot L_{SEC}} \tag{6}$$

B. Coupling capacitance and core loss

Coupling capacitance (C_{CPT}) limits the output gain of the digital transformer in high-frequency operations and is sensitive to high dv/dt fluctuation. A high C_{CPT} value limits detection capability at the secondary coil, resulting in a low CMTI. C_{CPT} is the combination of interwind ($C_{CP[1-5]}$) and layer (C_S) coupling capacitance given in Eqn. (7).

$$C_{CPT} = C_{CP[1-5]} + C_S \tag{7}$$

given,

$$C_{CP[1-5]} = \frac{\epsilon_0\epsilon_r \cdot S}{d},\ C_S = \frac{0.9 \cdot \epsilon_0\epsilon_r \cdot m_{thick} \cdot m_{space}}{m_{width}} \tag{8}$$

where d and S are the distance and overlapping area between adjacent layers, respectively.

Core loss (R_{CL}) occurs due to the changing magnetic flux emitted by the primary coil during core (air) magnetization and demagnetization. R_{CL} is proportional to the alternating magnetic flux and operating frequency.

III. Measurement and Analysis

The layout and die photo of the on-chip digital transformer fabricated in TSMC 0.18 μm HV CMOS (T18HVG2) technology are illustrated in Fig. 4. The transformer design has a core area of 1122.28 $\times$ 1128.28 μm^2 with an overall chip area of 1580 $\times$ 1580 μm^2.

The measurement setup for the proposed digital transformer is shown in Fig. 5. A 5 V voltage supply is delivered by the Keysight EDU36311A programmable power supply. The Keysignt 33600A waveform generator provides a V_{PRI} pulse signal, while output V_{SEC} is observed using a Wavesurfer 3104z oscilloscope.

The proposed on-chip transformer output waveform (V_{SEC}) at operating frequencies ($f_{operating}$) of 10 kHz, 100 kHz, 1 MHz, and 10 MHz are illustrated in Fig. 6. A bipolar squarewave with $+V_{pk}$ = 5 V and -V_{pk} = -5 V is applied to V_{PRI}, since L_{mutual} only occurs when the transformer input is an alternating signal. The measured V_{SEC} output frequency (f_{VSEC}) projects the same frequency as the $f_{operating}$, verifying its wide frequency range and strong mutual inductance. The worst t_{rise} and t_{fall} occur at f_{VPRI} = 10 MHz, with 9.2 ns and 8.9 ns, respectively.

Table I tabulates the t_{rise}, t_{fall}, and the t_{pro_delay} for six chips to check the reliability of the design. The average t_{rise}, t_{fall}, and t_{pro_delay} are 9.2 ns, 9.6 ns, and 43.8 ns, respectively. The worst-case variation for all parameters is less than 8 %, proving the robustness of the transformer design.

TABLE I
Different chips' rise and fall time, and propagation delay

Chip no.	t_{rise} (ns)	t_{fall} (ns)	t_{pro_delay} (ns)
1	9.5	10.1	44.2
2	9.2	8.9	44.2
3	9.2	9.1	43.4
4	9.0	10.3	43.3
5	9.6	9.9	43.8
6	8.9	9.2	44.0

TABLE II
V_{PRI} and V_{SEC} % duty cycle comparison and V_{SEC} rise time and fall time

% duty cycle		V_{SEC}	
T_{PRI_PWM} (%)	T_{SEC_PWM} (%)	t_{rise} (ns)	$t_{fall}(ns)$
5.0	6.4	7.4	8.3
10.0	10.5	7.9	7.0
20.0	20.3	8.0	8.9
30.0	30.2	7.6	7.9
40.0	40.2	7.3	7.9
50.0	50.1	7.8	8.0
60.0	60.1	7.4	7.1
70.0	70.1	7.9	8.0
80.0	79.9	7.6	7.9
90.0	89.8	8.3	7.9
95.0	94.4	8.0	7.8

TABLE III
ON-CHIP DIGITAL TRANSFORMER COMPARISON

	[13]	[7]	[8]	This work*
Year	2012	2017	2020	2023
Publication	JSSC	ISSCC	MWSCAS	
Process (μm)	0.35	0.5	0.18	0.18 T18HVG2
Verification	Meas.	Meas.	Post-sim.	Meas.
Modulation architecture	Pulse polarity	On-off keying	Pulse polarity	Pulse polarity
Multi-layer	×	×	✓	✓
Overlapping	✓	×	×	✓
$f_{operating}$	250 MHz	500 MHz	–	10 kHz - 10 MHz
t_{pro_delay}	5.5 ns	–	15 ns	44.0 ns
CMTI	35 kVμs	50 kVμs	–	100 kVμs

*Digital transformer only

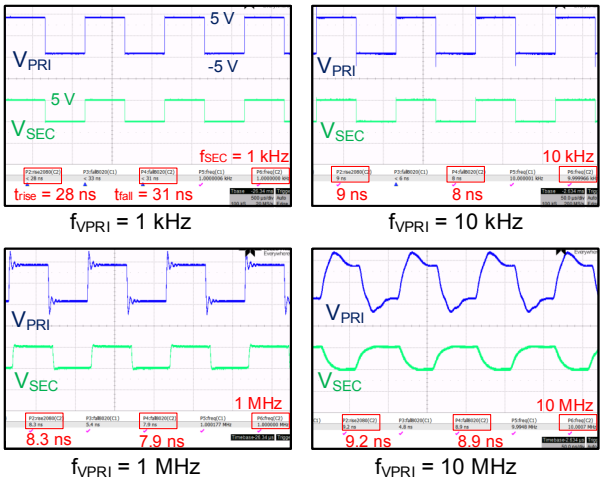

Fig. 6. V_{SEC} waveforms: t_{rise}, and t_{fall} at f_{VPRI} = 1 kHz, 10 kHz, 1 MHz, and 10 MHz

Fig. 7 shows the output waveforms for various % duty cycles at $f_{operating}$ = 100 KHz to determine whether the transformer design is suitable for power converter applications. The PWM outputs are 6.4, 30.2, 70.1, and 94.4 % when the input % duty cycle of 5, 30, 70, and 95 %, respectively. Table II summarizes the comparison of % duty cycle, t_{rise}, and t_{fall} for different values of PMW inputs. The worst error occurs at 5 % duty cycle input, producing 6.4 % output duty cycle (1.4 % variation). Notably, t_{rise} and t_{fall} exhibit a minimal deviation. These measurement data show that the proposed transformer is suitable for power conversion applications.

Fig. 8 shows the measured power consumption of the digital transformer for all chips. Each measured chip has nearly the same power consumption, with the lowest being 50 mW and the highest being 52 mW.

Tabulated in Table III is the performance comparison with related prior works. Our digital transformer implements multi-layer and overlapping topology to increase the mutual inductance without sacrificing the area. Though the overlapping approach produces higher coupling capacitance, our CMTI is superior to other works, since it has achieved higher self-

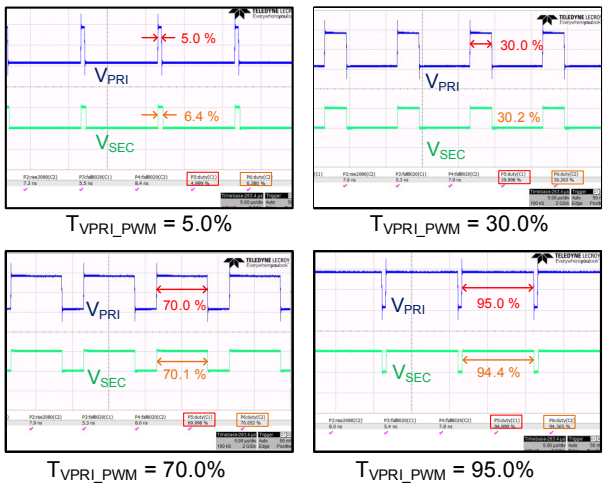

Fig. 7. V_{SEC} waveforms: t_{rise}, and t_{fall} at different V_{PRI} % duty cycle

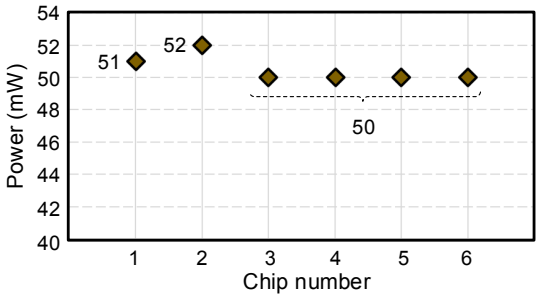

Fig. 8. Power consumption of different chips

inductance. The higher value of propagation delay is caused by higher coupling capacitance at 10 MHz. Our design includes thorough measurement data that validate the proposed digital transformer's functionality, accuracy, applicability, and effectiveness.

IV. CONCLUSION

This research presents an on-chip, multi-layer digital transformer fabricated using T18HVG2 technology. The multi-level, multi-layer transformer topology increases the mutual inductance with low on-chip area. The functionality of the proposed transformer has been validated through measurements (six chips) having the worst-case rise time, fall time, and propagation delay, deviation of 8 %. In addition, the chips are tested at different % duty cycles, having 1.4 % worst variation in the output PWM, which makes it suitable in power conversion applications.

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REFERENCES

[1] R. A. Bilir, N. Altıntaş, A. Bilir, E. Meşe, and Z. Tosunoğlu, "A comparative study on power mosfet reliability and failure modes," in *Proc. 2019 18th International Symposium INFOTEH-JAHORINA (INFOTEH)*, March 2019, pp. 1–5.

[2] D. Han, S. Kim, X. Dong, Z. Guo, H. Li, J. Moon, Y. Li, and F. Z. Peng, "An integrated active gate driver for half-bridge sic mosfet power modules," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2022, pp. 1413–1418.

[3] S.-Y. Li, W.-C. Hung, T.-W. Wang, Y.-T. Hsu, K.-H. Chen, K.-L. Zheng, Y.-H. Lin, S.-R. Lin, and T.-Y. Tsai, "20.1 a high common-mode transient immunity gan-on-soi gate driver for high dv/dt sic power switch," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2023, pp. 302–304.

[4] Infineon, *Advantages of coreless-transformer gate drivers over gate drive optocouplers*, Revised April 2022. [Online]. Available: https://www.infineon.com/dgdl/Infineon-AN-2022_01_Advantages_of_coreless_transformer_gate_drivers_over_gate_drive_optocouplers-ApplicationNotes-v01_01-EN.pdf

[5] P. Mahalingam, D. Guiling, and S. Lee, "Manufacturing challenges and method of fabrication of on-chip capacitive digital isolators," in *Proc. 2007 International Symposium on Semiconductor Manufacturing*, Oct. 2007, pp. 1–4.

[6] T. Mizumoto, Y. Shoji, M. Itoh, and R. Takei, "On-chip optical isolators and silicon photonics," in *Proc. 2012 17th Opto-Electronics and Communications Conference*, July 2012, pp. 877–878.

[7] S. Mukherjee, A. N. Bhat, K. A. Shrivastava, M. Bonu, B. Sutton, V. Gopinathan, G. Thiagarajan, A. Patki, J. Malakar, and N. Krishnapura, "25.4 a 500Mb/s 200pJ/b die-to-die bidirectional link with 24kV surge isolation and 50kV/μs CMR using resonant inductive coupling in 0.18μm CMOS," in *Proc. 2017 IEEE International Solid-State Circuits Conference (ISSCC)*, March 2017, pp. 434–435.

[8] I. Altoobaji, M. Ali, A. Hassan, M. Nabavi, Y. Audet, and A. Lakhssassi, "A fully integrated on-chip inductive digital isolator: Design investigation and simulation," in *Proc. 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2020, pp. 868–871.

[9] Texas Instruments, *Interfacing the ADS1202 Modulator With a Pulse Transformer in Galvanically Isolated Systems*, June 2003. [Online]. Available: https://www.ti.com/lit/an/sbaa096/sbaa096.pdf

[10] S. Tayenjam, V. N. R. Vanukuru, and S. Kumaravel, "A pcell design methodology for automatic layout generation of spiral inductor using skill script," in *Proc. 2017 International conference on Microelectronic Devices, Circuits and Systems (ICMDCS)*, Aug. 2017, pp. 1–4.

[11] A. Rodriguez-Echevarria, C. Lopez-Perez, and C. Correa-Betanzo, "A novel approach based on trace resistance compensation for summing networks for high-current measurement," *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 7, pp. 4968–4974, July 2020.

[12] S. Mohan, M. del Mar Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.

[13] S. Kaeriyama, S. Uchida, M. Furumiya, M. Okada, T. Maeda, and M. Mizuno, "A 2.5 kv isolation 35 kv/us cmr 250 mbps digital isolator in standard cmos with a small transformer driving technique," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 435–443, Feb. 2012.