An On-chip Temperature Sensor with 1°C Resolution And Wide Detection Range Using 180-nm CMOS Process

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***Abstract*—This work introduces a temperature sensor with a 1°C resolution and a sensing range of –40°C ∼ 80°C. The temperature sensor is composed of a temperature and current adjustment circuit, a multipath charging and discharging circuit, a voltage window comparator (VWC), and a path selector. The proposed sensor was realized using a typical 180-nm CMOS process. The post-layout simulation shows a maximum temperature error of 0.77°C and a linearity error of less than 1% in the worst process corner. The maximum output frequency is 0.9 MHz, with a core area of 0.331 mm^2.**

***Index Terms*—multipath charging and discharging, linearity error, PTAT, CTAT, duty cycle**

I. Introduction

The BJT-based temperature-to-digital-converter (TDC) temperature sensors usually employ analog-to-digital converters (ADC) which increase system complexity and can't achieve high resolutions [1]. Voltage or current mode temperature sensors, where the temperature is realized in terms of a thermal current or voltage complementary or proportional to absolute temperature (CTAT or PTAT), have been known as a better alternative [2]. This investigation proposes to generate a difference current from CTAT and PTAT currents, which has CTAT behavior, to ensure that the temperature sensor can detect every 1°C change without missing codes. A novel multipath charging and discharging circuit helps to maintain the duty cycle of the output signal in the operating cycle in all PVT (process, voltage, temperature) corners.

II. Design of Proposed Temperature Sensor

The proposed temperature sensor's functional block diagram is illustrated in Fig. 1.

A. Temperature and Current Adjustment Circuit

The Temperature and Current Adjustment Circuit is shown in Fig. 2. $\mathrm{I_{CTAT}(T)}$ current is generated with a P+ polysilicon resistor ($\mathrm{R_{201}}$) whose temperature coefficients is negative, i.e, -1.692×10^{-3}. A resistor with a larger positive temperature coefficient is selected in the current generator of PTAT. The $\mathrm{I_{PTAT}(T)}$ current is generated with an NWELL under OD resistor ($\mathrm{R_{202}}$) having a positive temperature coefficient, i.e., 3.68×10^{-3}. Assume that the $\mathrm{I_{CTAT}(T)}$ changes by -1 μA per 1°C, while the $\mathrm{I_{PTAT}(T)}$ current changes by 0.5 μA per 1°C. Both resistors are calibrated to reduce temperature variations. The temperature coefficient values are provided by manufacturing units. The $\mathrm{I_{CTAT}(T)}$ is a complementary current variation with temperature, as shown in Eqn. (1), and the $\mathrm{I_{PTAT}(T)}$ is proportional current variation with temperature, as shown in Eqn. (2) [3]. The current subtractor produces a difference current $\mathrm{I_{temp}(T)}$ from $\mathrm{I_{CTAT}(T)}$ and $\mathrm{I_{PTAT}(T)}$, is given by Eqn. (3), which is complementary to temperature variations. This will improve the resolution by increasing the current gap corresponding to each 1°C temperature to be detected and making the output current small so that there will be no missing codes.

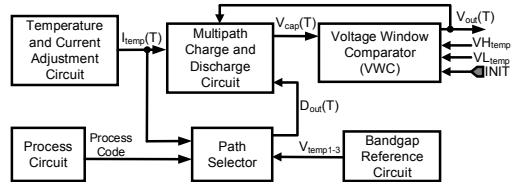

Fig. 1. System view of the proposed temperature sensor

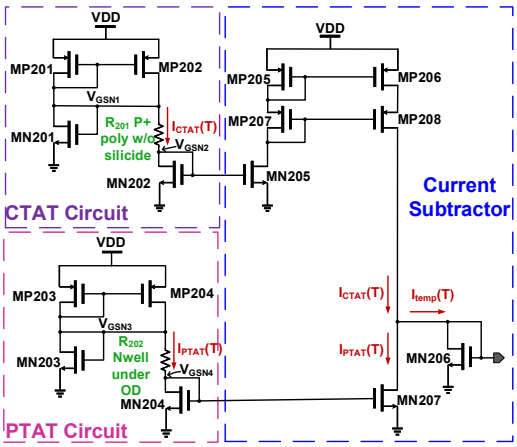

Fig. 2. Schematic of Temperature and Current Adjustment Circuit

$$\mathrm{I_{CTAT}(T) = I_{CTAT}(T_0) \cdot (1 + TCI_{CTAT}(T - T_0))} \quad (1)$$

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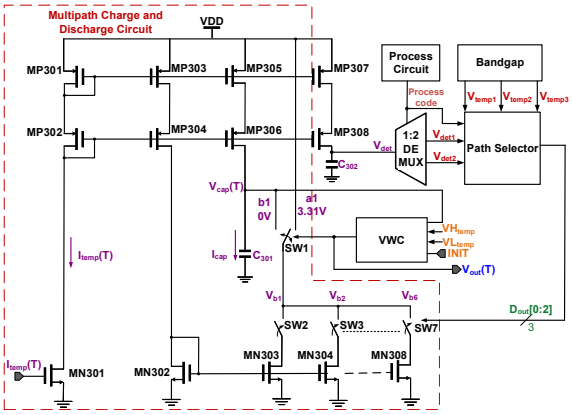
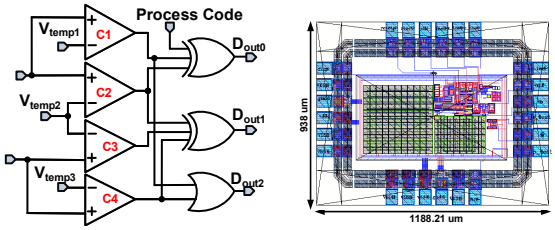


Fig. 3. Multipath Charge and Discharge circuit



(a) (b)

Fig. 4. (a) Path selector; (b) Layout of the temperature sensor

$$I_{PTAT}(T) = I_{PTAT}(T_0) \cdot (1 + TCI_{PTAT}(T - T_0)) \quad (2)$$

$$I_{temp}(T) = I_{CTAT}(T) - I_{PTAT}(T) \quad (3)$$

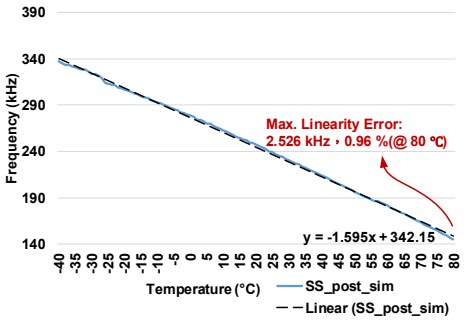
B. Multipath Charge and Discharge Circuit (MCDC)

The corresponding frequency generated by the MCDC's output depends on the $I_{temp}(T)$ current. The changes in the duty cycle impact the overall linearity of the system. The working cycle is from 49.7% to 50.615%. Additionally, relying solely on the discharge current path of a single transistor is insufficient to meet the requirements of a wide temperature range, spanning from -40°C to 80°C [4]. Therefore, this study proposes a novel Multipath Charge and Discharge Circuit (MCDC) with a Path Selector, as illustrated in Fig. 3. This MCDC circuit generates a voltage drop V_{cap} across the capacitor C_{301}. It is sent to the VWC [5] to be compared against VH_{temp} and VL_{temp}. The Path Selector determines the discharge path. The output frequency can be expressed as shown in Eqn. (4). After careful calibration, the capacitance value is determined to be 100 pF, and the current difference is adjusted to 0.75 μA/°C.

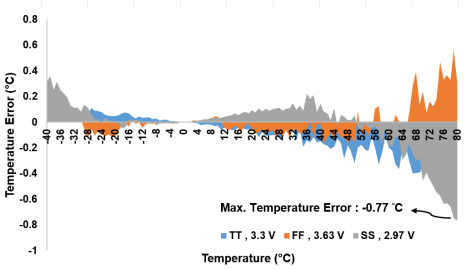
$$f_{out}(T) = \frac{I_{temp}(T)}{2 \cdot C_{301} \cdot (VH_{temp} - VL_{temp})} \quad (4)$$

III. Post-Layout Simulations

Using a standard TSMC 180-nm CMOS process, the temperature sensor is developed. It has a total area of 1114.5 mm^2 with a core area of 331.9 mm^2. Fig. 4(b) describes the layout. Fig. 5(a) illustrates the worst-case linear regression curve of temperature versus frequency in the SS corner, with a voltage of 2.97 V. The current generating circuit's current decreases as the temperature rises. As a result, it is challenging to drive the transistor in the slow corner. After the adjustment carried out by MCDC, the maximum linearity error is 0.96%. The maximum temperature error in extreme corners is 0.77°C is shown in Fig. 5(b).



(a)



(b)

Fig. 5. (a) Worst-case temperature vs. frequency simulation in SS corners; (b) Temperature error histogram

IV. Conclusion

A temperature sensor of range –40°C ∼ 80°C with high linearity is implemented using the TSMC 180-nm CMOS process. Based on the post-layout simulations, our design exhibited high linearity with a maximum linearity error of 0.96% with 1°C resolution.

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